Analysis of Switched-Capacitor Common-Mode Feedback Circuit

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***Abstract*—A detailed analysis of the dc behavior of switched-capacitor common-mode feedback circuit (SC-CMFB) is presented. A mathematical model, useful for analysis, is developed and the expressions for the output common-mode (CM) voltage, with and without considering the charge injection of switches and leakage currents, are derived. Further, the expression for dc CM settling time, is presented. The effect of parasitic capacitances, dc CM gain, charge injection error, and leakage currents, on the steady–state value of the dc CM voltage is analyzed and design guidelines to minimize these errors are presented. Finally, an improved version of the SC-CMFB circuit is analyzed. This circuit has very low errors due to charge injection and leakage currents and settles much faster than the traditional SC-CMFB circuit.**

***Index Terms*—Charge injection, circuit analysis, common-mode feedback (CMFB), feedback circuit, leakage currents, switched capacitor.**

I. Introduction

THE use of fully-differential circuits in implementing high-performance analog integrated circuits in a mixed-signal environment is becoming increasingly popular. Fully-differential circuits provide much better rejection of common-mode (CM) noise and high-frequency power-supply variations compared to their single-ended counterparts. However, since the CM loop gain from the external feedback loop around the fully-differential opamp is small, the CM voltage in fully-differential circuits is not precisely defined. Without proper control, the output CM voltage tends to drift to the supply rails due to power-supply variations, process variations, offsets, etc. Hence, an additional CM feedback loop is usually necessary. The circuit comprising this CM feedback loop is called the CM feedback (CMFB) circuit.

The design of a good CM feedback circuit can be quite challenging [4]. In most applications, the slew rate and unity-gain frequency of the CM loop should be comparable to that of the differential loop to avoid output signal distortion resulting from clipping due to slow settling of the output CM voltage. The number of parasitic poles in the CM loop should be minimized. Also, the gain of the CM loop should be sufficiently large so as to obtain the CM voltage within the desired accuracy. To be practical, the CM loop should not add significantly to the differential loop's load. For good stability, the CM loop should be adequately compensated by ensuring a good phase margin and a fast settling step response. Minimizing the number of nodes in the CM path simplifies compensation without limiting the speed [4].

The main advantages of SC-CMFBs are that they impose no restrictions on the maximum allowable differential input signals, have no additional parasitic poles in the CM loop, and are highly linear. However, SC-CMFBs inject nonlinear clock-feedthrough noise into the opamp output nodes and increase the load capacitance that needs to be driven by the opamp. Hence, SC-CMFBs are typically only used in switched-capacitor applications rather than continuous-time applications [4].

SC-CMFBs are widely used in fully-differential switched-capacitor circuits. However, a detailed analysis of the dc behavior of the SC-CMFB circuit and its nonideal effects, does not exist in the literature. This paper presents a detailed analysis of the dc behavior of the SC-CMFB circuit, along with its nonideal effects. In addition, this paper also provides design guidelines to improve the performance of the circuit. An improved version of the SC-CMFB circuit described in [5] is also analyzed. The outline of the paper is as follows. In Section II, switched-capacitor CMFB circuit design and operation are discussed and a half-circuit equivalent, suitable for mathematical analysis of dc behavior, is developed. In Section III, the dc analysis of SC-CMFB circuit, ignoring charge injection, mismatch, leakage currents and switch resistances, is presented and a closed-form expression of the dc output CM voltage is derived. In Section IV, the same analysis as in Section III, is carried out considering the charge injection due to switches and the leakage currents. In Section V, certain issues related with the design of SC-CMFBs such as the CM gain and loop bandwidth, CM dc settling time, steady–state CM voltage values, charge injection errors, and leakage current errors are discussed and design guidelines, for faster settling and lower clock-feedthrough noise, are given. Finally, a modified version of the traditional SC-CMFB circuit as described in [5], with faster settling time and higher accuracy of the steady–state value, is analyzed.

II. SC-CMFB and its Model

A. SC-CMFB Design

In general, a CMFB circuit consists of a CM sense/detect circuit and a comparison amplifier. The output voltage of the sense circuit is compared with the desired CM voltage and a bias voltage required to control the current sources of the opamp is produced.

The basic principle used in SC-CMFBs is described as follows. The capacitors C_1 and C_2 are precharged to V_{DC} with

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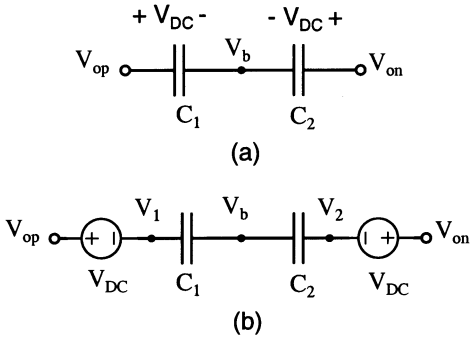


Fig. 1. Generation of CM voltage and level-shifting.

the polarity as shown in Fig. 1(a). The output voltages $V_{\rm op}$ and $V_{\rm on}$ are level-shifted by V_{DC} and then averaged by capacitors C_1 and C_2 to produce the desired bias voltage. As shown in Fig. 1(b), capacitors C_1 and C_2 charged to voltage V_{DC} with the polarity indicated, can be represented with a series voltage source of value V_{DC}.

Equating the current through C_1 and C_2,

$$V_b = \frac{(C_1 \cdot V_1 + C_2 \cdot V_2)}{(C_1 + C_2)}. \tag{1.1}$$

Since $V_1 = V_{\rm op} - V_{DC}$ and $V_2 = V_{\rm on} - V_{DC}$, substituting V_1 and V_2 and using $C_1 = C_2$ in (1.1) above yields

$$\begin{aligned} V_b &= \left[\frac{(C_1 \cdot V_{\rm op} + C_2 \cdot V_{\rm on})}{(C_1 + C_2)}\right] - V_{DC} \\ &= \frac{(V_{\rm op} + V_{\rm on})}{2} - V_{DC} \\ &= V_{\rm cm} - V_{DC} \end{aligned} \tag{1.2}$$

where $V_{\rm cm} = (V_{\rm op} + V_{\rm on})/2$ is the output CM voltage. *As evident in (1.2), the output CM sensing and comparison with a reference voltage (V_{DC}) is achieved directly with capacitors precharged to a desired offset voltage.*

The detailed implementation of a switched-capacitor CMFB circuit [1], [2] in conjunction with a folded-cascode amplifier implementation, is shown in Fig. 2. The input stage, shown as a box, typically consists of a pMOS differential pair with the drains of pMOS transistors connected to nodes A and B shown in Fig. 2. Transistors $M_{n1+}, M_{n1-}, M_{n2+}, M_{n2-}$ along with current sources I_{D1}, form the output stage of the folded-cascode amplifier. The rest of the elements in Fig. 2 constitute the SC-CMFB circuit.

During clock phase ϕ_2, C_{1+} and C_{1-} are connected to C_{2+} and C_{2-}, respectively. The dc voltage across C_{2+} and C_{2-} is determined by C_{1+} and C_{1-}, respectively, and is refreshed every ϕ_2 clock phase. During clock phase ϕ_1, C_{1+} and C_{1-} are charged to $V_{\rm cmref} - V_{\rm bias}$ and capacitors C_{2+} and C_{2-} generate the control voltage V_b, level-shifting the average output voltage by $V_{\rm cmref} - V_{\rm bias}$ as described in (1.2) above. Overall, switches S_{1+}, S_{1-}, S_{2+}, S_{2-}, S_{3+}, S_{3-}, and S_{4+}, S_{4-} along with capacitors C_{1+} and C_{1-} form a differential resistance and the whole circuit acts like a simple low-pass filter having a dc input voltage $V_{DC} = V_{\rm cmref} - V_{\rm bias}$. Note, that if the circuit is symmetric, then the voltages at nodes n_1 and n_2 are identical and these nodes can be shorted together. Thus, S_{1+}, S_{1-} can be combined into S_1 and S_{2+}, S_{2-} into S_2, resulting in a total of six switches.

Let us now understand how the output CM is precisely defined when the circuit reaches steady–state. During the steady–state, if the input gate–source voltage (V_b) of M_{n1+} and M_{n1-} is precisely defined, then the output CM voltage is precisely defined according to (1.2), i.e., $V_{\rm cm} = V_b + V_{\rm cmref} - V_{\rm bias}$ where $V_b = V_{\rm bias}$ typically. The gate–source voltage of transistors M_{n1+} and M_{n1-} is precisely defined by the following action. Transistors M_{n1+} and M_{n1-} act as *constant* current sources of value I_D where $I_D = I_{D1} + I_{D2}$ as shown in Fig. 2. If the transistors M_{n1+} and M_{n1-} are sized to operate in saturation, then gate–source voltage V_{gs}, of value V_B is determined such that it satisfies the equation $I_D = f(V_{gs}, V_{ds})$ for some I_D and V_{ds}. Note that V_{ds} of M_{n1+} and M_{n1-} is determined by the bias voltage V_{casc} and V_{gs} of M_{n2+} and M_{n2-}, respectively, and its almost constant due to cascoding. Hence, V_B is also constant. The charge necessary to form this voltage $V_{gs} = V_B$ on C_{p2} is drawn from C_{2+} and C_{2-}, which in turn, draw the charge from nodes V_{o+} and V_{o-}, respectively. The circuit configuration works like a CM OTA with the input CM defined to be V_B and a low-frequency gain of $A_{\rm cm}$. Thus, the output CM voltage $V_{\rm cm}$ is precisely defined. Further, due to the feedback provided by capacitors C_{2+} and C_{2-} around the high CM gain OTA, the node V_b acts like a virtual ground and its value remains almost constant ($V_b = V_B$) during the switched-capacitor transients or the output CM variations.

Once the CM voltage is defined at the output nodes after startup, the CM is controlled by the negative feedback action of the CM loop. Any CM variation at the output nodes is coupled at node V_b, via capacitor C_{2+}, and C_{2-}. As V_b changes, the gate–source voltage of transistors M_{n1+}, M_{n1-} changes, which in turn, changes the current sunk by these transistors, cancelling the variation of the output CM. Let us assume that a positive CM signal is present at the output. This positive variation will cause the currents in both M_{n1+}, M_{n1-} to increase, decreasing the output CM voltage and stabilizing it. Thus, as long as the CM loop gain is large enough and has enough bandwidth to stabilize fast CM variations, the CM output voltage is always maintained at the reference CM value.

B. SC-CMFB Model for dc Analysis

The convention for the SC-CMFB analysis used in the rest of the paper is defined as follows: $V(nT)$ denotes the voltage at the end of n^{th} clock cycle, and T is the clock period. In discrete domain, this is denoted as $V[n]$. The steady–state value is denoted as $V[\infty]$ where $V[\infty] = \lim_{n\to\infty} V[n]$. The motivation for proposing a new SC-CMFB model for dc analysis is as follows.

Very often in the literature, the CM amplifier in SC-CMFB circuit is modeled and analyzed for ac as well as dc behavior [3]. The CM amplifier is denoted as a single input amplifier with a gain of $-A_{\rm cm}$ and used both for ac and dc analysis. However, when such a model is used, it can be shown that the steady–state voltage difference across the feedback capacitor, $V_o[\infty] - V_b[\infty]$ in Fig. 2, is precisely defined to be $V_{\rm cmref} - V_{\rm bias}$ but the individual steady–state node voltages $V_o[\infty]$ and $V_b[\infty]$ are not defined. In order to precisely establish the output CM voltage,

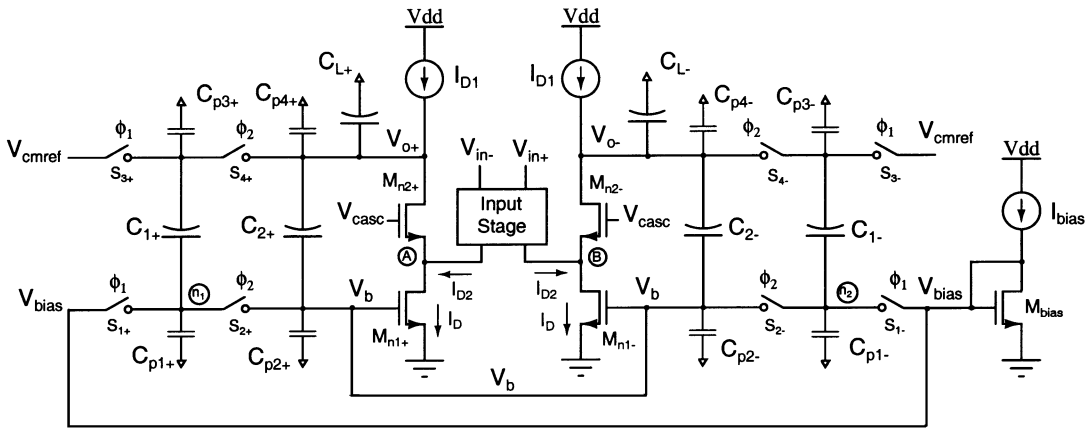


Fig. 2. A switched-capacitor CMFB circuit with a folded-cascode amplifier.

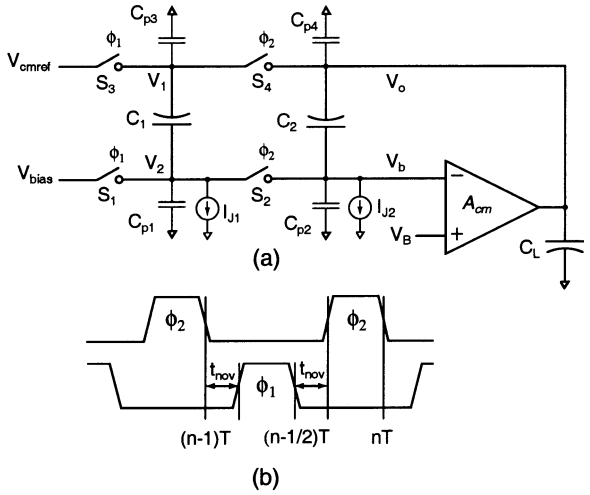


Fig. 3. (a) SC-CMFB half-circuit equivalent dc model. (b) Clock Waveforms.

$V_b[\infty]$ has to be defined. However, such a model fails to explain how $V_b[\infty]$ is defined. Hence, a model useful for dc analysis is proposed as shown in Fig. 3(a). If the circuit shown in Fig. 2 is fully-symmetric and there are no mismatches, then it can be replaced by a half-circuit equivalent model as shown in Fig. 3(a).

Note that the opamp with low-frequency gain $A_{\rm cm}$ represent the CM amplifier formed by M_{n1+}, M_{n1-}, M_{n2+}, M_{n2-} and the current sources I_{D1}. *The modeling of the single-ended CM OTA in Fig. 2 with a differential input CM OTA having a noninverting input voltage of V_B is the key point in analyzing the dc behavior of the SC-CMFB circuit.* As shown in Fig. 3(a), node V_b forms the inverting input of the amplifier connected in negative feedback (and hence, V_b acts like a virtual ground) as in Fig. 2. However, the noninverting input of the OTA connected to V_B is *implied* in Fig. 2. Since the feedback generates the bias voltage value V_B at the gate of transistors M_{n1+}, M_{n1-} and any deviation of voltage V_b from this bias voltage value V_B is amplified by the CM OTA, the representation of V_B as the positive input terminal in the model shown in Fig. 3(a) is justified. For simplicity, ideal switches with zero resistance, are considered for analysis, though in practice, MOS transistors are used to implement these switches. The dc leakage currents associated with the reverse-biased source and drain junctions of the MOS transistors acting as switches are also shown since they affect the dc analysis [3]. All other leakage currents are either supplied by a voltage source $(V_{\rm cmref})$ or by the OTA and, therefore, do not affect the analysis. This circuit model will be subsequently used for mathematical analysis of the dc behavior.

Using the model shown in Fig. 3(a), accurate expressions for $V_b[\infty]$, $V_o[\infty]$ and $V_o[\infty] - V_b[\infty]$ can be derived, as shown in Section III.

III. Analysis Without Considering Charge Injection and Leakage Currents

The analysis that follows in this section, is based on the following assumptions:

1) The SC-CMFB circuit is fully symmetric and there are no mismatches.
2) Switches are assumed to have a low resistance such that the settling time errors during any clock phase can be neglected.
3) Leakage currents and the charge injection of switches are ignored. (Analysis with the leakage currents and the charge-injection of switches is done in Section IV.)
4) CM amplifier has a low frequency gain of $A_{\rm cm}$.

Under the assumptions stated above, the circuit of Fig. 3(a) can be analyzed as follows:

Since nodes V_2 and V_b are high-impedance nodes from the dc point of view, charge is conserved at these nodes. The charge conservation equation, from the time instant $t = (n-1/2)T$ after switch S_1 opens till the time instant $t = nT$ before switch S_2 opens, at node V_b can be written as

$$\begin{aligned} &C_1 \cdot (V_{\rm bias} - V_{\rm cmref}) + C_{p1} \cdot V_{\rm bias} \\ &\quad C_2 \cdot \left(V_b\left[n - \frac{1}{2}\right] - V_o\left[n - \frac{1}{2}\right]\right) \\ &\quad + C_{p2} \cdot V_b\left[n - \frac{1}{2}\right] = (C_{p1} + C_{p2}) \\ &\quad \cdot V_b[n] + (C_1 + C_2) \cdot (V_b[n] - V_o[n]). \end{aligned} \tag{1.3}$$

Note that if there are no leakage currents, then the charge is conserved at node V_b during the period when ϕ_2 is low. Hence

$$\begin{aligned} V_b\left[n - \frac{1}{2}\right] &= V_b[n-1] \\ V_o[n - \frac{1}{2}] &= V_o[n-1]. \end{aligned} \tag{1.4}$$

Equation (1.4) can be used in (1.3) to eliminate $V_b[n-1/2]$ and $V_o[n-1/2]$, leading to

$$\begin{aligned} &C_1 \cdot (V_{\rm bias} - V_{\rm cmref}) + C_{p1} \cdot V_{\rm bias} + C_2 \\ &\cdot (V_b[n-1] - V_o[n-1]) + C_{p2} \cdot V_b[n-1] \\ &= (C_{p1}+C_{p2}) \cdot V_b[n] + (C_1 + C_2) \cdot (V_b[n] - V_o[n]) \,. \end{aligned} \tag{1.5}$$

Based on the equivalent dc model described in Section II, it can be written that

$$V_o[n] = A_{\rm cm} \cdot (V_B - V_b[n]) \tag{1.6}$$

Solving (1.5) and (1.6) to eliminate V_o, it can be written that

$$V_b[n] = K_b + \beta \cdot V_b[n-1] \tag{1.7}$$

where

$$\begin{aligned} K_b &= \frac{C_1 \cdot (A_{\rm cm} \cdot V_B - V_{\rm cmref}) + (C_1 + C_{p1}) \cdot V_{\rm bias}}{(C_1 + C_2) \cdot (A_{\rm cm} + 1) + C_{p1} + C_{p2}} \\ \beta &= \frac{C_2 \cdot (A_{\rm cm} + 1) + C_{p2}}{(C_1 + C_2) \cdot (A_{\rm cm} + 1) + C_{p1} + C_{p2}}. \end{aligned}$$

It is important to note from the above expression that $\beta < 1$.

Substituting the values of $V_b[n-i]$ recursively from $i = 1$ to n in (1.7) yields

$$\begin{aligned} V_b[n] &= K_b \cdot (1 + \beta) + \beta^2 \cdot V_b[n-2] \\ &= K_b \cdot \left(1 + \beta + \cdots + \beta^{n-1}\right) + \beta^n \cdot V_b[0] \\ &= K_b \cdot \left(\frac{1 - \beta^n}{1 - \beta}\right) + \beta^n \cdot V_b[0] \end{aligned} \tag{1.8}$$

where $V_b[0]$ denotes the initial voltage at node V_b at $t = 0$. The steady–state value or the final value of $V_b[n]$ denoted by $V_b[\infty]$ is given by

$$\begin{aligned} V_b[\infty] &= \lim_{n \to \infty} V_b[n] = \frac{K_b}{1 - \beta} \\ &= \frac{V_B + \left(\frac{1}{A_{\rm cm}}\right) \cdot \left[\left(1 + \frac{C_{p1}}{C_1}\right) \cdot V_{\rm bias} - V_{\rm cmref}\right]}{1 + \left(\frac{1}{A_{\rm cm}}\right) \cdot \left(1 + \frac{C_{p1}}{C_1}\right)} \end{aligned} \tag{1.9}$$

since $\beta < 1$. Thus, $V_b[n]$ can be written as

$$V_b[n] = V_b[\infty] + \beta^n \cdot (V_b[0] - V_b[\infty]) \tag{1.10}$$

Since $V_o[n] = A_{\rm cm} \cdot (V_B - V_b[n])$, an equation similar to (1.7) can be written as

$$V_o[n] = K_o + \beta \cdot V_o[n-1] \tag{1.11}$$

where $K_o = A_{\rm cm} \cdot [V_B \cdot (1 - \beta) - K_b]$.

Similar to the derivation of (1.10), $V_o[n]$ can be expressed as

$$V_o[n] = V_o[\infty] + \beta^n \cdot (V_o[0] - V_o[\infty]) \tag{1.12}$$

where $V_o[\infty] = A_{\rm cm} \cdot (V_B - K_b/(1-\beta)) = K_o/(1-\beta)$. Using (1.9) for $V_b[\infty]$, the steady–state value or the final value of $V_o[n]$, denoted by $V_o[\infty]$, is given by

$$\begin{aligned} V_o[\infty] &= \lim_{n \to \infty} V_o[n] = A_{\rm cm} \cdot (V_B - V_b[\infty]) \\ &= \frac{V_{\rm cmref} + \left[\left(1 + \frac{C_{p1}}{C_1}\right) \cdot (V_B - V_{\rm bias})\right]}{1 + \left(\frac{1}{A_{\rm cm}}\right) \cdot \left(1 + \frac{C_{p1}}{C_1}\right)}. \end{aligned} \tag{1.13}$$

Thus, from (1.9) and (1.13)

$$\begin{aligned} &V_o[\infty] - V_b[\infty] \\ &= \frac{(V_{\rm cmref} - V_{\rm bias}) \cdot \left(1 + \frac{1}{A_{\rm cm}}\right) + \frac{C_{p1}}{C_1} \cdot (V_B - V_{\rm bias}) - \frac{C_{p1} \cdot V_{\rm bias}}{A_{\rm cm} \cdot C_1}}{1 + \left(\frac{1}{A_{\rm cm}}\right) \cdot \left(1 + \frac{C_{p1}}{C_1}\right)}. \end{aligned} \tag{1.14}$$

If $A_{\rm cm}$ is very large, (1.14) can be approximated as

$$V_o[\infty] - V_b[\infty] \approx (V_{\rm cmref} - V_{\rm bias}) + \left(\frac{C_{p1}}{C_1}\right) \cdot (V_B - V_{\rm bias}). \tag{1.15}$$

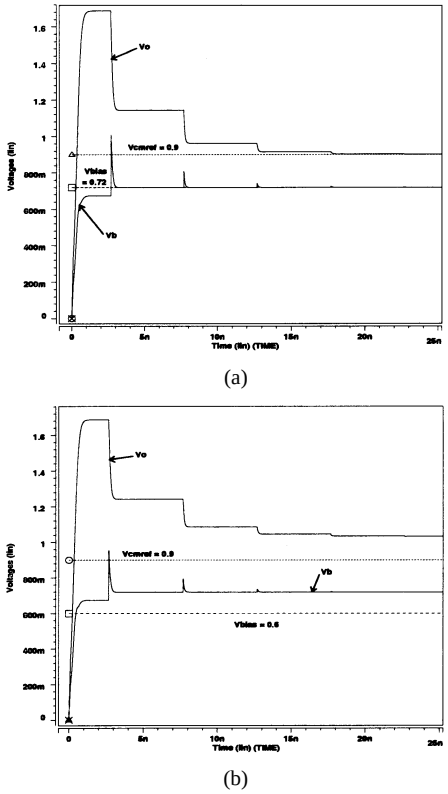
Practically, it is very difficult to estimate V_B accurately because of its dependence on the exact drain current, drain-source voltage, threshold voltage, etc. Thus, any mismatch between the external bias voltage $V_{\rm bias}$ and the input CM of the CM amplifier V_B, is scaled by a factor of C_{p1}/C_1. So this factor should be reduced as much as possible in order to achieve an accurate output CM.

The SC-CMFB circuit model shown in Fig. 3(a) was implemented in HSPICE with a folded cascode amplifier. An ideal switch model with a low on-resistance was developed to implement switches without the charge injection effects. The capacitor values chosen for this implementation are $C_1 = 1.5$ pF, $C_2 = 0.5$ pF and $C_{p1} = 0.15$ pF. The dc gain of the amplifier is 46.7 dB. As shown in Fig. 4(a), when $V_{\rm cmref} = 0.9$ V, $V_{\rm bias} = 0.72$ V and $V_B = 0.724$ V, V_o settles to the desired CM value of 0.9 V, identical to that computed from (1.13). When $V_{\rm bias}$ is changed to 0.6 V, V_o settles to a value of 1.031 V in Fig. 4(b). This confirms the validity of (1.13).

The value of V_b calculated from (1.9) is 0.719 V, which is also verified from the simulations in Fig. 4. Note that in both the cases, the value of V_b remains almost constant, equal to 0.719 V, irrespective of the $V_{\rm bias}$ voltage value. This proves the validity of the model shown in Fig. 3(a) where V_b was defined by the bias currents in transistor M_{n1+}, M_{n1-} in the feedback loop and was assumed to be independent of $V_{\rm bias}$.

IV. Analysis With Charge Injection and Leakage

The same assumptions as stated in Section III hold for the analysis in this section, except that the leakage current and charge injection will not be ignored. Let us consider switches S_1 and S_2 as shown in Fig. 3(a) with charge injection and leakage currents associated with the reverse-biased source and drain junctions of the MOSFETs used in their implementation. As shown in Fig. 3(a), the current source I_{J2} models the



(a) (b)

Fig. 4. Simulation plots of the output CM voltage V_o with (a) $V_{\rm cmref} = 0.9$, $V_{\rm bias} = 0.72, V_b = 0.724, C_{p1}/C_1 = 0.1, A_{\rm cm}$ =46.7 dB and (b) $V_{\rm cmref} = 0.9, V_{\rm bias} = 0.6, V_b = 0.724, C_{p1}/C_1 = 0.1, A_{\rm cm}$ =46.7 dB.

leakage currents of the source/drain-bulk junctions of transistors used in switch S_2 at node V_b and I_{J1} models the sum of the leakage currents of the source/drain-bulk junctions of transistors used in S_1 and S_2 at node V_2. Let $\Delta q_1 = \text{charge}$ injected on node V_2 when switch S_1 opens; $\Delta q_2 = \text{total charge}$ injected/absorbed on nodes V_2 and V_b when switch S_2 opens; $\Delta q_{2,vb} = \text{the fraction of the total charge } \Delta q_2$ injected on node V_b when S_2 opens.

From the time instant $t = (n-1)T$ when switch S_2 opens till the time instant $t = (n-1/2)T$ when switch S_1 opens, the charge balance equation at node V_b can be written as

$$\begin{aligned} &C_2 \cdot \left(V_b\left[n-\frac{1}{2}\right] - V_o[n-\frac{1}{2}]\right) + C_{p2} \cdot V_b\left[n-\frac{1}{2}\right] \\ =&C_2 \cdot (V_b[n-1] - V_o[n-1]) + C_{p2} \cdot V_b[n-1] \\ &+ \Delta q_{2,vb} - I_{J2} \cdot \frac{T}{2}. \end{aligned} \tag{1.16}$$

Similarly, (1.3) can be modified as

$$\begin{aligned} &C_1 \cdot (V_{\rm bias} - V_{\rm cmref}) + C_{p1} \cdot V_{\rm bias} \\ &+ C_2 \cdot \left(V_b\left[n-\frac{1}{2}\right] - V_o\left[n-\frac{1}{2}\right]\right) \\ &+ C_{p2} \cdot \left(V_b\left[n-\frac{1}{2}\right]\right) + \Delta q_1 - \Delta q_2 - (I_{J1}+I_{J2}) \cdot \frac{T}{2} \\ &= (C_{p1}+C_{p2}) \cdot V_b[n] + (C_1+C_2) \cdot (V_b[n] - V_o[n]). \end{aligned} \tag{1.17}$$

Using (1.16) and (1.17) and the steps similar to those described in Section III, an equation for $V_b[n]$ similar to (1.7), can be derived as

$$V_b[n] = K_b' + \beta \cdot V_b[n-1] \tag{1.18}$$

where

$$K_b' = K_b + \left(\frac{\Delta q_1 + \Delta q_{2,vb} - \Delta q_2 - (I_{J1} + 2 \cdot I_{J2}) \cdot \frac{T}{2}}{(C_1+C_2) \cdot (A_{\rm cm}+1) + C_{p1} + C_{p2}} \right)$$

and β is same as given in Section III.

The steady–state value of $V_b[n]$ denoted by $V_b[\infty]$ is modified as, shown in (1.19) at the bottom of the page.

Similarly, (1.13) can be modified as shown in (1.20) at the bottom of the next page.

From (1.19) and (1.20), $V_o[\infty] - V_b[\infty]$ can be easily derived. The dc solution for $V_o[\infty - 1/2] - V_b[\infty - 1/2]$ can be derived from (1.6) and (1.17), by first deriving the expressions for $V_o[n-1/2]$, $V_b[n-1/2]$ in terms of $V_o[n] - V_b[n]$ and then using the expression for $V_o[\infty] - V_b[\infty]$. Note that in presence of charge injection and leakage currents, the steady–state value $V_o[\infty - 1/2] - V_b[\infty - 1/2]$ is different from $V_o[\infty] - V_b[\infty]$.

V. Discussion

In this section, certain design issues regarding SC-CMFB circuit are discussed and design guidelines are provided as follows.

A. CM Gain and Loop Bandwidth

The CM gain of the CM loop should be as high as possible for good accuracy. As evident in the expressions for $V_o[\infty]$ and $V_b[\infty]$, the error terms are attenuated by $A_{\rm cm}$. The larger the $A_{\rm cm}$, the closer are the values of $V_o[\infty]$ & $V_b[\infty]$ to $V_{\rm cmref}$ and V_B, respectively, when $V_{\rm bias} \approx V_B$.

Secondly, the CM loop bandwidth should be large enough to suppress the highest frequency CM disturbances. This is necessary because in the event of output CM variations, a slower CM loop may allow the output signal to be saturated or clipped when the output swing is large and there is little voltage headroom. Also, in presence of mismatches or large signal condi-

$$\begin{aligned} V_b[\infty] &= \lim_{n\to\infty} V_b[n] = \frac{K_b'}{1-\beta} \\ &= \frac{V_B + \frac{1}{A_{\rm cm}} \cdot \left[\left(1+\frac{C_{p1}}{C_1}\right) \cdot V_{\rm bias} - V_{\rm cmref} + \frac{(\Delta q_1 + \Delta q_{2,vb} - \Delta q_2)}{C_1} - \frac{[(I_{J1}+2\cdot I_{J2})\cdot T]}{(2\cdot C_1)} \right]}{1 + \left(\frac{1}{A_{\rm cm}}\right) \cdot \left(1+\frac{C_{p1}}{C_1}\right)} \end{aligned} \tag{1.19}$$

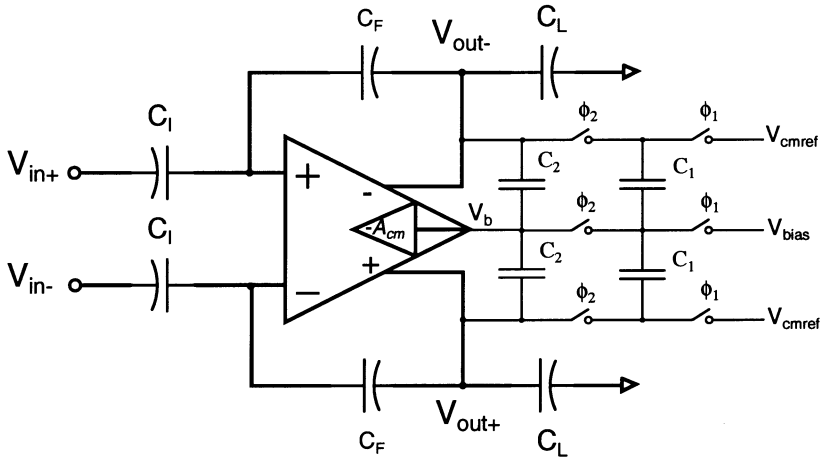


Fig. 5. A Fully-differential opamp in feedback configuration along with a SC-CMFB circuit.

tions (which cause unequal g_m in symmetric circuits), the CM variations can get converted into differential variations and can corrupt the differential signal. So a faster common- mode loop will have less differential signal distortion and faster differential signal settling in the presence of circuit nonidealities [14].

Ideally, one would like to suppress the CM disturbances over the bandwidth of the differential mode (DM) input signal i.e., make the unity-gain frequencies of the differential and the CM loops equal [7], [8], [10], [11]. Some references even advocate a larger CM loop bandwidth than DM loop bandwidth [9], [12], [13]. While desirable, making the CM loop bandwidth greater than or equal to that of the DM loop bandwidth is difficult to achieve in practice because of area, power dissipation and circuit constraints. For example, the circuits in which the CM loop and the differential loop share the same compensation network, the CM loop bandwidth is typically lesser than the differential loop because the CM loop includes more transistors and has additional high-frequency poles. Increasing the CM unity-gain frequency usually results in more area and power consumption. Hence, depending upon the application and circuit constraints, the CM loop bandwidth can be designed such that spurious CM signals are sufficiently suppressed in the band of interest that they do not disturb the differential performance of the op amp circuit.

Thirdly, the CM loop should be well compensated over the desired frequency range. Otherwise, the injection of high-frequency CM signals can cause the CM output to ring or even possibly become unstable. Thus, the CM loop should be properly stabilized to ensure a good phase margin and fast settling. A fully differential opamp in feedback configuration, with SC-CMFB is shown in Fig. 5.

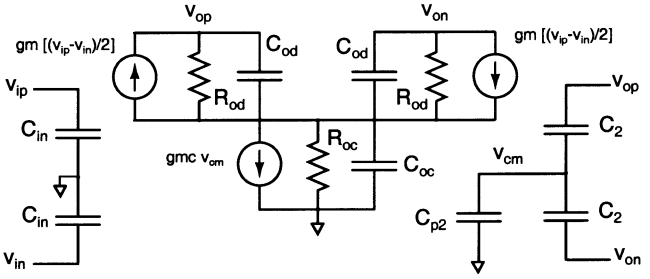


Fig. 6. Opamp model with differential gain and CM gain.

A linear opamp model shown in Fig. 6 is used for computing the DM and CM return ratios.

Similar to the analysis in [3], the differential return ratio *RR*(*DM*) can be calculated as

$$RR(DM) = \frac{(2 \cdot g_m \cdot Z_1 \cdot Z_2)}{\left(Z_1 + \frac{1}{(sC_F)} + Z_2\right)} \tag{1.21}$$

where $Z_1 = 1/(s(C_{in} + C_I))$, $Z_2 = R_{od}||[1/(s(C_{od} + C_T + C_L))]$, $C_T = C_1 + C_2$ during ϕ_2 and $C_T = C_2$ during ϕ_1. Also, the expression for *RR*(*CM*) is

$$RR(CM) = \frac{(g_{mc} \cdot Z_{oc} \cdot Z_3)}{2 \cdot (Z_{oc} + Z_{od} + Z_3) \cdot \left[\frac{C_t}{\left(C_T + \frac{C_{p2}}{2}\right)}\right]}$$

where $Z_{oc} = (2 \cdot R_{oc})||[2/(sC_{oc})]$, $Z_{od} = R_{od}||[1/(sC_{od})]$, $C'_L = C_L + (C_T \cdot (C_{p2}/2)/(C_T + C_{p2}/2))$ and $Z_3 = 1/s\{C'_L + [C_F \cdot (C_I + C_{in})]/(C_F + C_I + C_{in})\}$.

For small enough C_{p2}, as compared to C_T, $C'_L \approx C_L + C_{p2}/2$, Z_3 is almost independent of C_T and *RR* (*CM*) is proportional to $C_T/(C_T + C_{p2}/2)$. Increasing C_T increases *RR*

$$\begin{aligned} V_o[\infty] &= \lim_{n\to\infty} V_o[n] = A_{\rm cm} \cdot (V_B - V_b[\infty]) \\ &= \frac{V_{\rm cmref} + \left[\left(1 + \frac{C_{p1}}{C_1}\right) \cdot (V_B - V_{\rm bias})\right] - \frac{(\Delta q_1 + \Delta q_{2,vb} - \Delta q_2)}{C_1} + \frac{[(I_{J1} + 2 \cdot I_{J2}) \cdot T]}{(2 \cdot C_1)}}{1 + \left(\frac{1}{A_{\rm cm}}\right) \cdot \left(1 + \frac{C_{p1}}{C_1}\right)} \end{aligned} \tag{1.20}$$

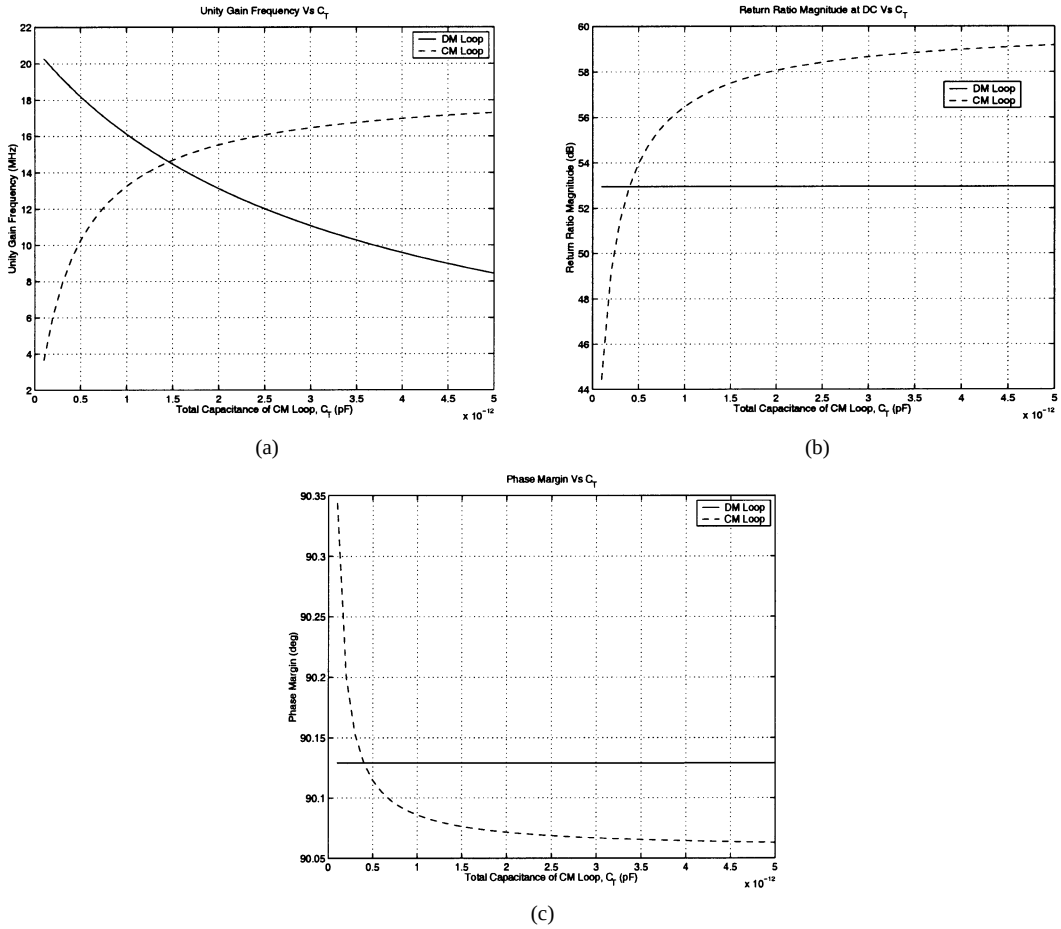


Fig. 7. The DM and the CM return ratio plots for the model in Fig. 6(a) DM and CM loop unity-gain frequencies vs. C_T (b) DM and CM loop dc gains versus C_T (c) DM and CM loop phase-margins versus C_T.

(*CM*). On the other hand, since C_T appears as an additional load to the differential loop, the differential unity gain frequency decreases as C_T increases. If *RR*(*CM*) is a certain known factor k of *RR*(*DM*) bandwidth and all other design parameters are known, then $RR(CM) = k \cdot RR(DM)$ can be solved for the value of C_T. In the example below, k is chosen to be 1 for simplicity. However, depending upon the application and circuit constraints, an appropriate value of k can be chosen. The graph of the differential loop and the CM loop unity-gain frequencies versus C_T is shown in Fig. 7(a). The model parameters shown in Fig. 6 are chosen to be: $g_m = 1$ mS, $C_{\text{in}} = 1.25$ pF, $C_I = 0.5$ pF, $C_F = 0.5$ pF, $C_L = 2$ pF, $R_{od} = 1$ MΩ, $C_{od} = 1$ pF, $g_{mc} = 1$ mS, $C_{p2} = 1$ pF, $C_{oc} = 1$ pF, $R_{oc} = 1$ MΩ. The optimum value of C_T is 1.45 *pF* as shown in Fig. 7(a). Fig. 7(b) shows the *RR* (*DM*) and *RR* (*CM*) dc gains versus C_T and Fig. 7(c) shows the phase margins of *RR* (*DM*) and *RR* (*CM*) as a function of C_T. In practice, SPICE simulations should be used to choose a proper value of C_T such that the CM loop bandwidth is comparable to that of the differential loop.

B. DC Output CM Settling Time

In most modern portable and battery-powered systems, a *power-down mode* (standby mode) is present. When the system is not in active use, the analog and the digital circuitry is shut down, resulting in significant savings in power consumption. Let us consider the circuit shown in Fig. 2, in context with the power-down mode. Since all the clocks are disabled and biasing currents for the amplifier are reduced to zero, the voltage at the high-impedance node V_b is neither properly defined, by the switching circuit nor by the amplifier in a feedback loop. In presence of leakage, the dc voltage values at nodes n_1, n_2, and V_b are not preserved during a long power-down duration. Hence, the dc output CM settling time of the SC-CMFB is crucial for a reliable operation of fully-differential analog circuits during an initial power-on or a transition from the power-down mode into an active mode. The dc output CM settling time of the SC-CMFB circuit is analyzed as follows.

During the clock phase ϕ_2, when C_1 charged to $V_{\text{cmref}} - V_{\text{bias}}$ is connected to C_2, there is a step change in the voltages of nodes V_o and V_b. Using (1.11)

$$\begin{aligned}\Delta V_o[n] &= V_o[n] - V_o[n-1] = K_o - (1-\beta)\cdot V_o[n-1] \\ &= (1-\beta)\cdot (V_o[\infty] - V_o[n-1]. \end{aligned} \tag{1.22}$$

If $C_1 \gg C_2$, then β decreases and the step size increases for the same n. Hence, the SC-CMFB circuit reaches its steady–state faster after startup. The same conclusion can be arrived at, using (1.12) and noting that the error term decreases faster for a smaller β as n increases.

If D is the required normalized dc settling-time error tolerance, then, using (1.12)

$$D > \left(\left|1 - \frac{V_o[n]}{V_o[\infty]}\right|\right) = \beta^n \left|1 - \frac{V_o[0]}{V_o[\infty]}.\right| \tag{1.23}$$

Taking the natural logarithm on both sides and rearranging (1.23), we get

$$n > \frac{\ln\left(\frac{D}{\left|1-\left(\frac{V_o[0]}{V_o[\infty]}\right)\right|}\right)}{\ln\beta} \tag{1.24}$$

since $0 < \beta < 1$.

Thus, the dc output CM settling-time for the SC-CMFB is given by

$$t_s = \left\lceil \frac{\ln\left(\frac{D}{\left|1-\left(\frac{V_o[0]}{V_o[\infty]}\right)\right|}\right)}{\ln\beta} \right\rceil \cdot T \tag{1.25}$$

where $\lceil x \rceil$ = rounding to the nearest integer greater than x and T = Clock period.

If $V_o[0] = 0$, then (1.25) reduces to

$$t_s = \left\lceil \frac{\ln(D)}{\ln\beta} \right\rceil \cdot T. \tag{1.26}$$

Rearranging β given in Section III as

$$\beta = \left(1 + \left\{\frac{C_1 \cdot \left[1 + \left(\frac{1}{A_{\rm cm}}\right)\right] + C_{p1}}{C_2 \cdot \left[1 + \left(\frac{1}{A_{\rm cm}}\right)\right] + C_{p2}}\right\}\right)^{-1}$$

it can be seen that as C_2/C_1 decreases, β decreases and, hence, t_s decreases according to (1.26).

C. Steady–State Values

The steady–state values of V_o and V_b i.e., $V_o[\infty]$ & $V_b[\infty]$ are given by (1.9) and (1.13), in case of no charge injection and leakage currents and by (1.19) and (1.20) when these effects are considered.

As evident from the above stated equations, the expressions for $V_o[\infty]$ and $V_b[\infty]$ are a function of $A_{\rm cm}$, C_{p1}, C_1 and are independent of C_{p2} and C_2. The mismatch between $V_{\rm bias}$ and V_B affects the steady–state value of V_o and is scaled by a factor of $(1 + C_{p1}/C_1)$. For better accuracy of the steady–state values to the desired values, C_{p1} should be minimized as much as possible and C_1, $A_{\rm cm}$ maximized. Note that C_{p3} and C_{p4} in Fig. 3(a) have no effect on the final values of V_o and V_b.

D. Error due to Charge Injection and Leakage

As shown in (1.20), the voltage error due to charge injection of switches is given by

$$\Delta V_{\rm error} = \frac{\left\{\left[(I_{J1} + 2 \cdot I_{J2}) \cdot \frac{T}{(2 \cdot C_1)}\right] - \frac{(\Delta q_1 + \Delta q_{2,vb} - \Delta q_2)}{C_1}\right\}}{1 + \left(\frac{1}{A_{\rm cm}}\right) \cdot \left(1 + \frac{C_{p1}}{C_1}\right)}. \tag{1.27}$$

As shown in Fig. 3(a), when switch S_2 opens at the end of ϕ_2 phase, a fraction of the total channel charge of S_2, i.e., $\Delta q_{2,vb}$, is injected at node V_b. When the switch S_2 closes at the begining of ϕ_2 phase, the sum of charges absorbed from node V_2 and V_bi.e., Δq_2, constitute the total channel charge. Thus, $\Delta q_{2,vb}$ is a fraction of Δq_2 and as per (1.27), it partially cancels the charge Δq_2. *Hence, the voltage error due to charge injection is primarily determined by the charge injection of the switch S_1 and it should be carefully designed.* Since the charge stored in the channel of a transistor is directly proportional to its width, the charge injection error increases with a bigger switch. In order to realize a low-series resistance switch S_1 for proper settling within a clock phase, the use of large width transistors is mandatory. In such a situation, one can either use an nMOS transistor with a half-sized dummy transistor or a parallel implementation of a large switch and a small switch to minimize the charge injection due to switch S_1. In the former technique, the nMOS transistor should turn off before the dummy transistor turns on. Similarly, in the latter technique, the large switch should turn off first before turning off the small switch. Also, as seen from (1.27), leakage current source I_{J1} contributes half as much error as that due to leakage current source I_{J2} since the node V_2 is connected to node V_b only during the ϕ_2 phase in Fig. 3(a). Hence, *the area of drain/source junctions of transistors in switch S_2 should be minimized.*

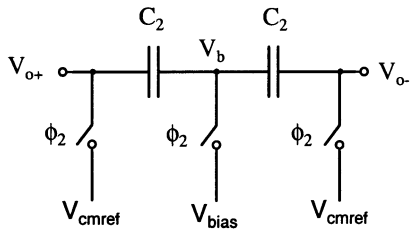


Fig. 8. A SC-CMFB circuit for use with amplifiers having invalid output during a clock phase.

According to (1.20), if the *net* voltage error due to charge injection and leakage currents as per (1.27) is negative, then $V_o[\infty]$ increases as compared to $V_{\rm cmref}$ and if it is positive then $V_o[\infty]$ decreases. Also, if $A_{\rm cm}$ is large, then according to (1.19), $V_b[\infty]$ is unaffected.

The following are the design guidelines presented based on the issues discussed above.

1) Applications With a Reset Phase: When the SC-CMFB circuit as given in Fig. 2 is used for switched-capacitor applications with a reset phase, e.g., Sample and Holds (S/H), clock phase ϕ_1 should be used for amplification/integration and clock phase ϕ_2 for refreshing the voltage on capacitor C_2. Thus, $C_T = C_2$ and as described in Section V-A, the value of C_2 can be determined by making the CM loop bandwidth comparable to that of the differential loop. Choosing C_1 larger than C_2 results in faster dc settling, lower steady–state errors, charge injection errors and leakage errors. However, as C_1 gets larger, switch S_1 must also increase in size, in order to charge the capacitor during ϕ_1 phase. Hence, C_1 must be judiciously chosen keeping the above facts in mind.

For applications with a reset phase, a simpler version of the circuit can be derived from that of Fig. 2 by removing C_1 and directly connecting the bias voltages as shown in Fig. 8.

The circuit consists only of capacitors C_2 and switches controlled by clock phase ϕ_2. However, this circuit cannot be used for opamps with auto-zeroing/offset cancellation phase in S/H or comparator applications where the opamp is connected in a unity-gain configuration during this operation.

2) Applications Without a Reset Phase: When the SC-CMFB circuit is used in applications where the output is valid at all times, the CM loop loads the differential loop differently in each clock phase. The total capacitance of the CM loop seen by the differential loop, is $C_T = C_2$ in clock phase ϕ_1 and $C_T = C_1 + C_2$ in clock phase ϕ_2. Thus, in clock phase ϕ_2, there is a worst case loading of the differential loop by the CM loop. One approach to solve this is to make the value of C_1 much smaller (between one-fourth and one-tenth) than that of C_2 such that $C_T \approx C_2$ in both clock phases [4]. The value of C_2 can be designed using the procedure described in Section V-A. However, as described in Section V-B and Section V-D, the dc settling time and the error due to charge injection and leakage increases significantly. Also, when C_1 is small and C_{p1} is nonnegligible, the mismatch between $V_{\rm bias}$ and the gate–source voltage of transistors M_{n1+}, M_{n1-} i.e., V_B, introduces further error in the steady–state value of V_o as evident from (1.20).

Another approach is to make the loading of the differential loop by the CM loop, such that the loading is equal to C_T, *on an average*. In this procedure, the optimum value of $C_T = C_{T,\rm opt}$ is determined by plotting the graph of differential loop and CM loop unity-gain frequencies versus C_T as described in Section V-A. Let us assume that the value of the parasitic C_{p2} is known. As shown in Fig. 2, during the clock phase ϕ_1, $C_T = C_2$ and the CM loop bandwidth decreases due to higher attenuation. When $C_T = C_1 + C_2$ during the ϕ_2, the CM loop bandwidth increases. If the deviation of the CM loop bandwidth in either case mentioned above, from the case when $C_T = C_{T,\rm opt}$, is p and $\delta = C_{p2}/2 \cdot C_{T,\rm opt}$, then

$$C_1 = \left\{ \frac{[2 \cdot p \cdot \delta \cdot (1+\delta)]}{\delta^2 - p^2} \right\} \cdot C_{T,\rm opt} \tag{1.28}$$

$$C_2 = \left\{ \frac{[\delta \cdot (1-p)]}{\delta + p} \right\} \cdot C_{T,\rm opt}. \tag{1.29}$$

Equations (1.28) and (1.29) are derived in the Appendix . If $\alpha = C_2/C_1$, then using (1.28) and (1.29), a quadratic equation for p can be written as

$$p^2 - (1+\delta) \cdot (1 + 2 \cdot \alpha) \cdot p + \delta = 0. \tag{1.30}$$

Solving it for α at different values of δ, the graph in Fig. 9 can be plotted. Note that since $\alpha > 0$, $p < 1$, and $p < \delta$ for both $\delta, p > 0$, (1.34) is always valid for a finite C_1.

For a sample value of $C_{p2} = 0.4$ pF, $C_{T,\rm opt} = 1$ pF and $C_1/C_2 = 4$, p can be found out to be 11.9% from the graph below.

An improved version of the SC-CMFB circuit that can be used for continuous-time applications, is shown in Fig. 10 below [5]. In the circuit shown in Fig. 10, an extra set of capacitors C_1 and an extra set of switches are used. Switches on the left side of axis of symmetry through V_{o+} and V_{o-} node, operate with opposite clock phase as compared to those on the right side. Thus, during every clock phase, the total loading on the differential loop due to CM loop is $C_T = C_1 + C_2$. According to the procedure described in Section V-A, the value of C_2 can be determined by making the CM loop bandwidth comparable to that of the differential loop. Then C_1 can be designed 5–10 times that of C_2 for faster dc settling, lower steady- state errors, charge injection errors and leakage errors. Thus, a better performance of SC- CMFB can be obtained using the circuit in Fig. 10, for *the same total capacitance loading of the DM loop, at the cost of additional die area.*

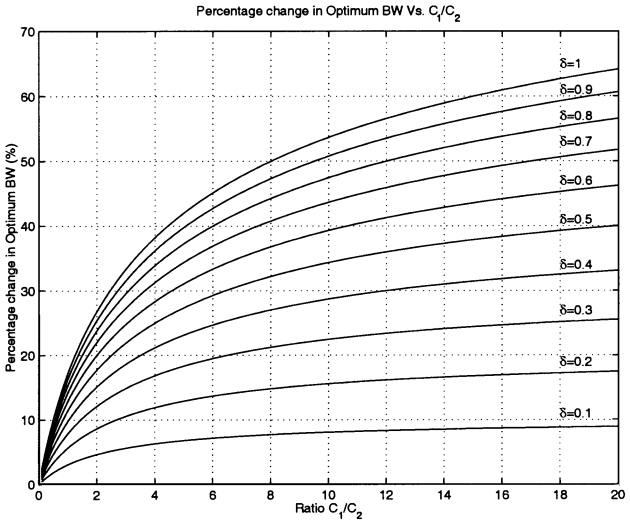


Fig. 9. A plot of percentage deviation in the optimum CM loop bandwidth versus C_1/C_2.

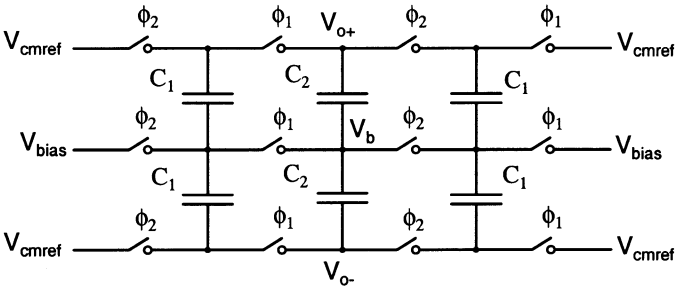


Fig. 10. Alternative SC-CMFB configuration with symmetric loading of the DM loop.

An analysis similar to that presented in Section III can be carried out in a similar fashion under the same assumptions. Let us denote the parameters derived in Section III for the traditional SC-CMFB circuit with a subscript "t" and the parameters for the modified circuit with a subscript "m."

It can be shown that the parameters for the modified circuit are related to the parameters for the traditional circuit according to the following:

$$K_{b,m} = (1+\beta_t) \cdot K_{b,t} \tag{1.31}$$

$$\beta_m = \beta_t^2 \tag{1.32}$$

$$K_{o,m} = (1+\beta_t) \cdot K_{o,t} \tag{1.33}$$

therefore

$$V_{o,m}[\infty] = V_{o,t}[\infty]$$
$$V_{b,m}[\infty] = V_{b,t}[\infty] \tag{1.34}$$

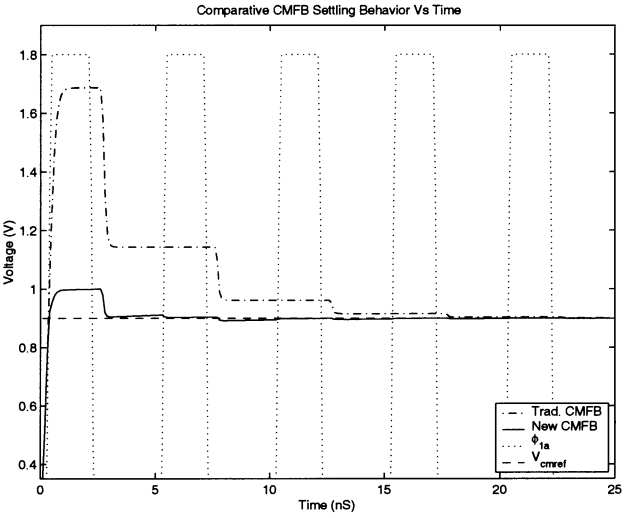


Fig. 11. A comparative plot of the settling behavior of the CMFB circuits shown in Figs. 2 and 10.

when no charge injection and leakage currents are considered. Further, assuming the same initial output voltage for both the circuits, the dc settling time, using (1.25), (1.32), and (1.34), can be written as

$$t_{s,m} = \left\lceil \frac{\ln\left(\frac{D}{\left|1-\left(\frac{V_{o,m}[0]}{V_{o,m}[\infty]}\right)\right|}\right)}{\ln(\beta_m)} \right\rceil \cdot T$$

$$= \left\lceil \frac{\ln\left(\frac{D}{\left|1-\left(\frac{V_{o,t}[0]}{V_{o,t}[\infty]}\right)\right|}\right)}{2\cdot\ln(\beta_t)} \right\rceil \cdot T \approx \frac{t_{s,t}}{2}. \quad (1.35)$$

Thus, the improved SC-CMFB circuit settles much faster than (almost twice as fast as) the traditional circuit. This can be verified from the simulation waveforms shown in Fig. 11.

The step-size for the new circuit is

$$\Delta V_{o,m}[n] = (1-\beta_m)\cdot(V_{o,m}[\infty] - V_{o,m}[n-1])$$
$$= (1-\beta_t^2)\cdot(V_{o,t}[\infty] - V_{o,m}[n-1]). \quad (1.36)$$

Since $\beta_m = \beta_t^2$ and $\beta_t < 1$, the improved SC-CMFB circuit reaches its steady–state faster than the traditional circuit after startup.

Considering the charge injection and leakage current error and assuming no mismatch, equations similar to (1.19) and (1.20) can be written as (1.37), shown at the bottom of the page, where

$$\chi = 1 + 2\cdot\left\{\frac{\left[C_2 + \left(\frac{1}{A_{\rm cm}}\right)\cdot(C_2 + C_{p2})\right]}{\left[C_1 + \left(\frac{1}{A_{\rm cm}}\right)\cdot(C_1 + C_{p1})\right]}\right\}.$$

Similarly, (1.13) can be modified as in (1.38), as shown at the bottom of the page.

Note that in above equations, since χ is greater than 1 for nonzero α, the error due to charge injection is further reduced. Since C_1 can be chosen to be larger than C_2 for the same total capacitance, the above mentioned circuit settles faster and has much lower charge injection errors as compared to the traditional circuit.

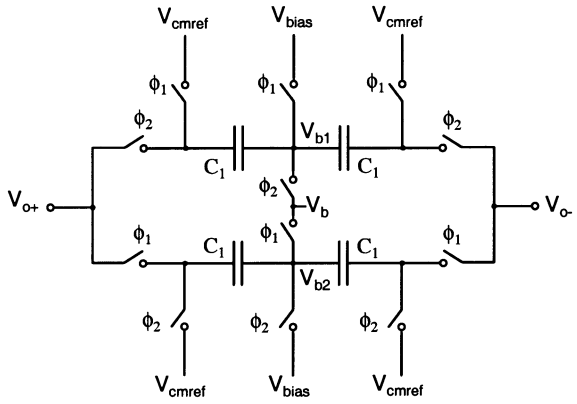


Fig. 12. A SC-CMFB circuit with symmetric loading of the DM loop as in [6].

Another circuit [6], which uses the circuit of Fig. 8 as a building block is shown in Fig. 12. In this circuit, while one pair of capacitors get charged to dc reference values, the other pair provides the CM feedback control. The output nodes are switched to the either pair during opposite nonoverlapping phases. Note that this circuit can also be derived from the circuit shown in Fig. 10 by removing C_2 from Fig. 10. While the circuit in Fig. 12 settles much faster than that in Fig. 10, there are some drawbacks associated with it. During the nonoverlap time between two clock phases, the CM feedback is not present. Hence, there is no CM control during the nonoverlap period. As a result, any high frequency CM noise can cause a drift in the CM value from the desired value.

Also, due to the presence of series resistance of switches connecting V_{o+}, V_{o-} to V_b in the high frequency CM signal path during each clock phase, the CM loop bandwidth is degraded. In Fig. 10, C_2 directly couples the high frequency CM variations to V_b.

$$V_{b,m}[\infty] = \lim_{n\to\infty} V_{b,m}[n] = \frac{K_{b,m}}{1-\beta}$$
$$= \frac{V_B + \frac{1}{A_{\rm cm}}\cdot\left[\left(1+\frac{C_{p1}}{C_1}\right)\cdot V_{\rm bias} - V_{\rm cmref} + \left(\frac{(\Delta q_1 - \Delta q_2)}{C_1\cdot\chi} + \frac{\Delta q_{2,vb}}{C_1}\right) - \frac{(I_{J1}+I_{J2})\cdot T}{C_1}\right]}{1+\left(\frac{1}{A_{\rm cm}}\right)\cdot\left(1+\frac{C_{p1}}{C_1}\right)} \quad (1.37)$$

$$V_{o,m}[\infty] = \lim_{n\to\infty} V_{o,m}[n] = A_{\rm cm}\cdot(V_B - V_{b,m}[\infty]) = \frac{V_{\rm cmref} + \cdot\left[\left(1+\frac{C_{p1}}{C_1}\right)\cdot(V_B - V_{\rm bias})\right] - \left(\frac{(\Delta q_1 - \Delta q_2)}{C_1\cdot\chi} + \frac{\Delta q_{2,vb}}{C_1}\right) - \frac{(I_{J1}-I_{J2})\cdot T}{C_1}}{1+\left(\frac{1}{A_{\rm cm}}\right)\cdot\left(1+\frac{C_{p1}}{C_1}\right)}. \quad (1.38)$$

VI. Conclusion

A detailed analysis of the switched-capacitor CMFB circuit has been presented. A half-circuit equivalent, suitable for mathematical analysis, was developed. The analysis of SC-CMFB circuit, with and without charge injection and leakage, was presented and a closed-form expression of the output CM voltage was derived. Certain issues related to the design of SC-CMFBs such as CM loop gain and bandwidth, dc settling time, steady–state CM voltage values and charge injection and leakage errors were discussed and design guidelines for faster settling and lower charge injection/leakage errors, were presented. A modified SC-CMFB circuit that offers better performance was analyzed.

Appendix

Referring to Fig. 7(a), let $C_T = C_{T,\rm opt}$ be the capacitance where the differential loop and CM loop curves intersect. In the vicinity of $C_{T,\rm opt}$, a *linear variation* of differential loop and CM loop unity-gain frequencies with respect to the variation in C_T can be assumed. Let p be the percentage permissible variation in the differential loop and CM loop unity-gain frequencies. Further, it is assumed that the parasitic C_{p2} is known and let $\delta = C_{p2}/2\cdot C_{T,\rm opt}$. If δ is small, then according to the expression for C_L' in Section V-A, $C_L' = C_L$ and the bandwidth of the CM loop is proportional to $C_T/(C_T + C_{p2}/2)$. If the CM loop bandwidth, when $C_T = C_{T,\rm opt}$ is *BW*, then it is $(1-p)\cdot BW$ when $C_T = C_2$ and $(1+p)\cdot BW$ when $C_T = C_1 + C_2$. Thus

$$1 + \frac{C_{p2}}{(2\cdot C_2)} = \frac{(1+\delta)}{(1-p)} \quad (A.1)$$

$$1 + \frac{C_{p2}}{[2\cdot(C_1+C_2)]} = \frac{(1+\delta)}{(1+p)}. \quad (A.2)$$

Solving (A.1) and (A.2), the expressions for C_1 and C_2 can be derived as

$$C_1 = \left\{\frac{[2\cdot p\cdot\delta\cdot(1+\delta)]}{\delta^2 - p^2}\right\}\cdot C_{T,\rm opt} \quad (A.3)$$

$$C_2 = \left\{\frac{\delta\cdot(1-p)}{\delta+p}\right\}\cdot C_{T,\rm opt}. \quad (A.4)$$

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