Why SPICE Won't Cut it for Analog Anymore

Ken Kundert
Designer's Guide Consulting, Inc.

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This is an opinion piece promoting the use of top-down design and analog HDLs for mixed-signal circuits. It was published in 1999.

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1 Design Productivity

At last year's Design Automation Conference, Ron Collett of Collett International presented findings from a 1997 productivity study in which his firm analyzed 21 chip designs from 14 leading semiconductor firms. The study revealed a productivity gap of 14x between the most and least productive design teams. The study also revealed that developing analog and mixed-signal circuitry requires three to seven times more effort per transistor than designing digital control logic, though this factor was normalized out of the 14x ratio.

I have been able to observe the real-world effects of Collett International's findings through discussions with many customers over the past year. In my experience, the primary culprits behind the poor productivity of those at the bottom of the scale are increasingly complex designs combined with a continued preference for bottom-up (i.e., transistor-level) design methodology and the occurrence of simulation late in the design cycle, which leads to errors and re-spins. There's a huge disparity in productivity between those mixed-signal designers who have transitioned to a "top-down" design methodology and use analog hardware description languages (AHDLs), and those who practice "bottom-up" design and rely solely on SPICE.

SPICE is the analog designer's version of Old Faithful — with the emphasis on "old." Originally designed for simple designs with a handful of transistors, SPICE can't keep up with the demands of today's many-thousand-transistor designs. Companies are going to have to overcome their fears and shift to a top-down design approach if they want to remain competitive. Just working harder isn't enough anymore. The good news is that, with the right combination of methodology and tools, and people trained to use both to optimal benefit, it is possible to consistently produce complex mixed-signal chips, with no re-spins, in three months on average. The secret? Using an analog-optimized HDL along with SPICE to verify the design earlier in the design process.

2 Complexity drives change

SPICE was great when it first came along because it was a lot better than actually soldering together, say, 10 transistors to create an op-amp. You could do a quick simulation and save yourself some time. Today, we're dealing with complicated mixed-signal circuits (e.g., PLLs, over-sampled A/D converters, PRLM disk channels) on the order of tens of thousands of transistors. It's not uncommon to have to simulate through several thousand cycles, just to get the circuit initialized, before you can actually make any measurements. With SPICE, you must basically complete a design all the way to the end before you can generate a transistor-level description. The likelihood that a design is exactly right once you get to that stage is minimal. This means you're verifying the design too late in the design cycle, when it's difficult — and extremely expensive — to make changes.

Analog-optimized HDLs allow the user to quickly write a block-level system model that can be easily simulated to weed out bad architectures and optimize the system's performance early in the design process. This is particularly valuable when it comes to the issue of synthesis. In digital design, you can create a high-level description of your system, verify it, and then simply push a button to get a gate-level equivalent of what you've described at the high level. In analog design, there's no button to push. That syn-

thesis is done by the designer, and it's a very costly step that takes a month or more, with no guarantee that the design is correct. The new AHDLs, working with a SPICE-level simulator (such as Cadence's Spectre circuit simulator), enable mixed-level (i.e., block-level and transistor-level) simulation. At every step, you can verify your moves so that when you actually get to the final design, you're much more confident that it will actually work together as an entire system. This approach can shave weeks, or even months, off the design cycle — helping companies meet their time-to-market window.

3 So, what's the problem?

The typical excuse designers give for not moving away from SPICE is that HDLs are hard to use. This is no longer the case; Verilog-A, in particular, is quite user-friendly. But designers cling to the idea that it is still better to use something they know, even if it is cumbersome and time consuming, than something they don't. To effect a change, companies have to encourage it throughout their entire organizations. They must push their engineers to learn these languages and be supportive of the process, giving them time and training to help speed the learning curve. Universities can take a role by starting to train students in these languages so that they will possess this skill when they enter the marketplace.

The key thing the EDA community can do to help companies make the SPICE-to-HDL transition is to step up efforts in the area of education. The huge response to a series of Verilog-A seminars that Cadence recently conducted is an indicator that we're on the right track in trumpeting the importance of this problem. Also, EDA firms need to continue working closely with the standards bodies (VHDL International, Open Verilog International) to help boost tool interoperability — which can only further the quest to boost customer productivity.

The transition to HDLs for analog design has long been a burning issue for me — from being a key developer behind the Spectre circuit simulator to participating in the Verilog-AMS and VHDL-AMS committees that helped get these languages developed. I've focused a lot of energy on promoting this notion because I feel so strongly about its importance to the industry. Now, a lot of the pieces are starting to fall into place. But the next move is up to the designers; they have to embrace the technology, see the value of it and start to use it. There is huge value here, and designers — not to mention the companies they work for — are going to lose out unless they make the switch.