The Role of High-Speed Serial Interfaces in MS-SoCs

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Describes the role of high-speed serial IO as the driver in the rapid rise in the development of mixed-signal systems on chip.

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1 The Nature of Mixed-Signal Circuits

It is widely understood that mixed-signal design is important at the periphery of electronic systems. Mixed-signal is a combination of digital and analog circuitry. Digital circuitry makes up the core of virtually all electronic systems, while the interfaces to the physical world, such as sensors, actuators, displays, etc. are exclusively analog. The mixed-signal interfaces effectively translate between the analog and digital domains. These interfaces not only allow the electronic systems to interact with the outside world, but are also needed to perform operations within the system that involve physical processes, such as storage and printing. In the past, the digital and mixed-signal circuits were designed by different groups and placed on separate integrated circuits. Generally the digital circuits were larger, more numerous, and higher value, which resulted in them being the primary focus for the industry.

Recently our ability to integrate more and more has suggested that both the digital and mixed-signal circuits would be integrated on the same chip; a mixed-signal system on chip or MS-SOC. This led to the prediction that soon over 80% of all ASICs will contain analog content, up from 20% in 1998. And while that is definitely the trend, high visibility exceptions such as cellular phones abound. Many analog circuits are by their very nature very sensitive and cannot be placed on the same substrate with naturally very noisy digital circuits.

In addition, more and more of the functions previously implemented in analog circuitry are moving to digital because a digital implementation is generally easier to design, allows the use of a cheaper process, is more easily adapted or programmed, and involves less risk. Consider a simple phoneline modem. It was originally implemented mostly in analog. But as the speed limits of a POTS line was reached and the digital transistors just kept getting smaller and faster, most of the functionality of the modem was converted first to digital hardware and then to software. Thus, not only is analog pushed to the periphery, it is pushed to the extremes: high speed, high frequency, high voltage, high current, high impedance, small signals, low noise, etc. When building custom chips, the applications where these extremes are required are the only ones suitable for analog[1]. In other applications, digital always replaces analog eventually.

Given these empirically verifiable facts, how will this astounding growth be achieved?

2 Importance of High-Speed Serial Communications

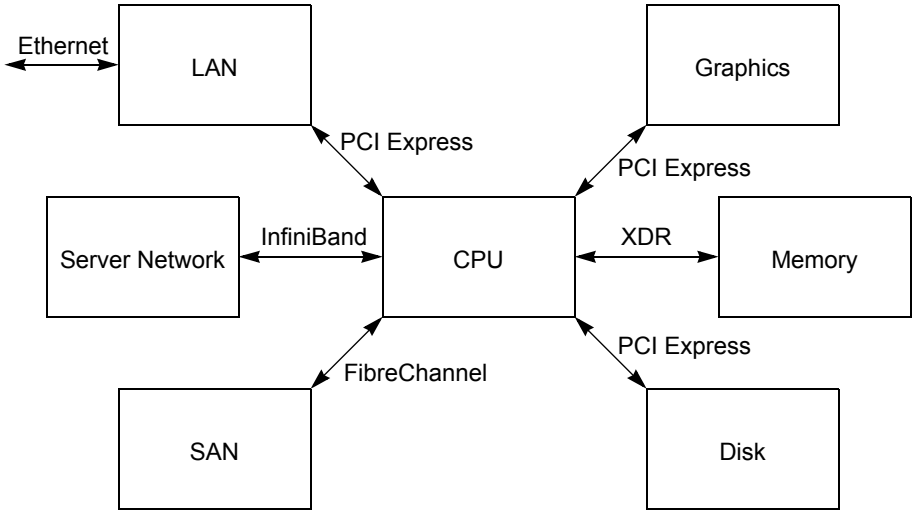
While it is true that mixed-signal circuitry is confined to the periphery of electronic systems, the amount of periphery is growing in an almost fractal-like way. While previously, the mixed-signal content was confined to the periphery of the entire electronics system, it is now proliferating to the periphery of individual chips and is expected to eventually propagate to the periphery of individual blocks within the chip itself. This results because increasing performance requirements for the overall system are requiring that the various parts of the circuit to communicate more quickly. In the past, communication largely occurred over digital parallel busses. Recently, however, designers

1. This explains why IP and synthesis systems targeted towards low performance analog hae nver gained any real traction in the market.

are replacing the parallel busses with high-speed serial links because they are more power and space efficient. For a given data transfer rate, the frequencies present in serial links are much higher than those found in parallel busses, and so require both high-speed analog circuits and design techniques.

To see the impact of these changes, consider the future of a Pentium-class computing system. Since man started making computers the focus has been on improving the speed of computation because it is what limited the overall performance of the computer. However, recently the overall performance has lagged while clock speeds keep racing ahead. The CPU has changed from being computation bound to communication bound. The cost of an arithmetic operation is cheap now; what is expensive is transferring data to and from memory or the I/O system. For example, whereas a Pentium Pro required 70 instruction cycles for a DRAM access, a Pentium 4 running at 2 GHz takes 500 to 600 cycles. In the future, at 5 or 10 GHz, a DRAM access will be several thousand clock cycles. Similar issues plague the I/O subsystems. The result is that the computing industry is in the process of adopting a whole host of high-speed communication links within the computer itself, as shown in Figure 1. PCI Express from Intel, and HyperTransport

FIGURE 1 *High speed communication links in upcoming computing systems.*



from AMD represent high speed replacements to the PCI bus. FibreChannel is a communication link for Storage Area Networks (SAN). InfiniBand is a high speed link for server farms that connects to either the SAN or to other servers. Each of these is expected to eventually operate from 4-10 GHz. In addition, another very high bandwidth link that is capable of passing more than 60GB/s is needed between the CPU and main memory. These links are expected to be either point-to-point links or switched fabrics, and could be implemented as either electrical or optical connections. Electrical will be initially preferred for chip-to-chip communication and optical for box-to-box communication[2]. Eventually, the optical link could reach directly to the chip and the electrical links could infiltrate, and be completely encapsulated within, the chips themselves,

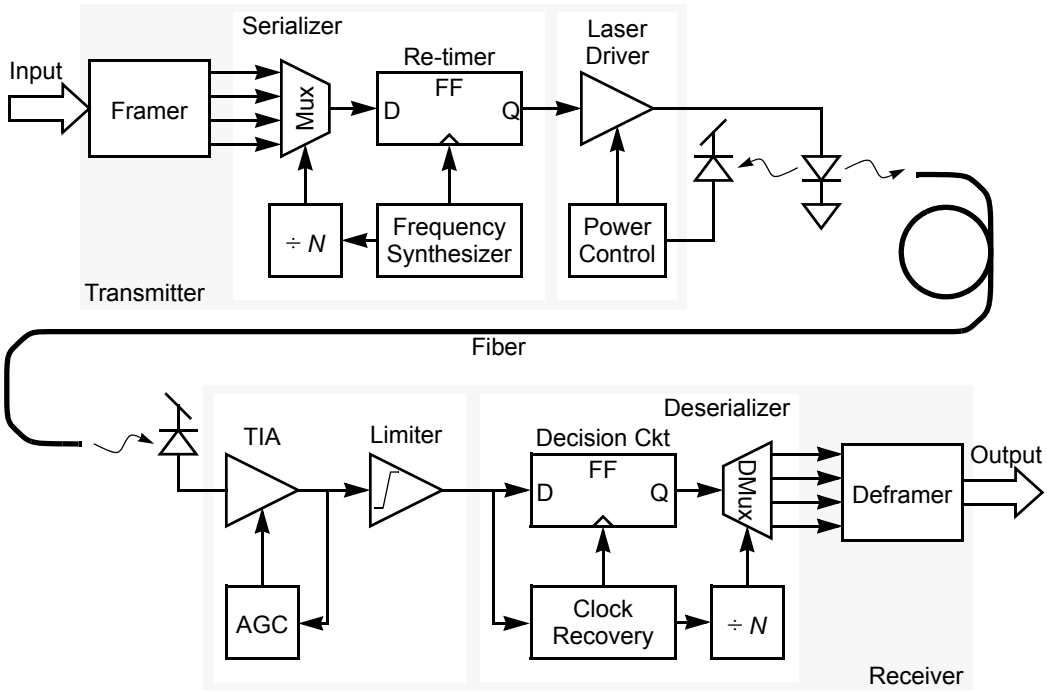
2. Optical links are preferred for high-speed box-to-box communication because fiber has less loss and has fewer interference problems than cables (EMI generation and susceptibility, ground loops, etc.).

where they would be used to provide high-speed communication between the various blocks of the chip. Because of the frequencies involved, each of these links will involve a substantial amount of mixed-signal circuitry. As a result, virtually every chip within a computer will have a significant mixed-signal content. As an example of this trend, consider the new Stratix-II from Altera. It is a high density programmable logic device, which were once purely digital devices, but this one includes dozens of channels of 1 Gbs signaling for chip-to-chip communications.

3 Overview of a Serial Communication System

The block diagram of a optical transceiver is shown in Figure 2. An electrical transceiver would be similarly constructed, except the laser driver, laser, fiber, photo detector, and trans-impedance amplifier would be replaced by a line driver, transmission line, and a line receiver.

FIGURE 2 *Optical transceiver system.*



In the transmitter, a number of channels are multiplexed into a high-speed serial data stream by the serializer. The result is re-timed and applied to the laser driver, which either drives the laser diode itself, as in the figure, or an optical modulator that would follow an unmodulated laser diode. Signal levels at the output of the laser driver range from 5-7 V into 50 Ω. A frequency synthesizer generates clocks for both the multiplexer and the re-timing flip-flop. Also, since the output power varies with temperature and aging, a monitor photo diode and power control circuit continuously adjusts the output level of the driver.

In the receiver, a photo diode converts the optical signal to a current and a trans-impedance amplifier and a limiter raise the signal swing to logic levels. Automatic gain control (AGC) is used to accommodate a wide range of signal levels (in some systems an optical amplifier precedes the photo diode). A clock recovery circuit extracts the clock from the data with proper edge alignment and re-times the data using a flip-flop as a decision circuit. The result is demultiplexed into the original channels. The circuitry that extracts the clock and the data from the input serial data stream and demultiplexes it into the output parallel data steam is referred to as the deserializer.

An OC-192 or OC-768 optical transceiver implementation is typically partitioned into several chips and modules. A single large CMOS chip contains the framer and deframer. The serializer and deserializer are combined onto one chip that is generally referred to as the serdes. Because of the high speeds involved, it is often implemented in a more exotic technology, such as SiGe or InP. Use of GaAs to implement the serdes appears to be declining, but CMOS looks promising and may well be the eventual winner. For lower data rate systems, the framer and the serdes would be combined on the same die. The laser driver is generally a separate die because of the high power levels involved. The transimpedance amplifier is also placed on a separate die to prevent the serdes from interfering with the small signals at its input.

With the coming OC-768 systems, the data rate of the optical signal is 40 Gb/s. The interface between the framer and the serdes includes 16 lines, each running at 2.5 Gb/s. Each of the 2.5 GHz data streams represents a chip-to-chip high speed serial link as specified by the SFI-5 standard, and so each involves a system that is the electrical equivalent to the one shown in Figure 2. Thus, the framer, at 500 kgates, is a large high-speed mixed-signal design.

Complete integration of an optical transceiver in silicon is not currently possible because the bandgap of silicon prevents efficient emission and detection of light at the wavelengths needed for optical communication. However, the alternative of using an electrical link for very high-speed chip-to-chip communication is undesirable because of the high power requirements and the need for expensive low-loss board materials. As a result, the need for a very high bandwidth connection between the CPU and main memory may drive the development of technologies that allow optical-friendly materials, such as InP, to be deposited on silicon to support implementation of optical emitters and detectors. The remaining optical components, such as waveguides, filters, prisms, etc. can already be implemented in silicon, and so a complete WDM optical communication system could be implemented to provide and extremely high bandwidth direct chip-to-chip optical link.

4 Summary

Serial communications design is an incredibly vital area. A very large number of designers are engaged designing serial communication links because there is a large number of communication standards that must be supported[3], the standards are con-

3. Important serial communication standards include USB 2.0, Firewire (IEEE 1394), Infiniband, Fibre Channel, 1 & 10 Gbs Ethernet (over copper and fiber), *x*DSL, DOCSIS cable modems, OC-48, OC-192, OC-768, SFI-4, SFI-5, HyperTransport, PCI Express, RapidIO, StarFabric, HomePNA, etc.

stantly being updated to support higher communication speeds, and because the area has proven to lucrative and is rapidly growing and so many competitors are vying for the market. Serial communications is naturally partitioned between optical and electrical communication. Optical is used for both the higher data rates and the longer haul communications. However, until you get very close to the emitters and detectors, both optical and electrical serial communications are quite similar.

In addition to the increasingly important role that mixed-signal design plays in computing, it plays and even more fundamental role in both wireless communication and networking. Mixed-signal communication systems are playing, or will soon play, a critical role in every high-value market currently being served by the electronics industry.

5 Glossary

3GIO Third-generation I/O based on the PCI software model. Currently known as PCI Express, previously known as Arapahoe.

AHDL Analog hardware description language (such as SpectreHDL or Verilog-A).

AMS Analog and mixed-signal. Refers to generically to the simulator and environment that supports the new Verilog-AMS and VHDL-AMS languages.

APD Advanced package designer (also known as APE). A product from Cadence for designing large and complex routed packages built on Allegro.

BER Bit-error rate.

BGA Ball-grid array. Large routed packages that support upwards of 500-1000 pins.

BJT Bipolar junction transistor.

CDR Clock and data recovery.

EM Electromagnetic.

FibreChannel
Fibre Channel, a highly-reliable, interconnect technology over copper or fiber that allows concurrent communications among workstations, mainframes, servers, data storage systems, and other peripherals and scales from 133 Mb/s to up to 4 Gb/s. It provides interconnect systems for multiple topologies (point-to-point, switched fabric, or arbitrated loop) that can scale to a total system bandwidth on the order of a terabit per second. Switches, hubs, storage systems, storage devices, and adapters are among the products that are on the market today.

HyperTransport
HyperTransport is used to interconnect chips on PC motherboards. At speeds of up to 12.8GB/s it is nearly 50 times faster than the PCI bus, although it is not an actual replacement for it. Instead, it will be used as a backbone technology, connecting processors to memory and I/O. AMD's HyperTransport is said to complement Intel's InfiniBand technology, which offers high-speed connections to external devices. HyperTransport is a full-duplex parallel bus that consists of from 2 to 32 lines for both the transmit and receive directions

that operate from 400 Mb/s to 1.6 Gb/s and uses low-voltage differential signaling (LVDS). (www.hypertransport.org)

Infiniband InfiniBand is a new common I/O specification to deliver a channel based, switched fabric designed to replace legacy I/O like PCI and PCI-X. It decouples the I/O subsystem from memory by utilizing channel-based point-to-point connections rather than a shared bus, load and store configuration. Infiniband utilizes a 2.5 Gb/s/wire speed connection with one, four or twelve wire link widths. This offers scalable performance through multi-link connections as well as a host of interoperable link speeds. The specification supports both copper and fiber implementations. (www.infinibandta.org)

LVDS Low voltage differential signaling.

NRZ Non return to zero. A signaling approach that sends two symbols per cycle, double the rate of conventional level-based signaling.

OC-192 10Gb/s serial optical communication standard for long-distance links.

OC-768 40Gb/s serial optical communication standard for long-distance links.

PCI Express
Third-generation I/O based on the PCI software model. Previously known as 3GIO and Arapahoe. PCI Express architecture is a high-speed, general-purpose serial I/O interconnect that scales to data rates up to 10 Gb/s/line/direction (the expected limit of copper) and supports multiple widths (1, 2, 4, 8, 12, 16 or 32 lines).

RapidIO The RapidIO architecture is a packet-switched data communication standard for interconnecting chips on a circuit board and circuit boards using a backplane. It is designed for embedded systems, primarily for the networking and communications markets. The initial RapidIO specification defines the physical layer technology suitable communications across standard printed circuit board technology at throughputs exceeding 10 Gb/s utilizing low voltage differential signaling (LVDS). (www.rapidio.org)

ROM Reduced-order model.

serdes Serializer/Deserializer. The portion of a Sonet system that converts low-rate parallel data into high-rate serial data in the transmitter and high-rate serial data to low-rate parallel data in the receiver (see SFI).

SONET/SDH
SONET and SDH are a set of related standards for synchronous data transmission over fiber optic networks. SONET is short for Synchronous Optical NETwork and SDH is an acronym for Synchronous Digital Hierarchy. The SONET standards are named OC-*XX,* where OC stands for optical communication, and *XX* is a number that denotes the data rate. OC-48 provides 2.5Gbs, OC-192 provides 10Gbs, and OC-768 provides 40Gbs.

SFI Serdes-Framer interface. A high-speed parallel interface that is used for communication between the framer and the serdes in a Sonet system. SFI-4 is used for OC-192 systems, it consists of two 16-bit busses, one for transmit and one for receive, each operating at 622 Mb/s/line. SFI-5, used with OC-768, is similar except each line operates at 2.5 Gb/s. (www.oiforum.com)

TIA	Trans-impedance amplifier. Amplifier that sits immediately after the photo diode in an optical receiver.
μW	Microwave.
VCO	Voltage-controlled oscillator.
XDR	New high-speed memory interface from Rambus.