# Comparison of the New VBIC and Conventional Gummel–Poon Bipolar Transistor Models

Xiaochong Cao, J. McMacken, K. Stiles, P. Layman, Juin J. Liou, Adelmo Ortiz-Conde, *Senior Member, IEEE*, and S. Moinian

Abstract—A new bipolar transistor model called VBIC has recently been developed and is likely to replace the Gummel–Poon model as the new industry standard bipolar transistor model. This paper focuses on the comparison of the VBIC and Gummel–Poon models under the dc operations. The extraction and optimization procedure coded in S+ statistical language and required for VBIC simulation is also developed and presented.

*Index Terms*—Author, please supply index terms. E-mail keywords@ieee.org for info.

# I. INTRODUCTION

■ HE BIPOLAR junction transistor (BJT) is one of the most widely used semiconductor devices in manufacturing integrated circuits and electronic components. Because of its superior speed performance, such a device has found wide applications in high-speed switching and digital electronics systems. The SPICE Gummel-Poon (SGP) model [1] has been the industry standard bipolar transistor model for more than 20 yrs. Users of the SGP model, however, have found it to be inadequate in representing many of the physical effects important in modern bipolar transistors. Recently, a group of representatives from the integrated circuit and computer-aided design industries have collaborated and developed a new industry standard bipolar model called the vertical bipolar inter-company model (VBIC) [2]. In addition to having an accurate model, it is imperative to be able to extract and optimize the parameters associated with such a model.

This paper seeks to compare the new VBIC and conventional SGP models under the dc operations. An accurate and efficient methodology to extract and optimize the dc parameters for the VBIC model is also developed. First, the SGP and VBIC models will be briefly reviewed. This will be followed by the discussion of the VBIC parameter extraction method. Finally, results calculated from the VBIC model using the parameters extracted from the present method, calculated from the SGP model, and obtained from measurements will be compared. It should be pointed out, due to the large number of VBIC parameters, that

Manuscript received December 18, 1999. This work was supported in part by a research grant funded by the Enterprise Florida (Account 16-22-975). The review of this paper was arranged by Editor T. Nakamura.

X. Cao and J. J. Liou are with the Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL 32816 USA (e-mail: jli@ece.engr.ucf.edu).

J. McMacken, K. Stiles and P. Layman are with the Modeling and Simulation Group, Lucent Technologies, Orlando, FL 32816 USA.

A. Ortiz-Conde is with the Departamento de Electrónica, Universidad Simón Bolívar, Caracas 1080-A, Venezuela.

S. Moinian is with the AT&T Bell Laboratories, Reading, PA 19605 USA. Publisher Item Identifier S 0018-9383(00)00698-5.



Fig. 1. Equivalent circuit for the new VBIC bipolar transistor model.

the parameters extracted and optimized in this paper are those associated with dc and room temperature operations. Extraction of parameters associated with ac, low/high temperatures, and self-heating is a topic of ongoing research and will be reported elsewhere in the future.

## II. REVIEW OF VBIC MODEL

Before discussing the VBIC model, we give a brief review of the SGP model. It is a three-terminal model (i.e., emitter, base, and collector terminals) and consists of three current sources  $I_{cc}$ ,  $I_{bc}$ , and  $I_{be}$ , two capacitances associated with the charges  $Q_{bc}$  and  $Q_{be}$  stored between the base and collector terminals and between the base and emitter terminals, respectively, and four series resistances, two associated with the base region and one each associated with the base and collector regions. The basic of all variants of the SGP model is the integral charge control model for the dc current  $I_{cc}$  passing through the emitter and collector terminals [1].

Fig. 1 shows the equivalent circuit of the new VBIC model. Unlike the conventional SGP model, which has three terminals, the VBIC is a four-terminal model comprising the base, emitter, collector, and substrate denoted by the letters b, e, c, and s, respectively, and the currents flowing into these terminals are  $I_b$ ,  $I_e$ ,  $I_c$ , and  $I_s$ . The other nodes in the VBIC are the extrinsic base bx, parasitic base bp, intrinsic base bi, intrinsic emitter ei, intrinsic collector ci, and extrinsic collector cx.

The VBIC model includes several features that make it distinct from the SGP model [2]. For example, the effect of parasitic substrate PNP transistor is included by a simplified SGP model (represented in Fig. 1 by the SGP equivalent circuit connected to the substrate terminal with components denoted by a subscript p). Another feature included is that the quasisaturation behavior is modeled with the elements  $R_{CI}$ ,  $Q_{bcx}$ , and a modified  $Q_{bc}$  [3]. Self-heating and excess-phase effects have also been accounted for in the VBIC model as separate options.

# III. VBIC PARAMETER EXTRACTION AND OPTIMIZATION

The VBIC parameter extraction and optimization method developed in this paper is coded in S+ statistical language [4] and is based on the experimental data measured from bipolar transistors fabricated at Lucent Technologies. Our extraction and optimization procedure follows in general the approach of Seitchik *et al.* [5].

The following is a brief description of the development of our S+ program for the VBIC parameters extraction and optimization. All the measurements data are stored in only one S+ object denominated "data," which contains several components with the names of base-emitter capacitance (CBE), base-collector capacitance (CBC), "substrate-collector capacitance (CSC), forward Gummel (FG), reverse Gummel (RG), forward output current-voltage (I-V) (FO), and reverse output I-V (RO). All the VBIC model parameters are put into a numerical vector denominated "para." A logical vector called "extract" is also used to define the parameters to be optimized; in this vector, values with "true" statement are to optimized and those with "false" statement are to be kept constant. A function "weight" could be used to minimize the effects of the experimental data that fall outside of the norm of typical data. Based on the model parameters extracted and optimized (i.e., stored in "para"), a function "evaluate" is used to generate the VBIC simulation results. A VBIC Fortran program, which is available in the public domain [6], is needed to interface with "evaluate" to carry out the simulation. A function "residual" compares and differentiates the simulated and experimental data. A function "optimize" is then used to optimize the parameters with "residual" values larger than those deemed acceptable. This function "optimize" is executed in conjunction with the nonlinear regression function "nlregb" available in S+.

The extraction and optimization of the VBIC parameters involves many steps. The order of these steps is important, as a nonoptimal sequence will result in less accurate parameters being extracted. In each step, a different "extract" (i.e., to define the parameters to be extracted and optimized) and "residual" (i.e., to define the measured data to be used for comparison) will be utilized. The steps for extracting and optimizing the VBIC parameters are given in sequence below.

#### A. Junction Parameters

The parameters associated with the emitter-base and base-collector space-charge regions are first extracted. From  $C_{be}$  versus  $V_{be}$  data, in reverse bias and low forward bias regions, extract  $C_{JE}$ ,  $P_E$ , and  $M_E$ . From  $C_{bc}$  versus  $V_{bc}$  data, in reverse bias and low forward bias regions, extract  $C_{JC}$ ,

 $C_{JEP}$ ,  $P_C$ , and  $M_C$ . From  $C_{sc}$  versus  $V_{sc}$  data, in reverse bias and low forward bias regions, extract  $C_{JCP}$ ,  $P_S$ , and  $M_S$ . Optimize the above parameters.

#### B. Early Effect Parameters

The next step is to extract the parameters associated with the early effect. The junction parameters extracted in the previous section can be used to calculate the forward and reverse early voltages ( $V_{EF}$  and  $V_{ER}$ ) using the following equations [7]:

$$(Q_{j,bc}^f - c_{j,bc}^f I_c^f / g_o^f) / V_{EF} + Q_{j,bc}^f / V_{ER} = -1 \qquad (1)$$

$$(Q_{j,be}^r - c_{j,be}^r I_e^r / g_o^r) / V_{ER} + Q_{j,bc}^r / V_{EF} = -1.$$
(2)

Here, superscripts f and r denote forward and reverse modes, respectively,  $Q_j$  is the charge in the junction, which can be calculated from the junction parameters,  $c_j$  is the derivative of  $Q_j$ , and  $g_o$  is the output conductance, which can be determined from the forward and reverse data. Because this early effect model was developed under low injection condition, it is necessary to extract the early effect parameters using data measured at relatively low bias conditions.

#### C. Low-Voltage Parameters

The linear region (i.e., low-voltage region) in the Gummel plot, which is not influenced by the series resistances and high-voltage effects, provides useful information for extracting the model parameters associated with the current transport in bipolar transistors. The approach of extracting low-voltage parameters is the same as that used in the SGP model parameter extraction. However, since the VBIC model incorporates several improved features, more parameters need to be determined, and the extraction procedure is more complicated.

From the forward Gummel plot, extract the following parameters:  $I_s$ ,  $N_F$ ,  $I_{BEI}$ ,  $N_{EI}$ ,  $I_{BEN}$ , and  $N_{EN}$ . From the reverse Gummel plot, extract the following parameters:  $I_s$ ,  $N_R$ ,  $I_{BCI}$ ,  $N_{CI}$ ,  $I_{BCN}$ ,  $N_{CN}$ ,  $I_{SP}$ ,  $W_{SP}$ ,  $N_{SF}$ ,  $I_{BEIP}$ , and  $I_{BENP}$ . Note that the parameters extracted include the parasitic PNP transistor current components. This is because, in the reverse Gummel plot, the base-collector junction is forward biased, and the parasitic transistor is conducting. Optimize these parameters. The voltage range of this extraction is normally between 0.4 and 0.8 V. It should be emphasized that this set of parameters is relatively easy to extract and requires minimal optimization due to the fact that they are isolated from the effects associated with the high current region.

## D. Knee Current Parameters

The knee currents are the currents at which the I-V data starts to deviate from its linear relationship. These parameters ( $I_{KF}$ and  $I_{KR}$ ) can be estimated from the forward beta (i.e., forward current gain) versus  $I_c$  and reverse beta (i.e., reverse current gain) versus  $I_e$ 



Fig. 2. (a) Forward and (b) reverse Gummel plots obtained from measurements and from VBIC model using the parameters extracted from both the low- and high-voltage regions.

plots by taking the current where the beta value is dropped to half of its peak value. Since  $I_{KF}$  and  $I_{KR}$  are influenced by the high-voltage effects, their values need to be optimized later when other parameters are extracted.

## E. High-Voltage Parameters

High-voltage effects in bipolar transistor make the parameter extraction difficult. They include voltage drops on series resistances, parasitic currents and resistances, high-level injection, quasisaturation, and avalanche breakdown. Since these ef-

Fig. 3. (a) Forward and (b) reverse current-voltage characteristics obtained from measurements and from VBIC model using all parameters except for those associated with the quasineutral region avalanche breakdown.

fects are interacting with each other, one subset of parameters cannot be extracted independently from the others. A better way to do this is to extract and optimize a subset of parameters using other subsets of parameters which are not yet optimized. This process is then repeated until all the parameters associated with the high-voltage region are optimized.

1) Forward Gummel Plot: In the forward Gummel plot at high voltages, extract the series resistances  $R_{BX}$ ,  $R_{BI}$ , and  $R_E$ . Next, these series resistances, together with the knee currents extracted previously, are optimized.

З

2



Fig. 4. (a) Forward and (b) reverse current gain versus current obtained from measurements and from VBIC model using the parameters.

2) Quasisaturation and Saturation: The parameters associated with the quasisaturation effect can be extracted from the forward current-voltage (forward I-V) characteristics under quasisaturation and saturation operations. They include the series resistances  $R_{CX}$  and  $R_{CI}$ , and quasisaturation parameters  $V_O$ ,  $G_{AMM}$ , and  $H_{RCF}$ . In addition, since the base-collector junction is forward biased and the parasitic PNP transistor is conducting, the parasitic current components extracted previously, together with the parameters extracted here, need to be optimized.



Fig. 5. (a) Forward and (b) reverse output conductance obtained from measurements and from VBIC model using the parameters.

3) Reverse Gummel Plot: In the reverse Gummel plot at high voltages, extract the parasitic resistance  $R_{BP}$  and  $R_S$ , and optimize all the former parameters.

Using all the parameters extracted and optimized so far, we have compared in Fig. 2(a) and (b) and 3(a) and (b) the calculated and measured Gummel plots and current-voltage characteristics under forward and reverse operations, respectively. In general, the fitting is quite good. In Fig. 3(a) and (b), however, the model becomes less accurate as the current level is increased, particularly for the reverse operation, where the effects of impact ionization become significant. This is because



Fig. 6. (a) Gummel plot, (b) *I–V* characteristics, and (c) current gain of the BJT under forward operation obtained from the SGP model, VBIC model, and measurements.

the parameters associated with avalanche breakdown have not been extracted and included in the VBIC model. This problem will be addressed and removed in the next step.

4) Weak Avalanche Breakdown: Next, based on the I-V characteristics in avalanche breakdown region, we carry out the extraction and optimization of the parameters  $A_{VC1}$  and  $A_{VC2}$  associated with forward weak avalanche breakdown and parameters  $A_{VE1}$  and  $A_{VE2}$  associated with the reverse weak avalanche breakdown.

# F. Global Parameter Optimization

Finally, all the above dc parameters are optimized to obtained the best fitting for the current gain and output conductance. Fig. 4(a) and (b) and Fig 5(a) and (b) illustrate the forward and reverse current gains and forward and reverse output conductances, respectively, obtained from the VBIC model playback and measurements. The predictions from the VBIC model using the parameters extracted compare favorably with measurements.

#### IV. COMPARISON WITH THE GUMMEL-POON MODEL

To illustrate the advantage of the VBIC model over its Gummel–Poon counterpart, we compare the dc characteristics of another bipolar transistor (i.e., different from the ones used in the previous section) obtained from VBIC model, SGP model, and measurements. Because the self-heating effect is not accounted for in the present VBIC model (i.e., the self-heating option is not considered), a device with relatively large size



Fig. 7. (a) Gummel plot, (b) *I–V* characteristics, and (c) current gain of the BJT under reverse operation obtained from the SGP model, VBIC model, and measurements.

is used. Fig. 6(a)–(c) and Fig. 7(a)–(c) show the forward and reverse characteristics of the BJT, respectively, calculated from the SGP model with the SGP parameters extracted from the conventional method, calculated from the VBIC model with the VBIC parameters extracted from the present method, and obtained from measurements. The results indicate that the SGP model is less accurate when the BJT is operating at relatively high current level and/or is operating at reverse operation. Again, because the self-heating does not play an important role, the observed improved accuracy of the VBIC model came

solely from the advanced features included in the main VBIC model (see Fig. 1). For small-size bipolar devices, the VBIC model is expected to be even more accurate than the SGP due to the availability of the self-heating option in the VBIC model.

# V. CONCLUSIONS

The VBIC model developed recently is likely to replace the SGP model as the industry standard for SPICE circuit simulation of bipolar transistor-based integrated circuits. As a result, there is a great interest in the quality of the new VBIC model. To this end, this paper presented the comparison of the new VBIC and conventional SGP models under the dc operations. The procedure and steps for the extraction and optimization of VBIC model parameters were developed, and improved accuracy of the VBIC model over the SGP model was clearly illustrated. The information is important to the engineers and researchers who recognize the importance of an accurate model and intend to use VBIC model for bipolar circuit design and simulation in the future.

#### REFERENCES

- [1] I. Getreu, Modeling the Bipolar Transistor. New York: Elsevier, 1978.
- [2] C. C. McAndrew *et al.*, "VBIC95, the vertical bipolar inter-company model," *IEEE J. Solid-State Circuits*, vol. 31, 1996.
- [3] G. M. Kull *et al.*, "A united circuit model for bipolar transistors including quasi-saturation effects," *IEEE Trans. Electron Devices*, vol. ED-32, p. 1103, 1985.
- [4] J. M. Chambers, Programing with Data—Guide to the S language. Berlin, Germany: Springer, 1998.
- [5] J. A. Seitchik *et al.*, "The determination of SPICE Gummel-Poon parameters by a merged optimization-extraction techniques," in *Proc. BCTM*, 1989.
- [6] . [Online] www-sm.rz.fht-esslingen.de/institute/iafgp/neu/VBIC/rel\_1\_ 1\_5/vbic.htm
- [7] C. C. McAndrew and L. W. Nagel, "SPICE early modeling," in *Proc.* BCTM, 1994, pp. 144–147.

Xiaochong Cao received the B.S. degree in biomedical engineering and instruments from Shanghai Jiao Tong University, Shanghai, China, in 1994, and the M.S.E.E. degree in microelectronics from University of Central Florida, Orlando, in 1998.

He then joined Avanti Corporation, Fremont, CA, as a Device Engineer in AvanLab, and now works in the TCAD development group as a Software Engineer, Silicon Business Unit, Avanti Corporation. His interests include statistical modeling, circuit performance response versus process control parameters, compact model parameter extraction, as well as relevant CAD tool development.

J. McMacken, photograph and biography not available at the time of publication.

K. Stiles, photograph and biography not available at the time of publication.

P. Layman, photograph and biography not available at the time of publication.

Juin J. Liou received the B.S. (honors), M.S., and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1982, 1983, and 1987, respectively.

In 1986, he joined the Department of Electrical and Computer Engineering, University of Central Florida (UCF), Orlando, where he is now a Professor and Graduate Coordinator. In the summers of 1992, 1993, and 1994, he worked at the Solid State Laboratory, Wright-Patterson Air Force Base, OH, as a Summer Research Faculty sponsored by the Air Force Office of Scientific Research. During his sabbatical leave in the Fall of 1997, he held the position of Visiting Senior Fellow in the Electrical Engineering Department, National University of Singapore, Singapore. His current research interests are semiconductor device physics, modeling, simulation, and reliability. He has published four books: Advanced Semiconductor Device Physics and Modeling (Boston, MA: Artech House, 1994), Principles and Analysis of AlGaAs/GaAs Heterojunction Bipolar Transistors (Boston, MA: Artech House, 1996), Semiconductor Device Analysis and Simulation (New York: Plenum, 1998), and Modeling, Simulation, and Parameter Extraction of MOSFET's (Boston, MA: Kluwer, 1998). In addition, he is currently preparing a book, Semiconductor Device Modeling and Simulation: An Integrated Approach, and has published more than 150 refereed journal articles and more than 100 papers (including 20 invited papers) in international and national conference proceedings.

Dr. Liou serves as an Associate Editor (under the area of VLSI and circuit simulation) for the *Simulation Journal* and Regional Editor (in USA) for *Microelectronics Reliability*. He is the recipient of the Distinguished Researcher Award, College of Engineering, UCF (1992 and 1998); Faculty Outstanding Award, UCF (1993); and Engineer of the Year, IEEE Orlando Section (1992).



Adelmo Ortiz-Conde (SM'91) was born in Caracas, Venezuela, on November 28, 1956. He received the B.S. degree in electronics from the Universidad Simón Bolívar, Caracas, in 1979, and the M.E. and Ph.D. degrees from the University of Florida, Gainesville, in 1982 and 1985, respectively. His doctoral research was in the area of semiconductor device modeling under the guidance of Prof. J. G. Fossum.

From 1979 to 1980, he served as an Instructor in the Department of Electronics, Universidad Simón

Bolivar. In 1985, he joined the Technical Staff of Bell Laboratories, Reading, PA, where he was engaged in the development of high voltage integrated circuits. Since 1987, he has been with the Department of Electronics, Universidad Simón Bolivar, and he was promoted to Full Professor in 1995. During his sabbatical leave in 1993–1994, he was with Florida International University, Miami, from September to December 1993, and the University of Central Florida (UCF), Orlando, from January to August 1994. He also was with UCF from July to December 1998 during a new leave of absence. His present research interest includes the modeling and parameter extraction of semiconductor devices. He has published one textbook, *Analysis and Design of MOSFET's: Modeling, Simulation and Parameter Extraction* (Boston, MA: Kluwer, 1998), and more than 70 international technical papers in specialized journals and conferences.

Dr. Ortiz-Conde is a member of the Editorial Advisory Board of Microelectronic and Reliability and he has served as Reviewer for national and international journals and conferences. He was the Technical Chairperson of the Second IEEE International Caracas Conference on Devices, Circuits and Systems, March 1998, and the General Chairperson of the first edition of this conference in 1995. He is currently Chairperson of steering committee of the third edition of this conference to be held in Cancun, México, in March 2000. He is a member of Eta Kappa Nu, Tau Beta Pi, Phi Kappa Phi, and the Galilean Society.

S. Moinian, photograph and biography not available at the time of publication.