REDUCTION OF FINITE-GAIN EFFECT IN SWITCHED-CAPACITOR FILTERS

Indexing terms: Filters, Switched-capacitor filters

A simple technique for significantly reducing the effect of the finite gain of amplifiers on the performance of switched-capacitor filters is presented. The effectiveness of this technique has been established by extensive simulation studies. This technique has the potential for simplifying amplifier design and extending the frequency range of switched-capacitor filters by trading gain for bandwidth.

Introduction: One of the important factors limiting the performance of MOS switched-capacitor (SC) filters is the finite gain of amplifiers. It has been shown that in SC filters the effect of finite gain is more serious than that of finite bandwidth.[1] In this letter we propose a simple technique to significantly reduce the finite-gain effect. It is based on the fact that in a vast majority of practical SC filters the sampling frequency is made much higher than the signal frequencies of interest in order to make the required continuous-time anti-aliasing and reconstruction filters easily realisable on silicon (an extensive survey of the literature has revealed that a ratio of at least 20:1 is maintained in most cases). Thus there would be considerable correlation between successive signal samples. This is exploited here to reduce the finite-gain effect.

Principle of operation: Fig. 1 shows the schematic diagram of a lossless integrator incorporating the proposed technique.

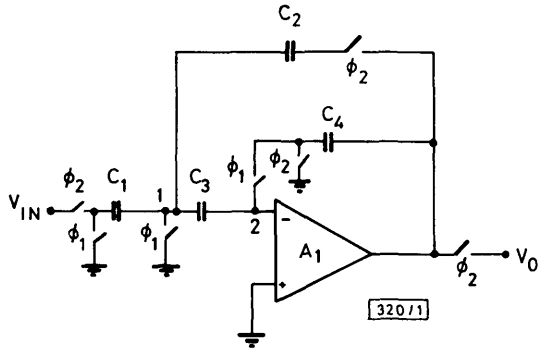

Fig. 1 *Schematic diagram of proposed lossless integrator*

This is a modified version of a well known SC integrator,[2] the difference being that here the output voltage does not change significantly during the offset compensation phase ϕ_1 because the auxillary capacitor C_4 is placed in the feedback path during this phase. Thus the voltage V_2 at node 2, being equal to $-V_0/A$ (where A is the amplifier gain) also retains its previous value. During the phase ϕ_1, V_2 is sampled across the auxillary capacitor C_3, and during the integration phase ϕ_2, C_3 is placed in series with the inverting input of A_1. Owing to the correlation between successive samples of V_2, the magnitude of the error seen at node 1 during the integration is much smaller than the magnitude of V_2 itself, resulting in a significant reduction in the finite-gain effect. On the other hand, in the conventional circuit the correlation properties of V_2 are destroyed because the output of the amplifier is reset to zero during the phase ϕ_1.

Routine analysis shows that the transfer function of this integrator is given by

$$\frac{V_0(Z)}{V_{IN}(Z)} = -\frac{C_1/C_2}{1 - Z^{-1} + \frac{1}{A}\left(1 - \frac{Z^{-1}}{D}\right)\left(1 - Z^{-1} + \frac{C_1}{C_2}\right)} \quad (1)$$

where D is given by

$$D = 1 + \frac{1}{A} + \frac{1}{A}\frac{C_3}{C_4}(1 - Z^{-1}) \quad (2)$$

The term $(1/A)[1 - (Z^{-1}/D)][1 - Z^{-1} + (C_1/C_2)]$ in eqn. 1 represents the finite-gain error.

Since the ratio C_3/C_4 is not tied down by any design constraint, it can be set to 1. Under this assumption it is seen that the value of D would be close to 1 even with relatively low values of A. Thus the finite-gain error term can be approximated as $(1/A)(1 - Z^{-1})[1 - Z^{-1} + (C_1/C_2)]$. The corresponding term for the conventional integrator is equal to $(1/A)[1 - Z^{-1} + (C_1/C_2)]$. Clearly the multiplication factor $(1 - Z^{-1})$ makes the finite-gain error in the modified integrator considerably smaller than that in the conventional one.

If parasitic capacitance is considered in the analysis, the error term gets modified to $(1/A)[1 + (C_{p2}/C_3)](1 - Z^{-1})[1 - Z^{-1} + ((C_1 + C_{p1})/C_2)]$, where C_{p1} and C_{p2} are the parasitics at the nodes 1 and 2 in Fig. 1. Thus the presence of parasitics slightly increases the magnitude of the finite-gain error term. However, the new circuit retains its superiority over the conventional one as the latter is also affected by parasitics when A is finite.

It is clear from the above that this technique is quite general in nature and can easily be applied to complex SC filters simply by augmenting each amplifier by two auxillary capacitors. The values of the auxillary capacitors have very little bearing on the performance of the filter and can thus be made small. The technique automatically provides offset compensation without imposing any excessive slew-rate requirements on the amplifiers because their outputs hardly change during the offset compensation phase. As in conventional offset compensated SC circuits,[1,3] owing to the non-overlapping clocks, the feedback loops of the amplifiers are open during short intervals. This may in some cases result in undesirable slewing of the amplifiers. This problem can be overcome by inserting an 'XY' capacitor network between node 1 and the output terminal of the amplifier in Fig. 1, as suggested in Reference 4. The presence of the 'X' capacitor slightly degrades the performance in the same way, as does the parasitic capacitance at node 1. A similar degradation would occur in the conventional circuits as well.

Simulation results: The effectiveness of the approach has been established by simulating several filters with WATSCAD.[5] Some illustrative results are given below. In all cases realistic values of parasitic capacitances have been inserted at the appropriate nodes. All the auxillary capacitors have been set equal to the smallest capacitor in the filter.

Fig. 2 shows the effect of the finite gain on the Q of a

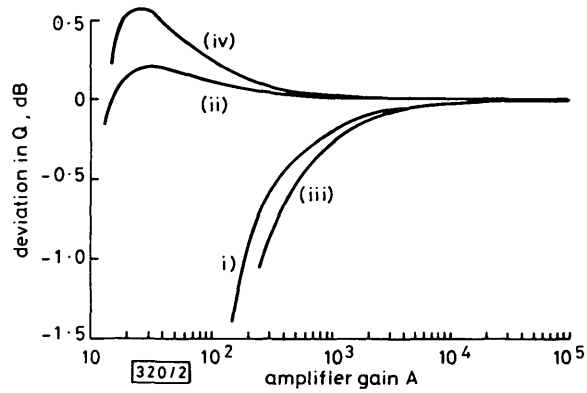

Fig. 2 *Effect of finite gain on Q of state-variable biquads with $f_c/f_0 = 20$*
(i) Conventional biquad, $Q = 5$
(ii) Modified biquad, $Q = 5$
(iii) Conventional biquad, $Q = 10$
(iv) Modified biquad, $Q = 10$

conventional state-variable biquad[3] and its modified counterpart. The superiority of the modified version is clearly evident. Similarly, a reduction has been observed in the effect of the finite gain on the value of the centre frequency f_0 as well.

Fig. 3 shows the finite-gain effect in a state-variable biquad constructed using very low time-constant (VLT) integrators.[6,7] VLT integrators are a special class of integrators which facilitate the realisation of very low-frequency filters using high-frequency clocks. They are seriously affected by the finite-gain effect because they invariably employ signal attenuation to reduce capacitor spread. The VLT biquads whose performances are shown in Fig. 3 have been realised using T-cells with an attenuation factor of 10. It is seen that in order to keep the Q error within 0·2 dB, the conventional VLT biquad requires an op-amp gain of at least 5000 even for a relatively

low value of Q. This requires the use of specially designed op-amps.[7] In contrast, the modified version only requires a gain of 100.

Fig. 4 shows the effect of the finite gain on the response of a

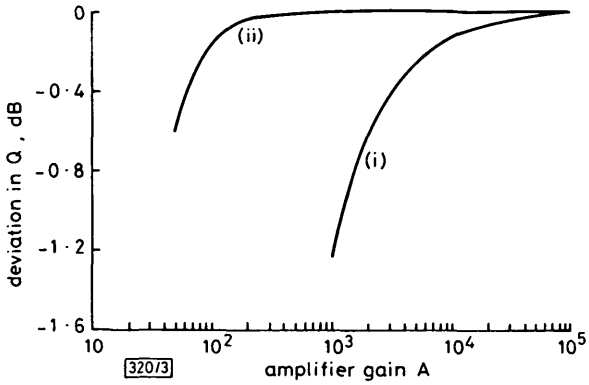

Fig. 3 *Effect of finite gain on Q of VLT biquads with* $f_c/f_0 = 800$ and $Q = 5$

(i) Conventional biquad
(ii) Modified biquad

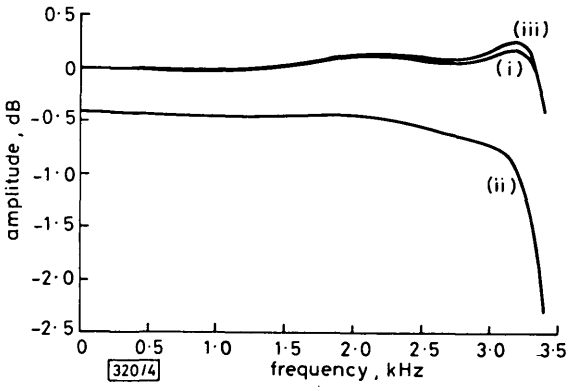

Fig. 4 *Effect of finite gain on response of a fifth-order elliptic ladder filter*

(i) Conventional filter, $A = 5000$
(ii) Conventional filter, $A = 100$
(iii) Modified filter, $A = 100$

fifth-order elliptic ladder filter which is commonly used in PCM systems. The design for this filter has been taken from Reference 8. Here again, the superiority of the modified version is evident.

The above examples show that we have here a simple method to significantly reduce the finite-gain effect in SC filters. This technique has the potential for simplifying amplifier design and extending the frequency range of SC filters by trading gain for bandwidth.

K. NAGARAJ*
K. SINGHAL
T. R. VISWANATHAN
J. VLACH

Faculty of Engineering
University of Waterloo
Waterloo, Ontario, Canada N2L 3G1

* On leave from Indian Telephone Industries

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References

1 MARTIN, K., and SEDRA, A. S.: 'Effects of finite gain and bandwidth on the performance of switched-capacitor filters', *IEEE Trans.*, 1981, **CAS-28**, pp. 822–829
2 LAM, K. K. K., and COPELAND, M. A.: 'Noise cancelling switched-capacitor filtering technique', *Electron. Lett.*, 1983, **19**, pp. 810–811
3 GREGORIAN, R., MARTIN, K. W., and TEMES, G. C.: 'Switched-capacitor circuit design', *Proc. IEEE*, 1983, **71**, pp. 941–966
4 LAKER, K. R., FLEISHER, P. E., and GANESAN, A.: 'Parasitic-insensitive biphase switched-capacitor filters realised with one operational amplifier per pole pair', *Bell Syst. Tech. J.*, 1982, **61**, pp. 685–707
5 VLACH, J., VLACH, M., and SINGHAL, K.: 'WATSCAD user manual' and 'WATSCAD tutorial', University of Waterloo, 1984
6 VAN PETEGHEM, P. M., and SANSEN, W. M. C.: 'T-cell SC integrator synthesises very large capacitance ratios', *Electron. Lett.*, 1983, **19**, pp. 541–543
7 SANSEN, W. M. C., and VAN PETEGHEM, P. M.: 'An area efficient approach to the design of very large time constants in switched-capacitor integrators', *IEEE J. Solid-State Circuits*, 1984, **SC-19**, pp. 772–779
8 LEE, C. F., *et al.*: 'Sensitivity and nonlinear distortion analysis for switched-capacitor circuits using SCAPN', *IEEE Trans.*, 1984, **CAS-31**, pp. 213–220

50 nm LINE FABRICATION IN 0·5 μm PMMA FILM ON SILICON SUBSTRATES WITH A 20 kV e-BEAM

Indexing terms: Semiconductor devices and materials, Electron-beam lithography

With an isopropyl alcohol (IPA) development, 50–100 nm lines are fabricated in 0·5 μm PMMA film on silicon substrates with a 20 kV e-beam. The slope of solubility rate in an IPA development is 10·2 at a high electron dose. A higher contrast and an improved resolution are obtained by using an IPA development.

Introduction: Electron-beam lithography techniques to fabricate fine structures with a dimension ranging from 10 to 100 nm are becoming increasingly important both for basic research on nanometre structure physics and for development of high-speed nanometre devices. In e-beam lithography forward-scattered electrons in the resist and backscattered electrons from the substrate limit the minimum size of patterns. To avoid this difficulty, high-voltage e-beams, thin membrane substrates and thin resists have been used to produce fine patterns.[1–6] However, to fabricate the devices, thick resists and thick substrates are necessary and a low-voltage e-beam is desirable to avoid degradation of the devices.

This letter shows that higher contrast in PMMA has been obtained with a high electron dose and an IPA development, and 50 nm lines have been fabricated in 0·5 μm PMMA resist on thick substrates with a 20 kV e-beam.

Experiments: PMMA (polymethyl methacrylate) was spun on to a silicon wafer to give a 0·5 μm film thickness and prebaked at 160°C for 20 min. The wafers were exposed on an e-beam exposure machine, JEOL JBX-5A. The patterns were written at a density of 16 spots/μm at 20 kV. Line dose exposure ranged from 6·4 to 9·6 × 10^{-9} C/cm at beam currents of 5 to 7·5 × 10^{-11} A. An e-beam spot size at a beam current of 5 × 10^{-11} A was about 20 nm. The exposed resist was developed in IPA and in a 1:3 mixture of MIBK (methyl isobutyl ketone) and IPA at 23°C. Cross-sectional profiles of lines drawn in PMMA were observed with an SEM.

Results and discussion: Fig. 1 shows the sensitivity curves of

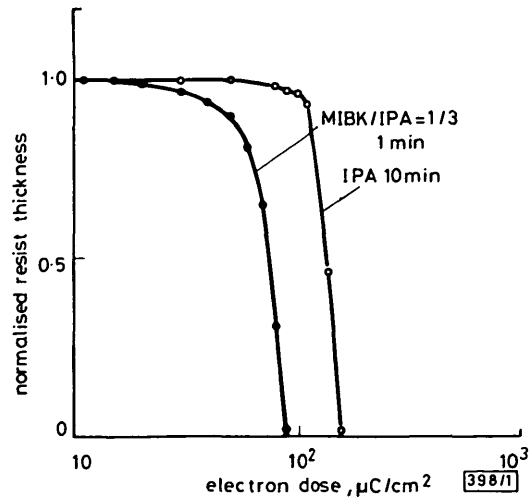

Fig. 1 *Sensitivity curve of 0·5 μm PMMA*