A Low Power 2.4-GHz Current Reuse VCO for Low Power Miniaturized Transceiver System

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***Abstract*— The explosive growth of short range wireless communication systems has lead to highly demand of compact radio frequency (RF) circuit with low power design. As voltage control oscillator (VCO) is the core block of RF systems, this paper presents a low power and highly miniaturized current reuse 2.45 GHz VCO. The proposed VCO is designed with the staking switch two series transistors using current reuse topology and inversion-mode of PMOS varactor tank. The proposed VCO consists a single on chip inductor and four MOS transistors that simplifies the VCO circuit and shrink the chip area remarkably. The proposed VCO is designed with 0.18-µm CMOS process. At 1.2 V DC supply, the proposed VCO draws only 315 µA current resulted to the VCO operate at ultra low power (0.38 mW). Over the tuning range the proposed VCO has the phase noise of -127 dBc/Hz at 1 MHz offset.In order to eliminate additional matching voltage circuit, the tuning voltage (Vtune) is kept similar to the DC voltage supply for 2.45 GHz ISM band applications. The performance of the proposed VCO show the excellent optimization for low power of compact transceiver system.**

Keywords- current reuse topology; CMOS; low power; PMOS varactor; voltage control oscillator (VCO).

I. INTRODUCTION

The short range wireless communications in the area of wireless sensor network, medical implant device and so on are rapidly increasing [1,2]. In this area, the more and more optimized (in terms of low power, low cost, and small size) radio frequency (RF) transceiver system is ever pushing demand. Recently, this demand has been paying much attention in the research work to more optimize the RF transceiver system. Depending on the application, most of the cases the betterment of the power and size is very critical issue in different blocks. Reducing the power of VCO, the key building block of transceiver, here by the main issue.

Designing of VCO is trade-offs among the several vital parameters such as power consumption, phase noise, and chip area [3], [5-7]. In the open literature a lot of VCO was reported where the current reuse and other techniques are used. A low power CMOS current reuse VCO is reported in [4] which consumes 3.96mW DC power including buffer. Using Flip Chip technology results the better spectral purity in [11] but the power consumption still remain 10.8 mW. On the other hand, in order to reduce the power consumption the staking VCO and tripler with current reuse technique is used in [13] and reached the power consumption 9 mW as well as the wide frequency tuning range from 7.06 to 8.33 GHz.

Therefore, the goal of this work is designing a VCO with optimum power consumption, spectral purity, and increasing the simplicity by reducing the number of circuit components for a low power short range miniaturized RF transceiver system.

The remaining part of this paper is organized as Section II presents the VCO topologies. Section III describes the designing technique of our proposed VCO, in order to achieve circuit simplicity, low power, and low phase noise performance. The simulated result is arranged in Section IV. Finally the proposed VCO is summarized in Section V.

II. OSCILLATOR TOPOLOGY

An oscillator can be considered as an interconnection of two single port networks. The one single port network is a frequency selective tank for oscillation and another is negative resistance/active network for compensation of losses associate in tank network (figure 1).

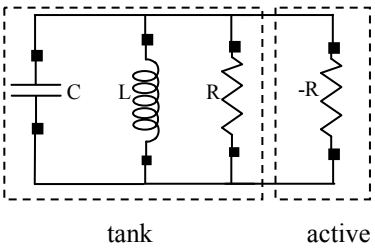

Figure 1. Analogy of LC tank VCO

If the pulse current $i(t)=I_{pulse}\ \delta(t)$ is applied to the tank circuit, the time domain response can be represented by using (1).

$$v_{out}(t) \approx \frac{I_{pulse} e^{\frac{-t}{2RC}}}{C} \left(\sqrt{\left(\frac{1}{LC} - \frac{1}{4R^2C^2} \right)} t \right) \qquad (1)$$

From this equation it is easy to see that the response of the system is sinusoidal and amplitude decay inversely proportional to the tank capacitance. When, $|R| >> \sqrt{(L/C)}$ the frequency of the sinusoidal output can be denoted by using (2). Therefore, to keep continuous oscillation with constant amplitude, energy is added to the tank network by the negative resistance.

$$\omega_{osc} = \sqrt{\frac{1}{LC}} \tag{2}$$

Among the several different topologies for the compensation of tank loss in oscillator, the cross couple differential or $-G_m$ LC VCO topology is the common choice for radio frequency integrated circuit (RFIC) in order to get better spectral purity and frequency stability. The spectral purity/phase noise is very important parameter in oscillator performance that mostly depends upon the quality factor (QF) of the tank circuit that used in oscillator. Hence the perfect designing of tank circuit results the better phase noise performance of VCO. It is vary usual that the C of the LC tank VCO is implemented by the varactor and the part of the C value is varied by the control voltage. The series resistance of varactor has an imperious effect on overall tank quality factor. In this regard, the diode varactor can enable voltage dependent frequency variation but in terms of tank QF, the MOS varactor is better for its lower gate resistance that result superior tank QF.

In the MOS varactor topology the MOS form a parallel plate capacitor with the gate as one plate and connected drain, source and bulk form another plate for the both cases inversion-mode MOS (I-MOS) and accumulation-mode MOS (A-MOS) [3]. The C value of this structure is a nonlinear function of V_{BG}. In the I-MOS, the MOS is operated under the condition $V_{BG} > |V_T|$ and the value of C is maximum when $V_{BG} >> |V_T|$ the maximum value of C of each MOS is nearly $C_{ox}=\varepsilon_{ox}(W \times L)/t_{ox}$. Where ε_{ox} is the dielectric constant of silicon dioxide, W is the gate width, L is the gate length, and t_{ox} is the thickness of oxide.

On the other hand the proper setting of G_m value of switching cross couple NMOS or/and PMOS transistor according to the tank impedance let the circuit oscillate. The modified version of cross couple differential VCO is a current reusing technique that is used in this work. In this system the one half cycle's current is reused in another half cycle in output that reduces the power consumption of VCO to half of typical cross couple differential model. In the next section the current reuse topology has been discussed in details.

III. CURRENT REUSE VCO DESIGN

The conventional differential $-G_m$ LC VCO is the still widely used oscillator in RFIC. Figure 2 shows the topology of the conventional oscillator with varactor tank and both PMOS and NMOS cross coupled pairs as the load (M1 and M2) and driver (M5 and M6) respectively. The same current flows through the load and driving devices and yield negative resistance to compensate the tank lose. The total negative resistance of the cross coupled pairs can be express by using (3).

$$R = -\frac{2}{G_{MN} + G_{MP}} \tag{3}$$

Where the G_{MN} and G_{MP} are the transconductance of NMOS and PMOS transistor respectively.

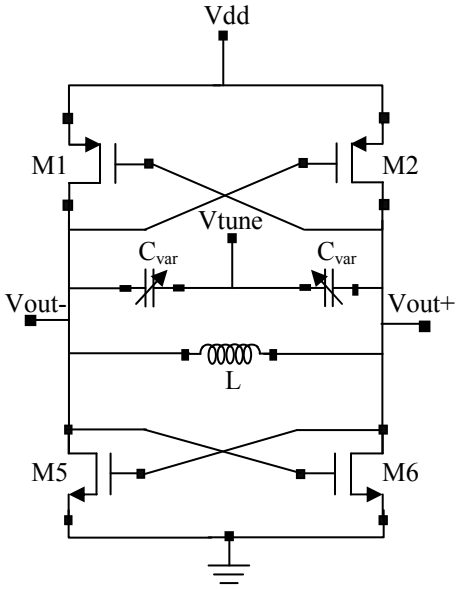

Figure 2. Typical $-G_m$ LC VCO with varactor tank

The proposed current reusing VCO is shown in figure 3. This topology uses NMOS and PMOS switching transistor in series like stacking opposite side of the tank circuit. The MOS switching transistors are cross connected to each other and generate the sufficient negative resistance which also eliminates one of the cross connected MOS pairs from the conventional topology (figure 2). The PMOS and NMOS transistor stack switch model is shown in figure 4. During the positive half cycle of the output, both switch S_1 (PMOS) and S_2 (NMOS) are closed (figure 4a). During this period, current flow through the tank from a DC supply to ground that charge the tank up to the equivalent capacitance of MOS varactor. During the next half cycle, the MOS switches are closed (figure 4b) and tank discharge in this period. Surprisingly, this topology draws the current from DC supply only for one half cycle of its oscillation. For another half cycle it reuses the tank discharge current and continue the output signal. This technique reduces the power consumption of the oscillator to the nearly half of the power consumption of the conventional oscillator with the same VCO specification. Both of the transistors operate at triode region and switch at the same time that allows the smooth voltage swing, controlled by the supply voltage.

In regard of phase noise degradation, the PMOS transistor is always preferable due to having the lower 1/f noise than the NMOS transistor [5]. On the other hand, among the different choice of varactor, PMOS varactor is preferred to be implemented in VCO resonator in order to achieve lower phase

noise [6]. The tank circuit is optimized with 2.4 nH inductor and the PMOS (PM2 and PM3) varactor with MOS size 20 µm in width and 12 µm in length to make sure the oscillation at the frequency around 2.45 GHz and the best spectral purity. The current in the tank circuit is controlled by the PM1 and NM1 staking switch which affect the tank performance and amplitude of the output voltage. The 20/0.18 µm PM1 and 27/0.18 µm NM1 can ensure the optimum current flow from a 1.2 V DC supply.

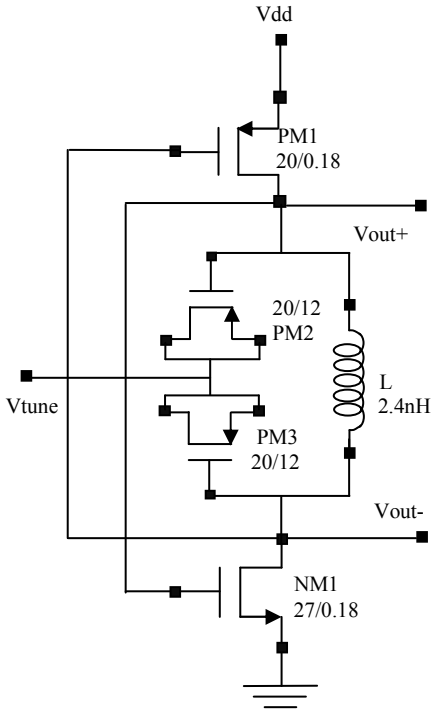

Figure 3. Proposed current reuse VCO with PMOS varactor tank

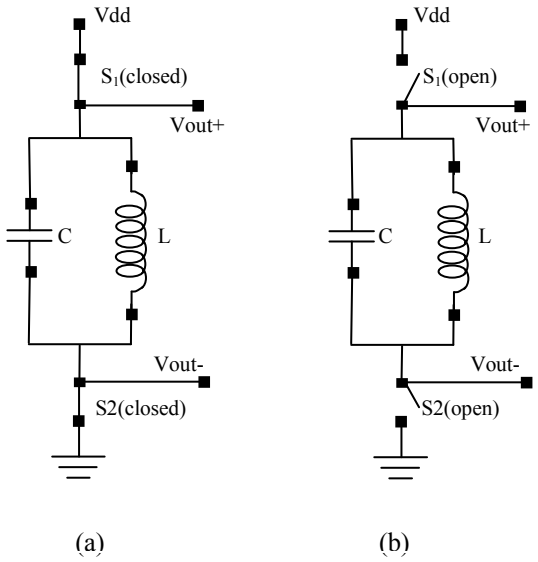

Figure 4. Operation of proposed VCO during (a) positive half, and (b) negative half cycle of output.

IV. RESULT AND DISCUSSION

As shown in figure 3, the proposed VCO is simulated in advance designing system (ADS) with TSMC 0.18 µm technology. The proposed VCO draws only 315µA average current from 1.2 V DC source which result the VCO operate at the power as low as 0.38 mW. This low power consumption makes the VCO quite significant for low power RF systems. The MOS varactor capacitance, over the tuning voltage is shown in figure 5 which slightly changed to upward due to the gate voltage variation when connected in VCO. The used MOS varactor allow to tune the voltage from 0.7 V to 1.5 V that result the frequency tuning from 3 GHz to 2.3 GHz. This tuning has significant influence on startup transient phase of oscillator that could affect the high speed on-off keying (OOK) system. At the tuning voltage 1.2 V the oscillator takes 10 ns time to reach the steady state oscillation. The tank circuit is optimized for the 2.45 GHz ISM band at the tuning voltage 1.2 V as same with the Vdd that exclude the additional tuning circuit at 2.45 GHz operation. Figure 6 shows the design reach the 2.45 GHz at the tuning voltage 1.2 V excellently. The single ended output waveform and the phase noise are shown in figure 7 and figure 8 respectively. The phase noise -127 dBc/Hz at 1 MHz offset proof the design is highly compatible for high speed system. All the simulation results show the well optimized performance of our proposed VCO for low power operation.

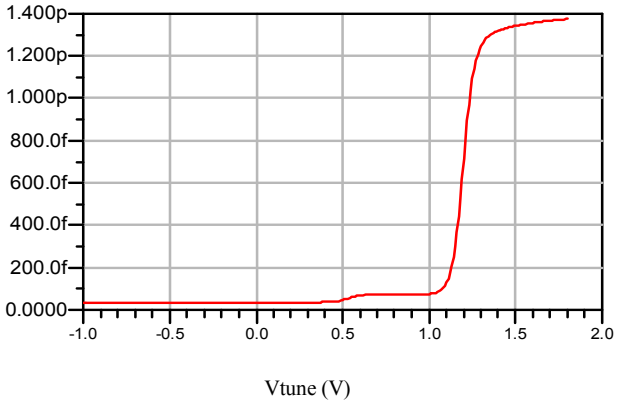

Figure 5. Capacitance variation with V_{tune} of inversion mode PMOS varactor

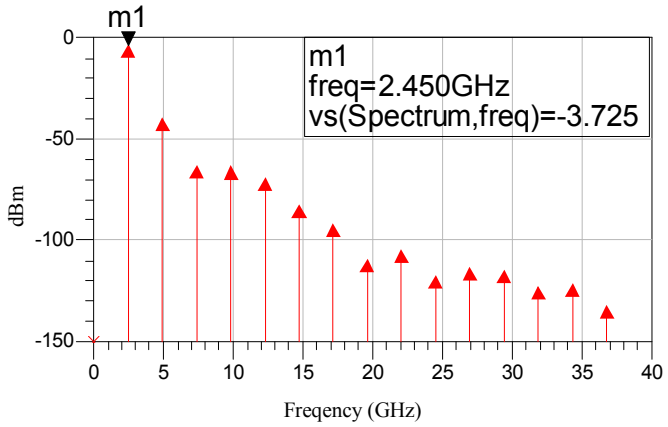

Figure 6. Frequency spectrum at V_{tune}=1.2 V

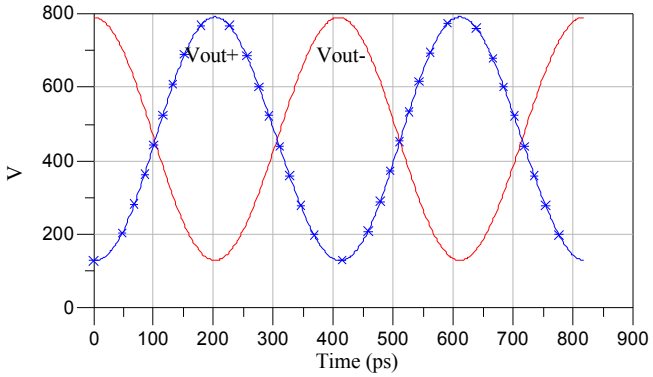

Figure 7. VCO single end output waveform at V_{tune}=1. 2 V

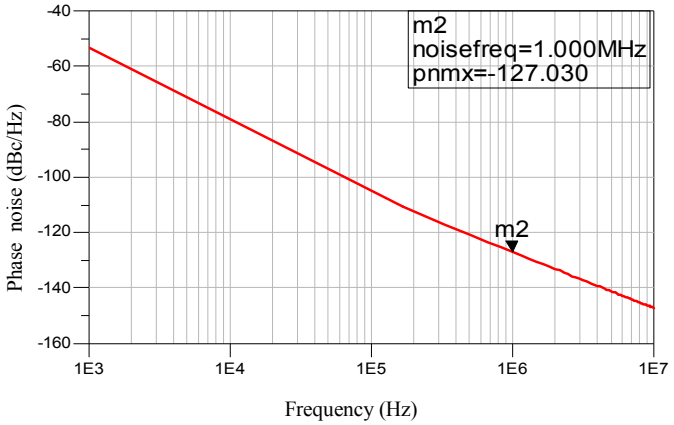

Figure 8. Phase noise of proposed VCO at V_{tune}=1.2 V

The Table 1 also compares the proposed VCO performance with some recently published work. It is clear from the table, our proposed VCO has the comparatively high performance in terms of power consumption, spectral purity and circuit simplicity with the least number of circuit components.

TABLE I
COMPARISON OF PROPOSED VCO PERFORMANCE

Ref.	Tech. (nm)	Freq. (GHz)	Vdd (V)	Power (mW)	PN (dBc/Hz) @ 1M	Comp-onents
[7]	350	5.87	2.4	19.2	-112	10
[8]	250	1.9-2.7	2.5	10	-124	11
[9]	90	5	1.2	2.52	-98.8	8
[10]	180	10.52	1.5	20.4	-122	24
[11]	350	2.45	3	10.7	-111	7
[12]	180	10	0.9	3.15	-114	16
This work	180	2.45	1.2	0.38	-127	5

V. CONCLUSION

A low power, low phase noise, and simplified current reuse VCO for miniaturized 2.45 GHz system is presented in this paper. The power is very precious thing for the low power short rang RF system like wireless sensor network, implant medical device and so on. Our proposed VCO is a good candidate for this kind of system in order to optimized the system power and size. The manipulated stacking switch series transistor of this VCO draws only 315 µA current from 1.2V DC source that result the VCO operate at 0.38 mW power.

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REFERENCES

[1] M. Kraemer, D. Dragomirescu, and R. Plana, "A High Efficiency Differential 60 GHz VCO in a 65 nm CMOS Technology for WSN Applications," *IEEE Microwave and Wireless Components Letters*, vol. 21, pp. 314-316, June 2011.

[2] Fan Xiangning, Zeng Jun, Chen Xiaoguang, "A 4.8 GHz RF CMOS wideband LC VCO for wireless sensor networks RFICs," *International Conference on Wireless Communications & Signal Processing,* pp.1-5, 13-15 Nov. 2009.

[3] R. L. Bunch, and S. Raman, "Large-signal Analysis of MOS Varactors in CMOS -Gm LC VCOs*," IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1325-1332, Aug. 2003.

[4] Ruey-Lue Wang, Hsuan-Der Yen, Wen-Kuan Yeh, Yi-Jiue Shie, "A 1.2V low-power CMOS voltage-controlled oscillator (VCO) using current-reused configuration with balanced resistors for IEEE 802.16e," in *9th International Conference on Solid-State and Integrated-Circuit Technology,* pp.1633-1636, 20-23 Oct. 2008.

[5] K. O. Kenneth, Namkyu Park, Dong-Jun Yang, "l/f Noise of NMOS and PMOS Transistors and their Implications to Design of Voltage Controlled Oscillators," in *IEEE RFIC Symp.*, pp. 59-62, 2002.

[6] J. D. van der Tang, and D. Kasperkovitz, "A Low-Phase-Noise Reference Oscillator with Integrated pMOS Varactors for Digital Satellite Receivers," *IEEE Journal of Solid-State Circuits*, vol. 35, pp.1238-1243, Aug 2000.

[7] Hsin-lung Tu, Tsung-Yu Yang, Hwann-Kaeo Chiou, "Low phase noise VCO design with symmetrical inductor in CMOS 0.35-µm technology," in *Proc. 17th Asia Pacific Microwave Conference*, pp. 4, 4-7 Dec. 2005.

[8] Haiyong Wang, Nanjian Wu, Guoliang Shou, "A novel CMOS low-phase-noise VCO with enlarged tuning range," in *International Conference on Microwave and Millimeter Wave Technology,* pp.570-573, 21-24 April 2008.

[9] R. D. Lorenzo, A. J. G. Arteaga, A. Rueda, and E. Peralias, "A 5GHz Wide Tuning Range LC-VCO in Sub-micrometer CMOS Technology," in *Asia Pacific Conf. on Circuits and Systems*, pp.558-561, Nov. 30-Dec. 3 2008.

[10] S. L. Jang, S. S. Lin, C. W. Chang, and S. H. Hsu, "Quadrature VCO Formed with Two Colpitts VCO Coupled via an LC-Ring Resonator," *Progress In Electromagnetics Research C,* vol. 24, pp. 185-196, 2011.

[11] A. dos Anjos, A. A. Pabon, and W. Van Noije, "2.45GHz Low Phase Noise LC VCO Design Using Flip Chip on Low Cost CMOS Technology" in *2012 IEEE Third Latin American Symposium on Circuits and Systems*, pp.1-4, Feb. 29-Mar. 2 2012.

[12] S. L. Jang, D. A. Tu, C. W. Chang, and M. H. Juang, "A Low Power Push-Push Differential VCO Using Current-Reuse Circuit Design Technique," *Progress In Electromagnetics Research C*, vol. 27, pp. 85-97, 2012.

[13] Pei-Kang Tsai, Tzuen-Hsi Huang, "Integration of Current-Reused VCO and Frequency Tripler for 24-GHz Low-Power Phase-Locked Loop Applications," *IEEE Transactions on Circuits and Systems II: Express Briefs,* , vol.59, pp.199-203, April 2012.