

40 Gbit/s limiting output buffer in 80 nm CMOS

G. Sialm, C. Kromer, T. Morf, F. Ellinger and H. Jäckel

A 40 Gbit/s 1V limiting output buffer for an AC-coupled 50 Ω load with a differential output swing of 660 mV and a gain of 18 dB is presented. A power consumption of only 24 mW and a simulated risetime of 11 ps are achieved by means of a systematic buffer optimisation.

Introduction: The aggressive downscaling of the transistor gate lengths enables the design of CMOS circuits operating at 40 Gbit/s. To route 40 Gbit/s signals from chip to chip in parallel Tbit/s links or in chip to measurement equipment, small and power-efficient 40 Gbit/s buffers are required. Recently published circuits at 40 Gbit/s are a CMOS amplifier [1], a multiplexer and demultiplexer [2] as well as drivers at 30 Gbit/s [3]. However, they suffer from modest output swings, which reduce noise immunity in broadband interconnects. Moreover, the decreasing supply voltages required to prevent oxide breakdown make the development of drivers with a large output swing, V_{out} , challenging. Therefore, the conventional power consumption per data rate (P/B) figure of merit (FOM), is extended by including V_{out} resulting in $V_{out}/(P/B)$. In this Letter, a five-stage differential-pair output buffer for an AC-coupled 50 Ω load in 80 nm CMOS with common-mode feedback (CMFB) is presented. The circuit reaches an FOM of 1100 mV/(mW/Gbit/s). This FOM is more than seven times larger than the highest FOM reported, see Table 1.

Table 1: Driver comparison

FOM [mV/(mW/Gbit/s)]	Technology	Data rate B [Gbit/s]	P [mW]	Differential V_{out} [mV]	Ref.
85.7	150 nm GaAs pHEMT	40	2800	6000	[5]
153.3	130 nm CMOS	12	43.85	560	[6]
120	130 nm CMOS	30	150	600	[3]
1100	80 nm CMOS	40	24	660	This work

Circuit design: The 50 Ω buffer is implemented in IBM's standard CU-08 CMOS process with eight metal layers. The design goal is to demonstrate a 50 Ω driver with a supply voltage of only 1 V and a differential $V_{out} > 500$ mV with an input voltage swing of $V_{in} = 300$ mV at a data rate of 40 Gbit/s and a risetime t_r of about 10 ps, low power consumption and small area.

In the following the design procedure of the driver in Fig. 1 is explained. The transistor width of the main driver is determined by (i) the 50 Ω output matching requirements and (ii) the common-mode voltage V_{CM} requirement for an optimal gain-power consumption ratio (G/P). Owing to the large output capacitance of 190 fF (pad capacitance of 100 fF), the dominant pole is at the output. Using shunt peaking with a 1 dB peak in the frequency response and a total load of 25 Ω the minimum achievable risetime t_r is 7.5 ps.

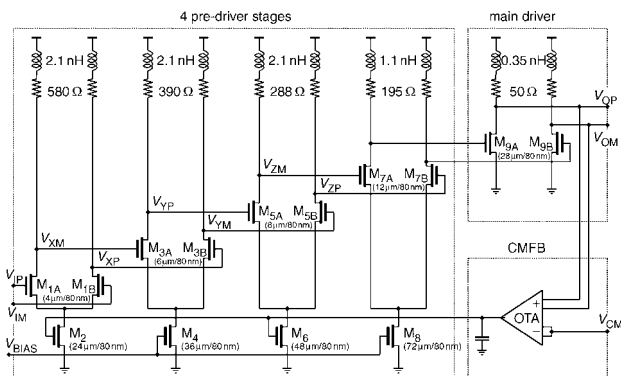


Fig. 1 Circuit schematics of implemented driver

To meet the matching requirements a large transistor is necessary ($w = 28 \mu\text{m}$). Therefore, the main task of the pre-driver is to step down

this large input capacitance without increasing the previous calculated t_r too strongly. Consequently, the number of pre-driver stages is optimised in such a way that for a given total capacitance step down ratio F_{tot} of 7 (ratio between the input capacitances of the main and the pre-driver) a minimal t_r and P result. For this F_{tot} , which is defined by the minimum transistor width, the optimal pre-driver stage number is 4. Because of the large bias resistor the minimum transistor width is restricted by the maximum peaking inductance [4]. The maximum inductance (≤ 2.1 nH) in turn is limited by layout constraints and driver chip area. A driver chip area of only $50 \times 80 \mu\text{m}$ has been achieved. This leads to a transistor width and an input capacitance of the pre-driver of $4 \mu\text{m}$ and 8 fF, respectively.

However, the minimum achievable t_r of a non-limiting five-stage driver with shunt peaking and a 1 dB overall peak in the frequency response is mainly determined by the RC constant of the output stage (dominant pole), yielding a t_r of about 10.5 ps. The reason is that for a five-stage driver a 1.72 times higher bandwidth per stage is required than for the same driver consisting only of a main driver. This factor corresponds roughly to the bandwidth enhancement factor for shunt peaking that yields a maximally flat frequency response [4].

To maintain a t_r of about 10.5 ps independent of process variations the input signal is additionally limited. For a given V_{in} , the maximum t_r improvement due to signal limiting is determined by the total gain of the driver. The total gain is in turn defined by V_{CM} of a stage ($V_{CMmin} = V_{CMout}$) and by the number of stages. As the number of stages is fixed, the minimal t_r and P can be achieved when optimising V_{CM} for a maximum G/P . Systematic simulations have shown that this can be accomplished for $V_{GS} = V_{DS} = 0.5$ V. Together with the saturation voltage of the current sources of 0.1 V the in- and output V_{CM} of a stage are 0.6 V. The simulated t_r reduction due to signal limitation for the 300 mV input signal used in the measurements is 19%. This corresponds to an effective bandwidth improvement of 25%.

The implemented CMFB prevents that small common mode shifts at the driver input result in large common mode shifts at the output, which may clip the signal. The CMFB is realised with an operational transconductance amplifier (OTA). The open-loop feedback gain and the phase margin yield 37 dB and 100 degree worst case, respectively.

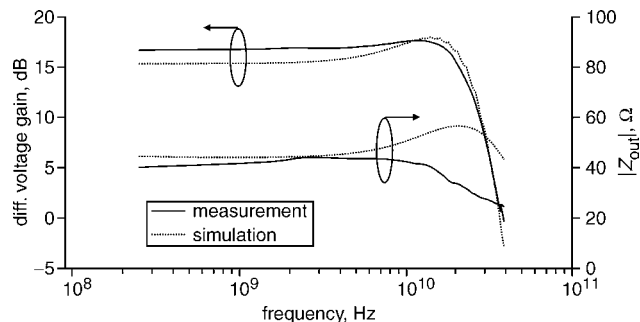


Fig. 2 Measured and simulated differential voltage gain and output impedance

Results: All measurements were performed on wafer and included the pad capacitance. Fig. 2 shows that the small signal driver bandwidth is 24 GHz without limiting. However, with signal limiting and $V_{in} \geq 300$ mV the effective bandwidth is, as explained, 30 GHz (+25%), which is sufficient for an NRZ data rate of 40 Gbit/s. Measured and simulated eye diagrams are reproduced in Fig. 3a; they show clearly open eyes at 40 Gbit/s. The 40 Gbit/s multiplexer used as a source has a differential V_{out} , t_r and rms jitter of 610 mV, 9 ps and 1.2 ps, respectively. The measured differential V_{out} of the 50 Ω driver is 660 mV after correction for cable losses. The measured t_r and rms jitter of the driver, including multiplexer and cabling at 40 Gbit/s, are 17 ps and 1.56 ps, respectively. Modelling the experimentally determined response of the measurement setup yields a total t_r of 18 ps, including the driver, which is in good agreement with the measurements. The simulated t_r of the buffer together with $t_r = 9$ ps of the multiplexer as shown in Fig. 3b results in 11 ps, and thus is close to the initial estimations.

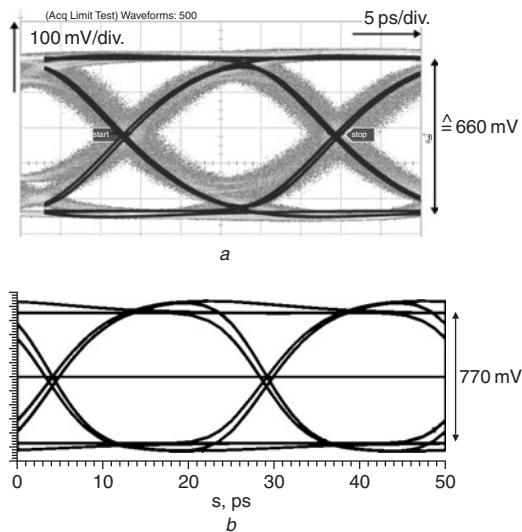


Fig. 3 Eye diagrams at 40 Gbit/s

a Measurement and simulation (black line) of driver including losses and delays of measurement equipment

b Simulation of driver including only multiplexer with 9 ps risetime

Conclusion: We have successfully demonstrated a 40 Gbit/s low power driver with a large differential output swing of 660 mV at only 1 V supply voltage.

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