A Second-Order High-Resolution Incremental A/D Converter with Offset and Charge Injection Compensation

JACQUES ROBERT AND PHILIPPE DEVAL

Abstract—**Sigma-delta modulation, associated with oversampling and noise shaping, is a well-known technique used in high-accuracy A/D converters. Such converters, required in telecommunications applications, are characterized by ac performance such as signal-to-noise ratio. Moreover, they are mainly dedicated to applications which can tolerate offset and gain errors. On the other hand, measurement and instrumentation applications require absolute accuracy, e.g., offset and gain errors cannot be tolerated. These applications are characterized by dc performance such as differential and integral nonlinearities, offset and gain errors, and they often require high resolution. The second-order incremental A/D converter, which makes use of sigma-delta modulation associated with a simple digital filter, is capable of achieving such requirements. Experimental results, obtained of circuits fabricated in a SACMOS 3-μm technology, indicate that 15-bit absolute accuracy is easily achievable, even with a low reference voltage.**

I. Introduction

RECENTLY, a first-order micropower incremental A/D converter was proposed [1], [2]. An absolute accuracy of 16 bits has been obtained, but the conversion time was large, of the order of 1 s for a consumption of 65 μW, restricting the applicability of such a circuit to very slowly varying signals. In this paper, the use of a second-order structure, allowing a considerable reduction of the conversion time, is first discussed. The optimal digital processing of the comparator outputs is derived with a simple temporal method. An offset and charge injection compensation is then presented. Finally, a comparison with sigma-delta converters will be carried out.

II. First- and Second-Order Sigma-Delta Modulator

Fig. 1(a) represents a first-order sigma-delta modulator. The stability of this circuit is ensured because there is only one integrator in the loop. This structure has been used in a first-order incremental A/D converter [1], [2]. Fig. 1(b) represents a conventional second-order sigma-delta modulator. Since there are two integrators in the loop, their outputs can be very large and must be limited [4], which is not acceptable in the design of a second-order incremental A/D converter.

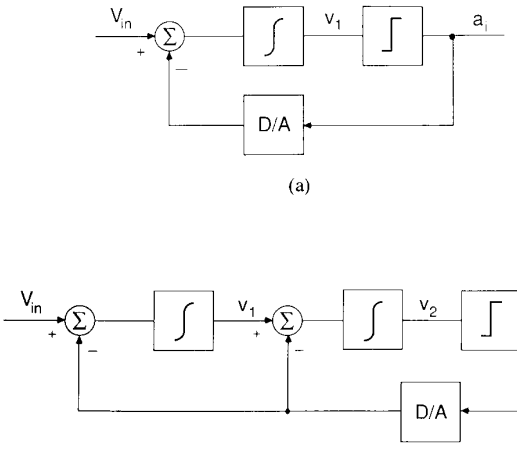

Fig. 1. (a) First-order sigma-delta modulator, and (b) conventional second-order sigma-delta modulator.

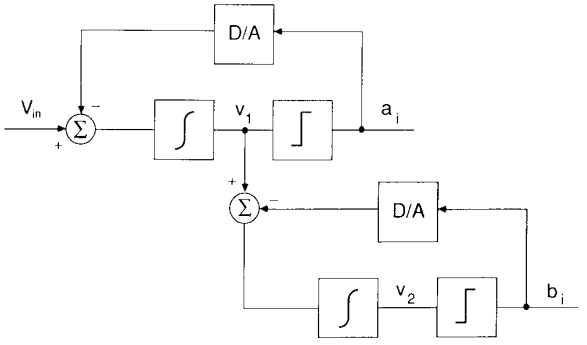

Fig. 2. Second-order multistage sigma-delta modulator.

Fig. 2 shows a different structure of a second-order sigma-delta modulator, also called a multistage sigma-delta modulator [4], [5]. The stability of this modulator is ensured because there is only one integrator in each loop. This structure will be used in the second-order incremental A/D converter.

Manuscript received October 21, 1987; revised January 25, 1988.
The authors are with the Electronic Laboratory, Swiss Federal Institute of Technology, 1015 Lausanne, Switzerland.
IEEE Log Number 8820726.

0018-9200/88/0600-0736$01.00 ©1988 IEEE

III. First-Order Incremental A/D Converter

Fig. 3 represents the circuit diagram of the analog part of the first-order incremental A/D converter [1], [2]. It is composed of a stray-insensitive switched-capacitor integrator, a comparator, and switch control logic.

A four-phase nonoverlapping clock cycle constitutes one integration period (IP), as defined in Fig. 4. The integrator output voltage is designated by $v_1[i, j]$, where i corresponds to the current integration period IP_i and j to the clock cycle ($j = 1$, 2, 3, or 4). Assuming ideal components, the circuit operation for one integration period is as follows.

During clock cycle ϕ_1, S_1 and S_4 are closed, charging $\alpha_1 C_1$ to the input voltage V_{in}.

During ϕ_2, S_3 and S_5 are closed, transferring the charge from $\alpha_1 C_1$ to C_1:

$$v_1[i,2] = v_1[i,1] + \alpha_1 V_{in}. \tag{1}$$

At the end of the charge transfer, the comparator output is denoted by a_i, where $a_i = 1$ (-1) if $v_1[i,2] > 0$ (< 0).

During ϕ_3, S_3 (S_2) and S_4 are closed if $a_i = 1$ ($a_i = -1$).

During ϕ_4, S_2 (S_3) and S_5 are closed if $a_i = 1$ ($a_i = -1$), so that

$$v_1[i,4] = v_1[i,1] + \alpha_1 (V_{in} - a_i V_R) \tag{2}$$

where V_R represents the reference voltage. Note that the dynamic range of V_{in} is given by

$$-V_R \leqslant V_{in} \leqslant V_R. \tag{3}$$

Now, consider a sequence composed of p integration periods IP_i ($1 \leqslant i \leqslant p$), preceded by the resetting of v_1 and a sample and hold of V_{in}. During IP_1, the comparator compares $v_1[1,2] = \alpha_1 V_{in}$ with 0, resulting in a comparison level equal to

$$L_1 = 0 \Rightarrow \begin{cases} a_1 = 1, & \text{if } V_{in} > 0 \\ a_1 = -1, & \text{if } V_{in} < 0. \end{cases} \tag{4}$$

During IP_2, $v_1[2,2] = \alpha_1 (2V_{in} - a_1 V_R)$ is compared to 0, resulting in a comparison level equal to

$$L_2 = a_1 V_R / 2 \Rightarrow \begin{cases} a_2 = 1, & \text{if } V_{in} > 0.5 a_1 V_R \\ a_2 = -1, & \text{if } V_{in} < 0.5 a_1 V_R. \end{cases} \tag{5}$$

Finally, during IP_p, $v_1[p,2]$ is compared to 0:

$$L_p = \left(\sum_{i=1}^{p-1} a_i V_R \right) \Big/ p$$

$$\Rightarrow \begin{cases} a_p = 1, & \text{if } V_{in} > \left(\sum_{i=1}^{p-1} a_i V_R \right) \Big/ p \\ a_p = -1, & \text{if } V_{in} < \left(\sum_{i=1}^{p-1} a_i V_R \right) \Big/ p. \end{cases} \tag{6}$$

Fig. 5 represents each comparison level L_i as a function of i ($p = 8$). One can distinguish four "dead zones," two near 0, one near $+V_R$, and one near $-V_R$, which have widths equal to V_R/p. If a quantization error of less than ± 0.5 LSB is desired, the maximum resolution is given by

$$n_1 = 1b[2V_R/(V_R/p)] = 1b(p) + 1 \text{ [bits]} \tag{7}$$

where $1b(p)$ denotes the binary logarithm of p. Hence, for a resolution of $n_1 = 16$ bits, a total number of $p = 32768$ integration periods is required for every conversion cycle, involving a very slow operation.

The output code N_1 is performed by using an up–down counter [2] which evaluates the quantity

$$N_1 = \left(\sum_{i=1}^{p} a_i \right) + \text{sign}(v_1[p,4]) \tag{8}$$

where sign ($v_1[p,4]$) is equal to 1 (0) if $v_1[p,4]$ is positive (negative). As shown by (8), the digital processing of the comparator output corresponds to a very simple digital filter having a rectangular-shaped impulse response (each coefficient is equal to 1). Some different filters can be used [7]. Resolution may be increased, but *accuracy cannot*. This is due to the dead zones of Fig. 5. Fig. 6(a)–(c) represents

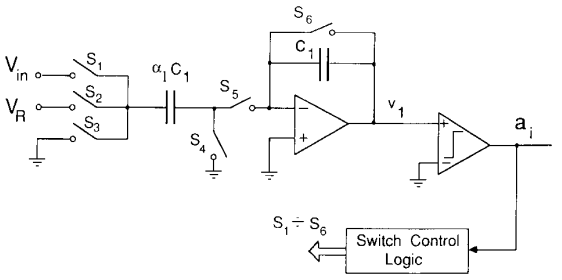

Fig. 3. Circuit diagram of the first-order incremental A/D converter.

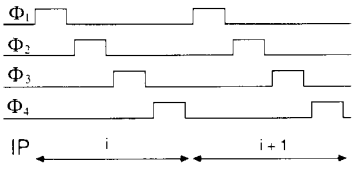

Fig. 4. Integration period (IP) associated with a four-phase nonoverlapping clock cycle.

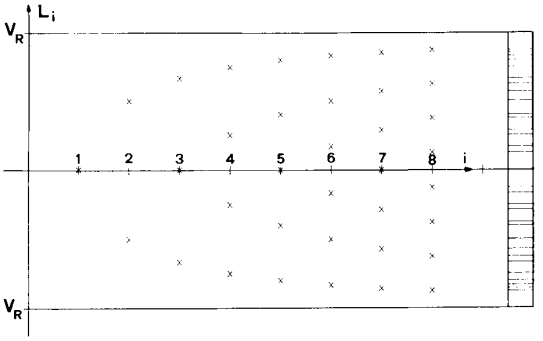

Fig. 5. Comparison levels L_i as a function of i ($p = 8$ in this case).

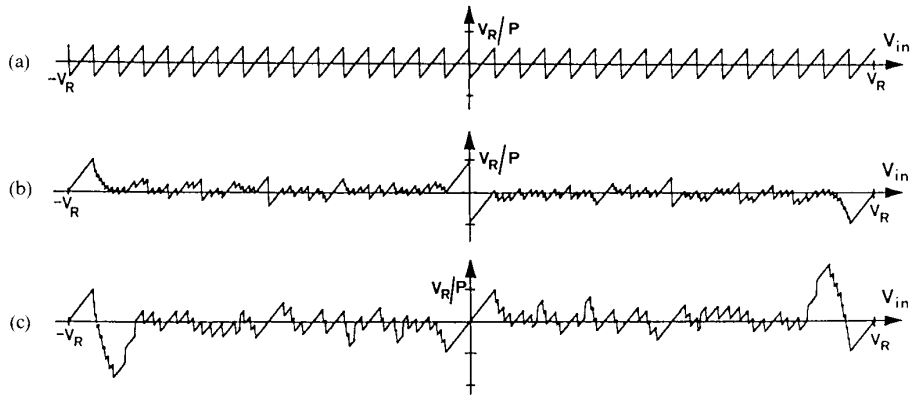

Fig. 6. Simulation of the integral nonlinearity of a first-order sigma-delta modulator ($p=16$): (a) rectangular window, (b) nonsymmetrical triangular window, and (c) symmetrical triangular window.

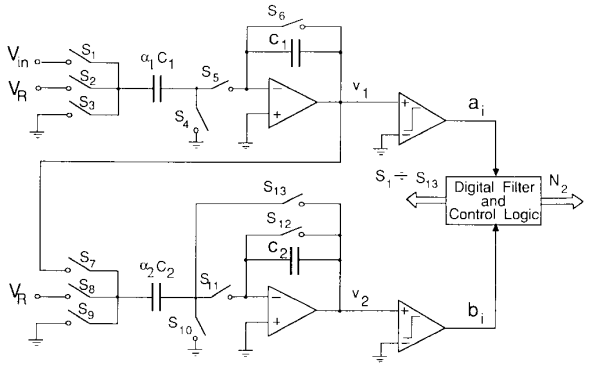

Fig. 7. Circuit diagram of the second-order incremental A/D converter.

a simulation of the integral nonlinearity with $p=16$ for three different filters: a) $C_i=1$ (rectangular window as defined by (8)); b) $C_i=p+1-i$ (nonsymmetrical triangular window); and c) $C_i=i$ for $1\leqslant i\leqslant p/2$, and $C_i=p+1-i$ for $p/2+1\leqslant i\leqslant p$ (symmetrical triangular window [7]), respectively. One can see that resolution is increased in Fig. 6(b) and (c) (the total number of different codes is higher than in Fig. 6(a)), but the maximum integral nonlinearity errors which are associated with the "dead zones" of Fig. 5 are increased.

It has been demonstrated that the converter accuracy is independent of the capacitor ratio α_1 [1], [2]. Moreover, the effect of the amplifier offset and the charge injection can be compensated by using a compensation described in Section VI.

IV. Second-Order Incremental A/D Converter

Fig. 7 represents the analog part of the second-order incremental A/D converter [5]. Assuming ideal components and $\alpha_1=\alpha_2=1$, one conversion cycle is composed of the following.

1) A resetting of both integrator outputs and a sample and hold of V_{in}.

2) A first integration period IP_1 (note that during this integration period v_2 is not modified), where one obtains

$$v_1[1,4]=V_{in}-a_1V_R \tag{9}$$

$$v_2[1,4]=0. \tag{10}$$

3) $(p-1)$ integration periods; V_{in} ($v_1[i-1,4]$) is integrated in the first (second) integrator during IP_i, so that

$$v_1[2,4]=2V_{in}-(a_1+a_2)V_R \tag{11}$$

$$v_2[2,4]=V_{in}-a_1V_R-b_2V_R \tag{12}$$

$$v_1[3,4]=3V_{in}-(a_1+a_2+a_3)V_R \tag{13}$$

$$v_2[3,4]=3V_{in}-(2a_1+a_2)V_R-(b_2+b_3)V_R \tag{14}$$

$$v_1[p,4]=pV_{in}-\sum_{i=1}^{p}a_iV_R \tag{15}$$

$$v_2[p,4]=(p-1)pV_{in}/2-\sum_{i=1}^{p-1}a_i(p-i)V_R-\sum_{i=2}^{p}b_iV_R. \tag{16}$$

4) An integration period IP_{p+1}, involving

$$v_2[p+1,4]=p(p+1)V_{in}/2-\sum_{i=1}^{p}a_i(p+1-i)V_R-\sum_{i=2}^{p+1}b_iV_R. \tag{17}$$

Under the conditions $\alpha_1=1$, $\alpha_2=1$, it can be shown that the dynamic range of $v_2[p+1,4]$ is given by

$$-V_R\leqslant v_2[p+1,4]\leqslant V_R. \tag{18}$$

With (17), (18) can be rewritten in the form of

$$\begin{aligned}-2V_R/[p(p+1)]&\leqslant V_{in}-\left\{\sum_{i=1}^{p}a_i(p+1-i)+\sum_{i=2}^{p+1}b_i\right\}2V_R/[p(p+1)]\\&\leqslant 2V_R/[p(p+1)].\end{aligned} \tag{19}$$

Defining D and x as

$$D = \sum_{i=1}^{p} a_i(p+1-i) + \sum_{i=2}^{p+1} b_i \tag{20}$$

$$x = 2V_R/[p(p+1)] \tag{21}$$

(19) can be rewritten in the form of

$$-x \leqslant V_{in} - Dx \leqslant x. \tag{22}$$

Ideal A/D converter quantization error is normally given by

$$-V_{LSB}/2 \leqslant V_{in} - NV_{LSB} \leqslant V_{LSB}/2 \tag{23}$$

where N is the digital representation of V_{in} and V_{LSB} is the analog voltage corresponding to the least significant bit. Equations (22) and (23) give

$$V_{LSB} = 4V_R/[p(p+1)]. \tag{24}$$

The converter output code N_2 is thus given by

$$N_2 = \left(\sum_{i=1}^{p} a_i(p+1-i) + \sum_{i=2}^{p+1} b_i \right) \Big/ 2. \tag{25}$$

Resolution is given by (note that $-V_R \leqslant V_{in} \leqslant V_R$)

$$n_2 = 1b(2V_R/V_{LSB}) = 1b[p(p+1)] - 1$$
$$= 21b(p) - 1 \text{ [bits]}, \qquad \text{if } p \gg 1. \tag{26}$$

The above development does not take into account the error caused by the capacitor matching. Introducing $\alpha_1 = 1 + \Delta\alpha_1$ and $\alpha_2 = 1 + \Delta\alpha_2$, one can show that an additional quantization error ϵ_c results:

$$\epsilon_c = 0.25p\Delta\alpha_1 \text{ [LSB]}. \tag{27}$$

It is interesting to notice that the value of α_2 does not affect the conversion accuracy. As an example, a 16-bit resolution, which requires from (26) that $p = 362$, associated with a standard technology ($\Delta\alpha_1 = 0.1 \sim 0.2$ percent) involves an error ϵ_c smaller than $0.1 \sim 0.2$ LSB.

An extra-bit accuracy can be obtained by detecting the sign of $v_2[p+1,4]$ at the end of the conversion cycle. This can be achieved without increasing significantly the conversion time. Equations (24)–(27) are replaced by

$$V_{LSB} = 2V_R/[p(p+1)] \tag{28}$$

$$N_2 = D + \text{sign}(v_2[p+1,4]) \tag{29}$$

$$n_2 = 21b(p) \text{ [bits]} \tag{30}$$

$$\epsilon_c = 0.5p\Delta\alpha_1 \text{ [LSB]}. \tag{31}$$

Hence, for a $n_2 = 16$-bit resolution, a total number of $p + 1 = 257$ integration periods is required for each conversion cycle. Compared to a first-order structure, this yields an important reduction of the conversion time. It should be pointed out that (30) gives the *maximum resolution* corresponding to a quantization error of less than ± 0.5 LSB.

TABLE I

	order			
Resolution	1	2	3	4
12	2048	65	25	18
13	4096	91	31	21
14	8196	129	39	24
15	16368	182	48	28
16	32768	257	60	33

The digital processing of the comparator outputs, as shown by (20) and (29), corresponds to two digital filters having triangular- and rectangular-shaped impulse responses. The order of the sigma-delta modulator and the digital filter must therefore be equal if the quantization error is expected to satisfy (23).

V. Mth-Order Incremental A/D Converter

The developments of Section IV can be extended to a mth ($m > 2$) order incremental A/D converter. Due to the use of a multistage sigma-delta modulator, there are no overload effects even if $m > 2$ [5], [6]. It can be shown that resolution is given by

$$n_m = 1b\left\{ \left[\prod_{i=1}^{m} (p+i-1) \right] \Big/ m! \right\} + 1$$
$$= m1b(p) - 1b(m!) + 1, \qquad \text{if } p \gg 1. \tag{32}$$

Table I represents the total number of integration periods $N_{IP1} = p + m - 1$ required for each conversion cycle as a function of the resolution and the order. Each comparator output sequence is fed into a digital filter. Impulse response of the ith filter ($1 \leqslant i \leqslant m$) is of $(m - i + 1)$th order. Such filters can easily be implemented by using counters, adders, and registers, without requiring prohibitive die area. Converter output code is obtained by adding the filter outputs.

VI. Offset and Charge Injection Compensation

Consider the general case of a mth-order incremental A/D converter. Each integrator I_i ($1 \leqslant i \leqslant m$) can be characterized by an input-referred offset $V_{\epsilon i}$. This offset is caused by the charge injection of the switches which are situated on the right side of the capacitors $\alpha_i C_i$ ($1 \leqslant i \leqslant m$) and by the amplifier offset. Note that $V_{\epsilon i}$ can be made independent of V_{in} [1]. In order to compensate the effect of these $V_{\epsilon i}$ terms, the conversion cycle is divided into three periods, preceded by a reset of each integrator output and a sample and hold of V_{in}.

1) During the first period, which requires $p + m - 1$ integration periods, the circuit operation corresponds to that described in Section IV. The integrator output voltage

TABLE II

Resolution	order 1	2	3	4
12	2049	94	41	30
13	4097	130	51	34
14	8197	184	63	40
15	16369	258	77	48
16	32769	366	97	56

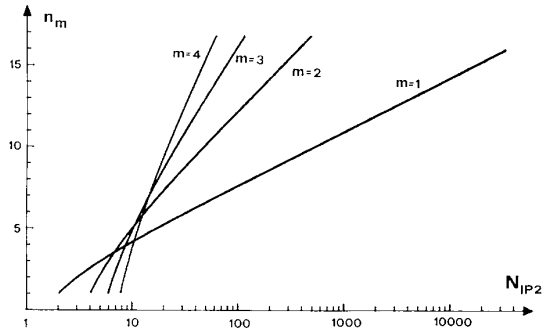

Fig. 8. A graph of n_m against N_{IP2} for various values of the order m.

v_m is given by

$$v_m[p+m-1,4] = \left\{\prod_{i=1}^{m}(p+i-1)\right\}V_{in}/m! + F_1(a,b,\cdots,V_R,p,m) + \sum_{i=1}^{m}\left\{2V_{\epsilon i}\prod_{j=i}^{m}(p+m-j)\right\}\Big/(m-i+1)! \quad (33)$$

where $F_1(a,b,\cdots,V_R,p,m)$ represents the voltage component of V_m related to the reference voltage.

2) During the second period, the output voltages of the first $m-1$ integrators are reset ($v_i[p+m,4]=0$, $1 \leqslant i \leqslant m-1$), while $v_m[p+m-1,4]$ is inverted [1]:

$$v_m[p+m,4] = -v_m[p+m-1,4]. \quad (34)$$

3) During the third period, which requires $p+m-1$ integration periods, the circuit operation is analogous to that of the first period, except that the voltage v_1 integrates $-V_{in}$ instead of $+V_{in}$. One obtains

$$v_m[2p+2m-1,4] = -\left\{2\left\{\prod_{i=1}^{m}(p+i-1)\right\}V_{in}/m! + F_2(a,b,\cdots,V_R,p,m)\right\}. \quad (35)$$

One can see from this last equation that all error terms $V_{\epsilon i}$ have disappeared. It can be shown that resolution is now given by

$$n_m = 1b\left\{\prod_{i=1}^{m}(p+i-1)\right\}\Big/m!+2 = m1b(p)-1b(m!)+2\ [\text{bits}], \quad \text{if } p \gg 1. \quad (36)$$

Table II represents the total number of integration periods $N_{IP2}=2p+m$ required for each conversion cycle as a function of the resolution and the order. Fig. 8 presents a graph of n_m against N_{IP2} for various values of m. The ratio of conversion times with and without offset compensation is given by

$$N_{IP2}/N_{IP1} = 2^{(m-1)/m}, \qquad m \geqslant 1,\ p \gg m. \quad (37)$$

It should be pointed out that the order of the digital filter is not modified by the offset and charge injection compensation.

VII. Comparison with Sigma-Delta Converters

When the number of integration periods p is doubled, (36) indicates a gain of m bits. In terms of signal-to-noise ratio, this corresponds to an improvement of $6m$ dB per octave. Theory of sigma-delta modulation [3], [9] shows that the corresponding improvement of sigma-delta converters is equal to $6m+3$ dB per octave of oversampling (9 dB (15 dB) for the first (second) order). Those results have been obtained under the condition that the input voltage is "sufficiently busy." It should be pointed out that these values correspond to the average noise level on the whole dynamic range [3]. It is well-known that certain quiet input levels produce a drastic increase of the in-band noise; such peaks of noise decrease only with a ratio of 6 dB (12 dB) per octave of oversampling for a first- (second-) order structure (see [8, fig. 2]). These peaks of noise are related to the "dead zones" of Fig. 5.

MOS technology involves large converter offset caused by the amplifier offset and charge injection. The incremental converter is very well suited to offset compensation, while sigma-delta converters are not. This difference excludes many sigma-delta converter applications.

Digital signal processing required by sigma-delta converters demands extensive digital filters, while the incremental converter needs only a simple one. As an example, a second-order filter designed for a 16-bit resolution involves a die area equal to only 1 mm^2 in a 3-μm SACMOS process. The design of incremental converters is therefore very versatile: filter design can easily be carried out for a wide range of applications.

The incremental converter requires a sample and hold, whereas sigma-delta converters sample continuously the input signal, which must be sufficiently busy. In many applications, the quantization of specific samples is desired. For example, some industrial process controls use multiplex operation. It also happens that the input signal is not always available. Therefore, as a sample and hold is necessary, incremental converters offer significant advantages over sigma-delta converters.

VIII. Experimental Results

A second-order micropower incremental A/D converter has been integrated in a 3-μm low-voltage p-well SACMOS technology. The capacitances were equal to 10 pF ($\alpha_1 =$

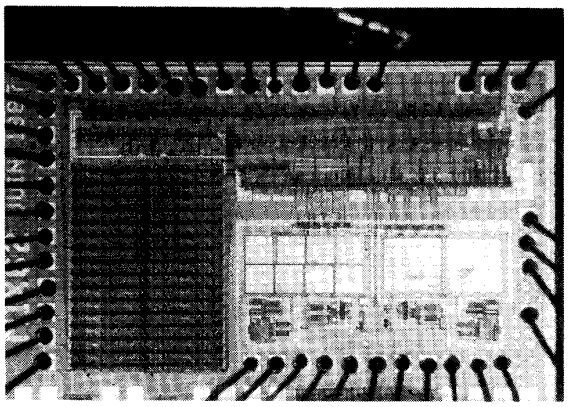

Fig. 9. Photograph of the second-order incremental A/D converter.

TABLE III

Supply voltage	$V_{DD} = -V_{SS} = 2.5$ V
Power consumption of the analog part	325 μW
Resolution	15 bits
Reference voltage	0.82 V
V_{LSB}	50 μV
Conversion time	10 ms
Active die area (including logic and pads)	4.6 mm^2
Offset	< 0.25 LSB
Gain error	< 0.3 LSB
Differential nonlinearity	< 0.3 LSB
Integral nonlinearity	< 0.3 LSB
PSSR	> 65 dB

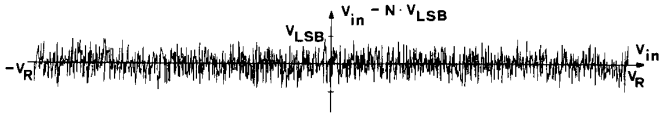

Fig. 10. Measured quantization error function. $V_R = 0.82$ V, $n = 15$ bits, and $T_c = 10$ ms.

$\alpha_2 = 1$), and the operational amplifiers were single-stage cascoded transconductance amplifiers. The photograph of the chip is shown in Fig. 9. Its die area is 4.6 mm^2.

Table III summarizes the experimental results while Fig. 10 presents a typical measured quantization error function.

IX. Conclusions

A different use of sigma-delta modulation has been reported. Compared to a first-order incremental A/D converter, the use of a second-order structure allows a substantial reduction of the conversion time. No overload effects exist, even if multiple loop structures are used.

An optimal digital filtering has been derived. It was found that the order of both the filter and the sigma-delta modulator must be equal. Such filters are easy to implement and require modest die area. The presented A/D conversion principle is well suited to offset compensation.

Compared to some other high-resolution A/D converters, the incremental converter requires only a single reference voltage for bipolar operation. Moreover, it does not need laser trimming or self-calibration cycles. As with many other A/D converters, the incremental converter requires a sample and hold. This is its only drawback compared to sigma-delta converters.

References

[1] J. Robert and V. Valencic, "Offset and charge injection compensation in an incremental analog-to-digital converter," in *Proc. European Solid-State Circuits Conf.* (Toulouse, France), Sept. 1985, pp. 45–48.

[2] J. Robert, G. C. Temes, V. Valencic, R. Dessoulavy, and P. Deval, "A 16-bit low-voltage CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 2, pp. 157–163, Apr. 1987.

[3] J. C. Candy, "A use of double integration in sigma-delta modulation," *IEEE Trans. Commun.*, vol. COM-33, no. 3, pp. 249–258, Mar. 1985.

[4] T. Hayashi, Y. Inabe, K. Uchimura, and T. Kimura, "A multistage delta-sigma modulator without double integration loop," in *ISSCC Dig. Tech. Papers*, Feb. 1986, pp. 182–183.

[5] J. Robert and P. Deval, "A second order high-resolution incremental A/D converter with offset and charge injection compensation," in *Proc. European Solid-State Circuits Conf.* (Bad Soden, Germany), Sept. 1987, pp. 109–112.

[6] Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, and M. Ishikawa, "A 16b oversampling A/D conversion technology using triple noise shaping," in *ISSCC Dig. Tech. Papers*, Feb. 1987, pp. 48–49.

[7] J. C. Candy, Y. C. Ching, and D. S. Alexander, "Using triangularly weighted interpolation to get 13-bit PCM from a sigma-delta modulator," *IEEE Trans. Commun.*, vol. COM-24, no. 11, pp. 1268–1275, Nov. 1976.

[8] J. C. Candy and O. J. Benjamin, "The structure of quantization noise from sigma-delta modulation," *IEEE Trans. Commun.*, vol. COM-29, no. 9, pp. 1316–1323, Sept. 1981.

[9] J. C. Candy, "Decimation for sigma-delta modulation," *IEEE Trans. Commun.*, vol. COM-34, no. 1, pp. 72–76, Jan. 1986.

Jacques Robert was born in Lausanne, Switzerland, on July 14, 1959. He received the M.S. degree in electrical engineering from the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 1984.

He is employed as a Research Assistant at the Swiss Federal Institute of Technology, and is involved in CMOS micropower A/D converter design.

Philippe Deval was born in La Rochelle, France, on July 15, 1960. He received the M.S. degree in electrical engineering from the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 1983.

Since 1984 he has been employed as a Research Assistant at the Electronic Laboratory of the Swiss Federal Institute of Technology. His research field is CMOS A/D converter design.