# AMS Designer User Guide: PLL Modeling

IEE 5644 Mixed-Signal IC Design and Laboratory

National Chiao-Tung University Department of Electronics Engineering

### 1. Getting Start

- Copy the file need for Demo
   % cp ~msic/Tools\_Course/AMS\_DEMO.tar
- Extract the archive % tar xvf AMS\_DEMO.tar
- Change the directory to working directory % cd AMS\_DEMO
- Start the AMS environment % icms&

### 2. Files Required for Simulation

#### • Environment Definition file

The *hdl.var* file sets options and switches used by the simulator. Typical *hdl.var* file looks like :

SOFTINCLUDE /home/user/eda/solaris/cadence\_2003/LDV/LDV40/tools.sun4v/inca/file/hdl.var

# include default setup

DEFINE ncuse5x

# set library structure for 5.X. The 5.X format is a Cadence library standard directory structure,

# where each cell is reference by *library.cell:view*.

DEFINE cdslib ./cds.lib

# include libraries

Define NCVLOGOPTS -linedebug -messages

# tell ncvlog to compile the code in a manner that allows setting breakpoint in the analog and

# digital code in the Cadence AMS Simulator Windows

Define NCVHDLOPTS -V93 -linedebug -messages

# tell ncvhdl to compile the code in a manner that allows setting breakpoint in the analog and

# digital code in the Cadence AMS Simulator Windows

DEFINE WORK PLL\_examples

# setting current working library

DEFINE MODELPATH ./model/logs353va.scs(tt)

# include models need for transistor level simulation

• Analog Primitive Table files

Cadence Verilog-AMS use an Analog Primitive Table file to identify which devices are analog primitives or subcircuits rather than Verilog modules. Use **genalgprim** command to create a primitive table from an existing Spectre model file.

#### % cd model

% genalgprim logs353va.scs (or ./gen\_apt instead)

• Connect module

Connect module connect analog and digital blocks to translate one domain to the other. Connect module include a D-to-A converter (*logic2elect.v*), a A-to-D converter (*elect2logic.v*) and a connecting rule definition module (*crules.v*). Use **ncvlog** to compile these files.

% ncvlog -ams -use5x ./connect\_lib/crules.v % ncvlog -ams -use5x ./connect\_lib/elect2logic.v % ncvlog -ams -use5x ./connect\_lib/logic2elect.v (or ./ compileConnect instead)

### 3. Binding Cells for Simulation

In DFII window, create a new cell (**File>new>cell view**), as shown in Fig. 2.

💌 icms - Log: /home/us	er/cwfan/CDS.log		
File Tools Options		Help	1
New P Open	Library DESIGN SYSTEMS INC. ALL RIGHTS RESERVED. STEMS Laboratories INC., Cellview duced with permission., journe and online documentation are		
Export	tial information and may be disclosed/used only icense agreement controlling such use and disclosure. RIGHTS NOTICE (SHORT FORM) closure is subject to restriction		
Make Read Only Close Data	2.227-19 or its equivalent. @(#)\$CDS: icms.exe version 5.0.0 05/25/2002 12:34 (cds11620) \$ sub-version 5.0.0.132 (32-bit addresses)		
Defragment Data > Exit END OF SITE CUSTOMIZ	ATION		
warning: Cannot conv I	rert string "-adobe-neivetica-medium-r-normaiu-100-75-75-p-0-1808859-1" to type FontStruct		
mouse L:	M: R:		

Fig.1 DFII window

Choose the **Tool** to **Hierarchy-Editor** and fill in the **Cell Name** blank with **PLL**.

🗵 Create New File 🛛 🔀					X
ок	Cance	el Defaults		Help	
Library Name			.L_exampl	es 💷	_
Cell Name		PI	LLĽ		
View Name		C	onfig		
Tool			Hierarc	hy-Editor	
Library path file					
/home/user/cwfan/AMS_DEMO/cds.lib					

Fig.2 Create a config view cell

New Configuration
Top Cell
Library: PLL_examples Cell: PLL View: Browse
Global Bindings
Library List:
View List:
Stop List:
Description
OK Cancel Use Template Help

Click Browse button in New Configuration window

Fig. 3 New Configuration window

### Select PLL>schematic

<b>Choose th</b>	e Top Cell	
-Top Cell-		Browse
Library:	PLL_examples	cds.lib ▲ ∳- 😧 PLL_examples
Cell:	PLL	• • • • D_ff
View:	schematic	PD_test
		Config
	OK Cancel	Filters Help

Fig. 4 Select a cell for simulation

Click **Use Template** button in New Configuration, select **Name** as **AMS** as shown in Fig. 5.

🗵 Use Template 🛛 🔀				
Template				
Name:	AMS 💌			
From File:	dssetup/hierEditor/templates/AMS			
OK Cancel Apply Help				

Fig. 5 Use Template window

Right click the **View Found**, and select each cell with the cell view shown in Fig. 6. The **View to Use** is the view used during simulation.

🗵 Cadence?hierarchy editor: New Configuration						
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Top Cell						
Library: PLL	_examples	Cell:  PLL	View: schemati	Open		
-Global Binding	gs					
Library List:	basic					
View List:	verilogams veriloga bet	havioral functional schematic s	vmbol			
	,		-			
Stop List:	symbol					
Cell Bindings						
Library	Cell	View Found	View to Use	Inherited View List		
PLL_examples	PD	veriloga		verilogams veriloga be 🔺		
PLL_examples	PLL	schematic		verilogams veriloga be		
PLL_examples	VCO	veriloga		verilogams veriloga be		
PLL_examples	ср	veriloga		verilogams veriloga be		
PLL_examples	div_4	symbol		verilogams veriloga be		
PLL_examples	lp_filter	schematic		verilogams veriloga be		
PLL_examples	power_supply	schematic		verilogams veriloga be		
analogLib	cap	symbol		verilogams veriloga be		
analogLib	res	symbol		verilogams veriloga be		
analogLib	vdc	symbol		verilogams veriloga be		
analogLib	vpulse	symbol		verilogams veriloga be		
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set forth at FAF	set forth at FAR 1252.227-19 or its equivalent.					
FMP: Library physical path not found at line number 3						
of file /home/user/cwfan/AMS_DEMO/cds.lib						
Created new configuration.						
Readv						

Fig. 6 Hierarchy-Editor

🗵 Cadence?hierarchy editor: New Configuration (Save Needed)						
File Edit View Plug-Ins Help						
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Top Cell						
		/ 				
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-Global Binding	]8					
Library List:	basic					
View List:	verilogams veriloga beha	avioral functional schemati	c symbol			
Stop List:	sympol					
	printer					
Cell Bindings						
Library	Cell	View Found	View to Use	Inherited View List		
PLL_examples	PD	veriloga	veriloga	verilogams veriloga be 🔺		
PLL_examples	PLL	schematic		verilogams veriloga be		
PLL_examples	VCO	veriloga	veriloga	verilogams veriloga be		
PLL_examples	ср	veriloga	veriloga	verilogams veriloga be		
PLL_examples	div_4	verilog	verilog	verilogams veriloga be		
PLL_examples	lp_filter	schematic	schematic	verilogams veriloga be		
PLL_examples	power_supply	schematic	schematic	verilogams veriloga be		
analogLib	cap	symbol		verilogams veriloga be		
analogLib	res	symbol		verilogams veriloga be		
analogLib	vdc	symbol		verilogams veriloga be		
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Bound cell (PLL_examples div_4) to view "verilog".						
Bound cell (PLL_examples Ip_filter) to view "schematic".						
Bound cell (PLL	_examples power_supply	() to view "schematic".		<u> </u>		
Ready			A Und			

Fig. 7 Update the settings

Click on the **update** icon to save the settings.

## 4. Running AMS Designer

In the Hierarchy-Editor window, click on **Plug ins** > **ams**. The AMS toolbar menu will now appear towards the left on the menu bar as shown in Fig. 8.

🗵 Cadence?hierarchy editor: (PLL_examples PLL config)						
File Edit Vi	ew AMS			Plug-Ins Help		
n 🛋 📮 📝 🕅 👦 🗛 🚳 角 🎼 🖩 🖬						
	<u> </u>					
- top Gen						
Library: PLL	Library: PLL_examples Cell: PLL View: schematic Open					
Global Bindin	gs					
Library List:	basic					
View List:	verilogams veriloga bel	havioral functional schemati	c symbol			
Stop List:	symbol					
Cell Bindings						
Library	Cell	View Found	View to Use	Inherited View List		
PLL_examples	PD	veriloga	veriloga	verilogams veriloga be 🔺		
PLL_examples	PLL	schematic		verilogams veriloga be		
PLL_examples	VCO	veriloga	veriloga	verilogams veriloga be		
PLL_examples	ср	veriloga	veriloga	verilogams veriloga be		
PLL_examples	div_4	verilog	verilog	verilogams veriloga be		
PLL_examples	lp_filter	schematic	schematic	verilogams veriloga be		
PLL_examples	power_supply	schematic	schematic	verilogams veriloga be		
analogLib	cap	symbol		verilogams veriloga be		
analogLib	res	symbol		verilogams veriloga be		
analogLib	vdc	symbol		verilogams veriloga be		
analogLib	vpulse	symbol		verilogams veriloga be		
<u>_</u>				<u> </u>		
Messages	*****					
	_елантріез сруто чіем	четнода .				
Bound cell (PLL_examples div_4) to view "verilog".						
Bound cell (PLL_examples Ip_filter) to view "schematic".						
Bound cell (PLL_examples power_supply) to view "schematic".						
Saved the current configuration to (PLL_examples PLL config).						
Ready				Filters OFF CDBA		

Fig. 8 Hierarchy-Editor

Click on the AMS menu> Run Directory...

💌 AMS Run Directory	X
Run directory:	/home/user/cwfan/AMS_DEMO/PLL_run Browse
Existing run directories:	
🗌 Always use this run di	rectory for this configuration
Copy Run Directory Set	up
From this run directory	
	Browse
Existing run directories	:
Files to copy:	
Сору:	Do not copy:
	OK Cancel Apply Help

Fig. 9 AMS run directory

A default run directory appear as \$AMS\_DEMO/ PLL\_run, then click on OK.

Run directory will receive:

- simulation output files
- log files produced during simulation flow
- environment files related to form settings
- waveform data
- simulation control files
- SimVision script files

Pull down **AMS>Options>Complier** in Hierarchy-Editor window. Use the Browse button under **hdl.var file,** select the *hdl.var* under AMS\_DEMO directory.

AMS Options	
Categories:	7- ···
₽- Netlister	Compiler
- Verilog-AMS	hdl.var file: /home/user/cwfan/AMS_DEMO/hdl.var
©-Compiler	Browse Edit
• Verilog-AMS	
• VHDL	
- Elaborator	Exclude Libraries From Compilation
- Simulator	Library name:
Global Design Data	bba
	Remove
	Compile digital HDL without "-ame" option

Fig. 10 AMS Options window

Click on **Elaborator** in AMS Option window, and modify it to **100ps/100ps**.

MMS Options	X
Categories:	
<b>♀</b> - Netlister	Elaborator
verilog-AMS	Maximum number of errors: 50 -
Verilog-AMS	Log file: Overwrite log file 🔻
<ul> <li>Elaborator</li> <li>Simulator</li> </ul>	🗹 Update design units if needed
Global Design Data	Ignore source file timestamps when using -update
	Default discipline: logic
	Use detailed discipline resolution
	Default timescale: 100ps/100ps
	✓ Allow undefined parameters
	Additional arguments:
	OK Cancel Apply Help

Fig. 11 Setting timescale

Click on **Simulator>Analog Solver>Tran Analysis**, enter 1u in the Stop time field.

AMS Options	
Categories:	
P-Netlister	Tran Analysis
- Verilog-AMS	
∲- Compiler	
- Verilog-AMS	
VHDL	Analysis title:
🗪 Elaborator	
P→ Simulator	Stop time:
- Performance	
- C Interface	
- Messages/Errors	Error preset: moderate 💌
- Analog Solver	
- Convergence/Accuracy	Additional ontions:
- Output/Debug	
- Tran Analysis	
Global Design Data	
	OK Cancel Apply Help

Fig. 12 Setting simulation time

Click on **Analog Solver>Tran Analysis>Convergence/Accuracy** Modify **Maxstep** to **100p**.

ategories:				
∲- Netlister	Tran Convergence/Accu	racy		
- Verilog-AMS	Numerical Options			
o-Compiler	Integration method:	<default value=""> 💌</default>	Cmin:	0.0
Verilog-AMS				
- VHDL	Step:	<value defaulted<="" td=""><td>Maxstep:</td><td>100p</td></value>	Maxstep:	100p
🗢 Elaborator				
- Simulator	Reiref:	<default value=""> 💌</default>	Lteratio:	<value defaulted<="" td=""></value>
- Performance				
- C Interface	Maxiters:	5		
<ul> <li>Messages/Errors</li> </ul>				
-Analog Solver	Initial Conditions/Not	lesets		
- Convergence/Accuracy	Initial condition:	ali 🔻		
- Output/Debug				
∲- Tran Analysis	Set initial conditions	:		
-Convergence/Accuracy				
- Output	Read IC from file:			
Global Design Data		Browse	Edit	
	Read nodesets from	file:		
		Browse	Edit	
	Skipdc:	no 🔻		

Fig. 13 Accuracy setting

Execute **AMS>Design Prep** in Hierarchy-Editor window, enable **Netlist** - **All** and **Compile** – **All** and then click **Run**.

💌 AMS Design Prep	
🗹 Netlist	Netlister Options
🔿 Incremental	
IIA 🖲	
🗹 Com pile	Compiler Options
O When netlisting	
All cellviews	
Run Cance	l Help

Fig. 14 AMS design Prep window

💌 AMS	Design Prep - Summary	×
Ĵ	Design Prep complet	ed successfully.
	Netlisted cellviews:	3
	Compiled cellviews v	vith
	Verilog netlists:	8
	VHDL netlists:	0
	Errors:	0
	New global signals fo	ound: 0
	New design variables	s iouliu. U
	ОК	

Fig. 15 AMS design Prep summary

When compiling completed, the Design Prep Summary message box appears.

Click on **AMS>Run Simulation** in Hierarchy-Editor window fill the blanks as show in Fig. 16.

🗷 AMS Run Simulation				×
Configuration:				
Library PLL_examples	Cell	PLL	View	config
Global Design Data Module:				
Library PLL_examples	Cell	cds_globals	View	PLL_config
Connect Rules:				
Library	Cell	mixedsignal	View	
Simulation Snapshot:				
Library	Cell	PLL	View	ams1060937567558
Elaborator Options		Simul	ator Op	otions
🗹 Run Elaborator		🗹 Run 8	6 im ulat	or
		Run Moo	ie: Gl	л 💌
Save NC commands to	o file "	./runElabSim"		
Run	c	ancel Apply	н	elp

Fig. 16 AMS run simulation

When the Elaborator is finished, the Cadence AMS simulator window appears. Click on the **Navigator** icon to open the Navigator window.

Codence AMS Simulator	
Elle Run Set Show Select Windows Options	Help
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10 , width(2 sh), \delay(0), vval(0,0)) (*	
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15 pover_supply #(.vdd2(3.3)) (*	
<pre>15 integer library_binding = "FLL_examples"; *) 17 ( .vddd( 16 cds_globals.\vdd! ) );</pre>	
17         18         div_4 (* integer library_binding = "PLL_examples"; *) I6 ( .RSTN(	У
Debug Scope PLU	$\overline{\Delta}$
Subscopes = [	Δ
Analog Kernel using -ANALOGCONTROL	
/home/user/cwtan/AHS_DEMU/PLL_run/amSBC.scs.	
No. Logy one connection to node we will also have a start of the new start	
path.	
Circuit inventory:	
nodes 10 equations 19	
and simulator 1 cepacitor 2	
elact21gii 2 laci-221gii 1	
resistor 1	
VC0 1 vsource 4	
Transformation analysis 'anshalysis': time = $(0 \text{ s} - )1 \text{ us}$	
ncsim> source/home/user/eda/solaris/cadence_2003/LDV/LDV40/tools.sun4v/inca/files/ncsimrc	
And and T	
Ready transient(initial	zation)

Fig. 17 AMS simulator window



Fig. 18 Navigator window

Select signals you want to observe and click on the **Waveform View** icon, then SimVision window appears.

SimVision: Waveform 1										
<u>F</u> ile <u>E</u> dit <u>V</u> iew Ex <u>p</u> lore	For <u>m</u> at <u>W</u> ine	dows								Help
🗃 🖌 🗠 🛛 🐇 🛍	×			<b>Q</b>	□₄ ϝ□	<b>0</b> 4 <b>•</b> 0	RE	🕨 💽	•	💼 • 💷 ·
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Baseline = 0 Cursor-Baseline = 0		Baseline = 0 TimeA = 0(0)								
	Cursor 👻	0 200ns	400ns	600ns	800ns	1000ns	1200ns	1400ns	1600ns	1800ns
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		<b>0</b>	400	600	800	1000	1200	1400	1600	2000ns >
10									0.0	bjects selected

Fig. 19 SimVision window

Click on the **Run** button to start the simulation as show in Fig. 20.

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File Run Set Show Select Windows Options	Help
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0) y rearce #(.rise(100p), .peried(5.6.n), .val(3.3), .fal(100p), .type('pulse') 10, .vid#(5.6.n), .Val630(0), .val(0.00), .val(0.00), . 11 integer library.handing = 'analagib'; *) V3 ( []], 12 dat.lebat.vadd ):	-
<pre>13 14 15 15 15 15 15 15 15 15 15 15 15 15 15</pre>	
17 10 div_4 (* integer library_binding = "Pil_examples"; *) 16 ( .ESTN(	
Debug Scope PLL	X
Subscopes and	V
	4.0
Analog Kernel using -AMALOGONTROL /home/watr/ewfox/AMS_DEMO/FLL_rum/oms80.scs.	
Mariar from spectre during topology chark. Odly one consection to mode "Alg.JohaisVed" '. So De path from ande "PLL.vetri' to ground, Gwin installed to provide path.	
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Jagocalety 1 versiter 1 VCD 1 versiter 4	
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	Transient/initialization

Fig. 20 Start simulation

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19 92	seurce #	(rise(100p), .peried(5.6n), .vell(3.3), .fall(100p), .type("pulse")	
1 4	.widthC	2.00), .tdelay (0), .val(0.0)) (* (brav bioline = "analadib", *) %2 (****)	
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5 in	ateger 1:	ply #(.vod(5.5)) (^ brary_binding = "FL_examples"; *) I7 ( .vddd(	
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ulatio	on comple	ete via transfeat analysis stopfime at time 2 US	
Uzage	e - 0.5s	rystes - 7.3s user - 7.8s total (15.3s cps)	
187 F			

Fig. 21 Simulation complete

When simulation is completed, check the simulation time in the bottom of the AMS simulation window.

Back to Hierarchy Editor, and change PD, cp, VCO, div\_4 to **schematic view**, **Run direction** to PLL\_run2 and repeat these steps. Compare the simulation time difference.

Click on **File>Open Databas** in SimVision window and change the folder to PLL\_run/waves.shm/waves.trn as show in Fig. 22.



Fig. 22 SimVision design browser

Compare the waveform difference between two different simulations.