

AMS Designer User Guide: PLL Modeling

IEE 5644 Mixed-Signal IC Design and Laboratory

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1. Getting Start

- Copy the file need for Demo
% cp ~msic/Tools_Course/AMS_DEMO.tar
- Extract the archive
% tar xvf AMS_DEMO.tar
- Change the directory to working directory
% cd AMS_DEMO
- Start the AMS environment
% icms&

2. Files Required for Simulation

- Environment Definition file

The *hdl.var* file sets options and switches used by the simulator.

Typical *hdl.var* file looks like :

```
SOFTINCLUDE /home/user/eda/solaris/cadence_2003/LDV/LDV40/tools.sun4v/inca/file/hdl.var
# include default setup

DEFINE ncuse5x
# set library structure for 5.X. The 5.X format is a Cadence library standard directory structure,
# where each cell is reference by library.cell:view .

DEFINE cdslib ./cds.lib
# include libraries

Define NCVLOGOPTS -linedebug -messages
# tell ncvlog to compile the code in a manner that allows setting breakpoint in the analog and
# digital code in the Cadence AMS Simulator Windows

Define NCVHDOPTS -V93 -linedebug -messages
# tell ncvhdl to compile the code in a manner that allows setting breakpoint in the analog and
# digital code in the Cadence AMS Simulator Windows

DEFINE WORK PLL_examples
# setting current working library

DEFINE MODELPATH ./model/logs353va.scs(tt)
# include models need for transistor level simulation
```

- Analog Primitive Table files

Cadence Verilog-AMS use an Analog Primitive Table file to identify which devices are analog primitives or subcircuits rather than Verilog modules. Use **genalprim** command to create a primitive table from an existing Spectre model file.

```
% cd model
```

```
% genalprim logs353va.scs (or ./gen_apt instead)
```

- Connect module

Connect module connect analog and digital blocks to translate one domain to the other. Connect module include a D-to-A converter (*logic2elect.v*), a A-to-D converter (*elect2logic.v*) and a connecting rule definition module (*crules.v*). Use **ncvlog** to compile these files.

```
% ncvlog -ams -use5x ./connect_lib/crules.v  
% ncvlog -ams -use5x ./connect_lib/elect2logic.v  
% ncvlog -ams -use5x ./connect_lib/logic2elect.v  
(or ./ compileConnect instead)
```

3. Binding Cells for Simulation

In DFII window, create a new cell (**File>new>cell view**), as shown in Fig. 2.

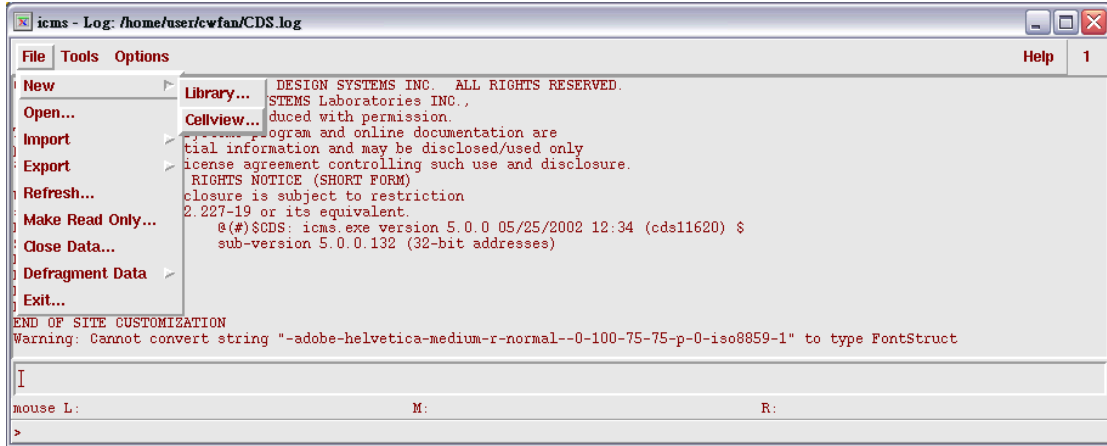


Fig.1 DFII window

Choose the **Tool** to **Hierarchy-Editor** and fill in the **Cell Name** blank with **PLL**.

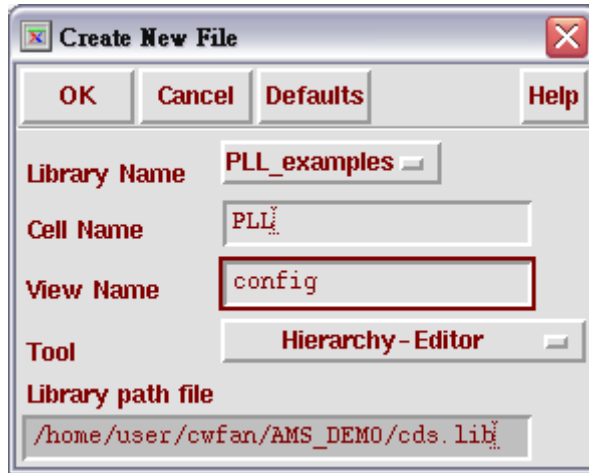


Fig.2 Create a config view cell

Click **Browse** button in New Configuration window

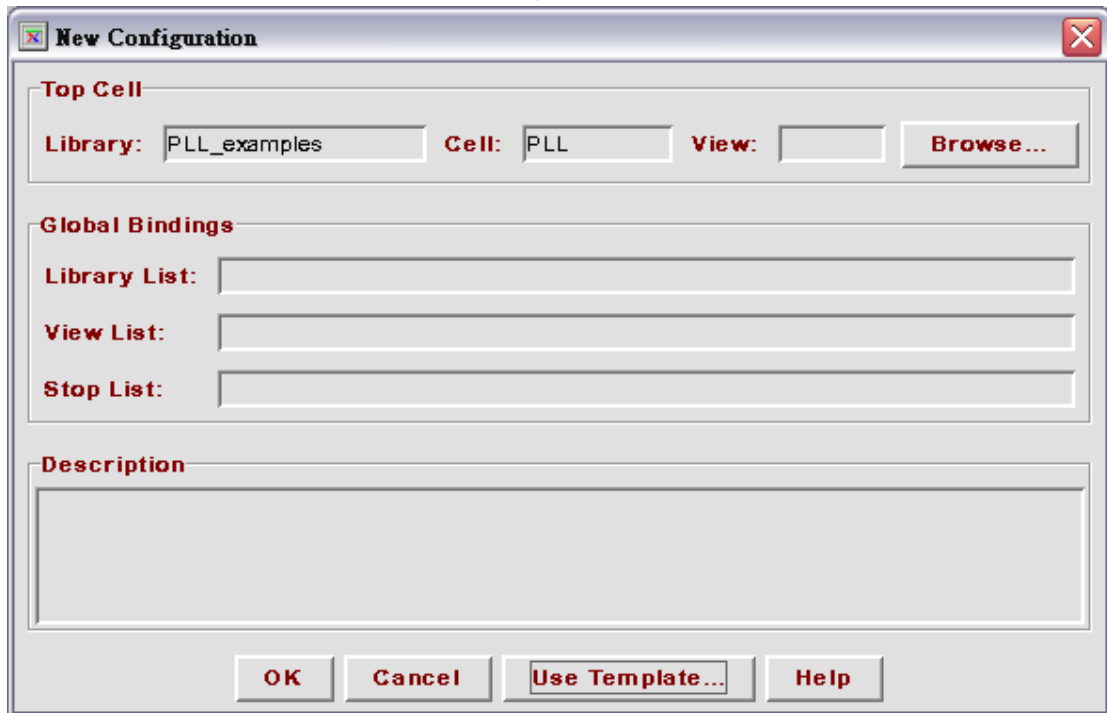


Fig. 3 New Configuration window

Select **PLL>schematic**

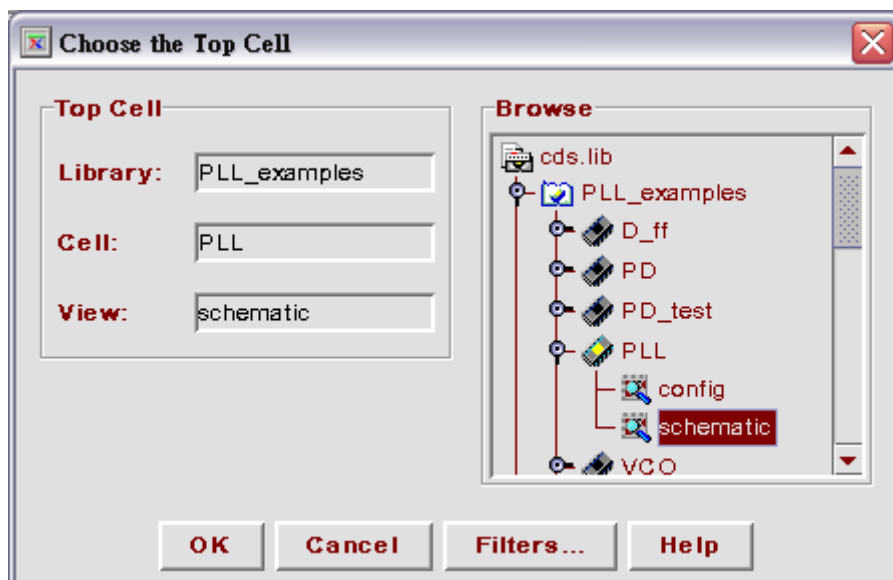


Fig. 4 Select a cell for simulation

Click **Use Template** button in New Configuration, select **Name** as **AMS** as shown in Fig. 5.



Fig. 5 Use Template window

Right click the **View Found**, and select each cell with the cell view shown in Fig. 6. The **View to Use** is the view used during simulation.

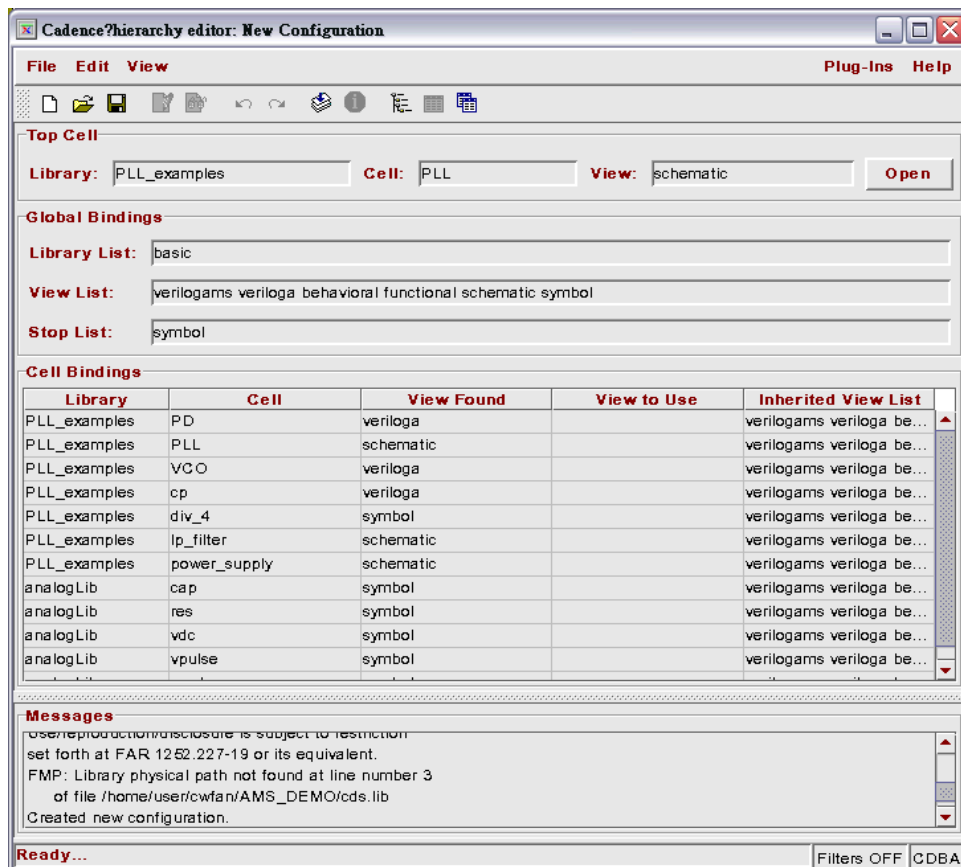


Fig. 6 Hierarchy-Editor

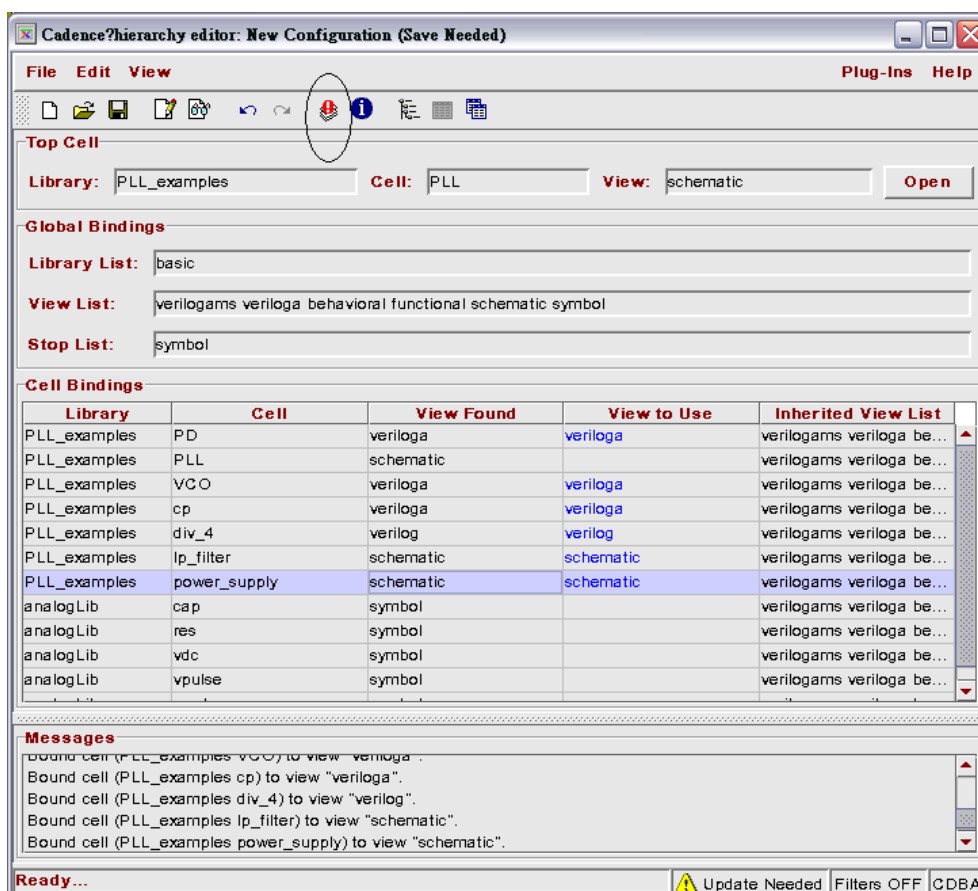


Fig. 7 Update the settings

Click on the **update** icon to save the settings.

4. Running AMS Designer

In the Hierarchy-Editor window, click on **Plug ins > ams**. The AMS toolbar menu will now appear towards the left on the menu bar as shown in Fig. 8.

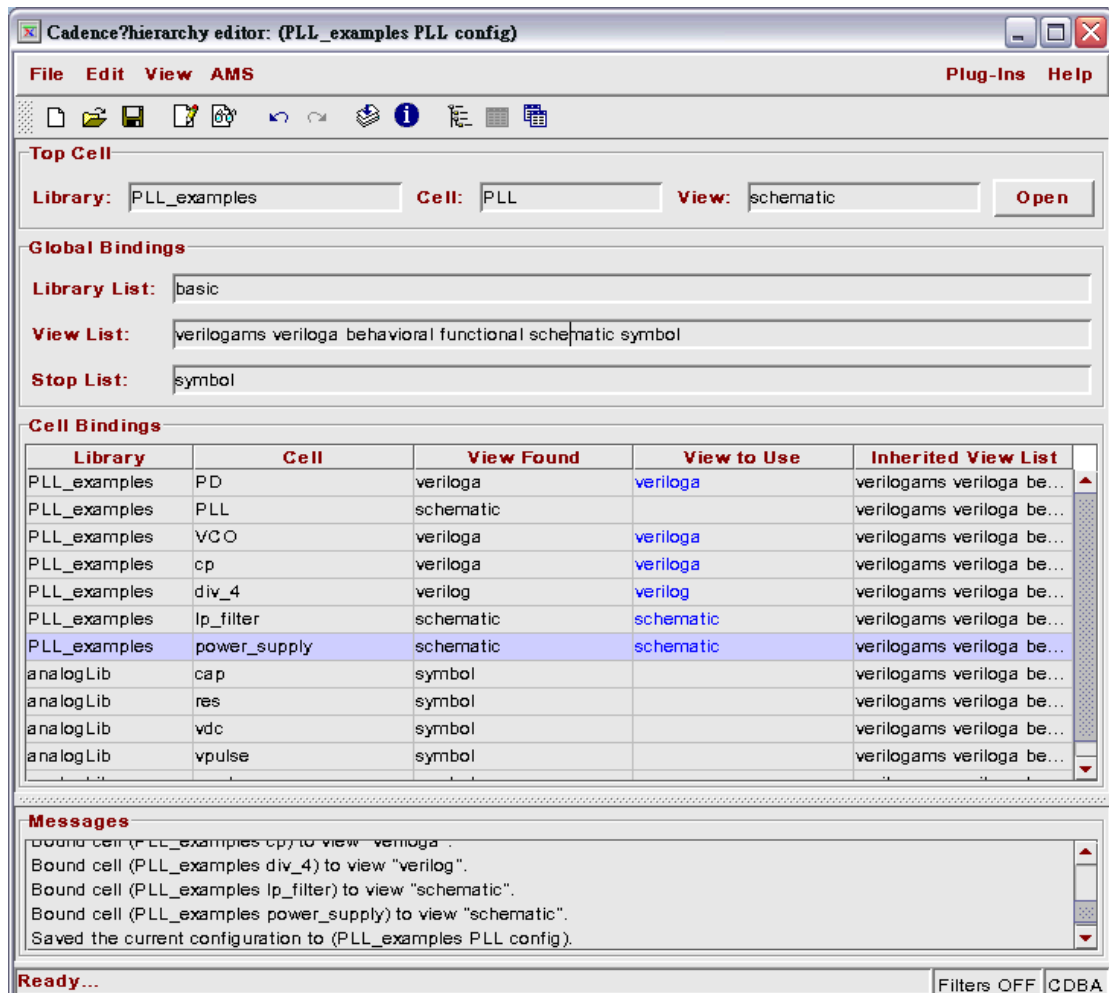


Fig. 8 Hierarchy-Editor

Click on the AMS menu > **Run Directory...**

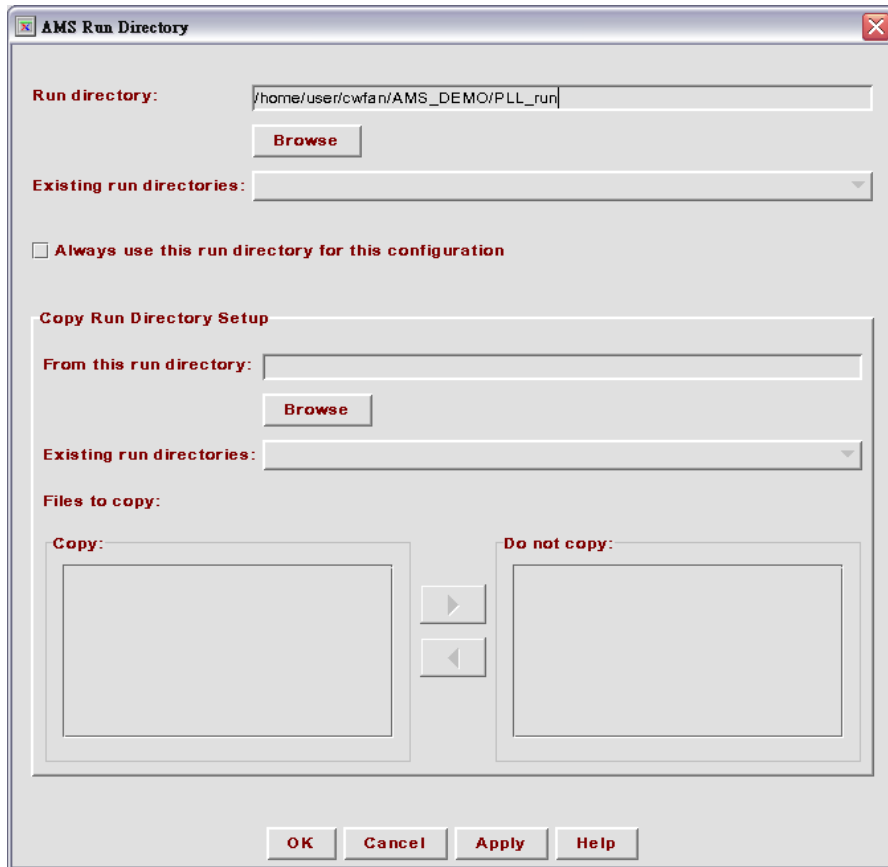


Fig. 9 AMS run directory

A default run directory appear as \$AMS_DEMO/ PLL_run, then click on OK.

Run directory will receive:

- simulation output files
- log files produced during simulation flow
- environment files related to form settings
- waveform data
- simulation control files
- SimVision script files

Pull down **AMS>Options>Compiler** in Hierarchy-Editor window. Use the Browse button under **hdl.var file**, select the *hdl.var* under AMS_DEMO directory.

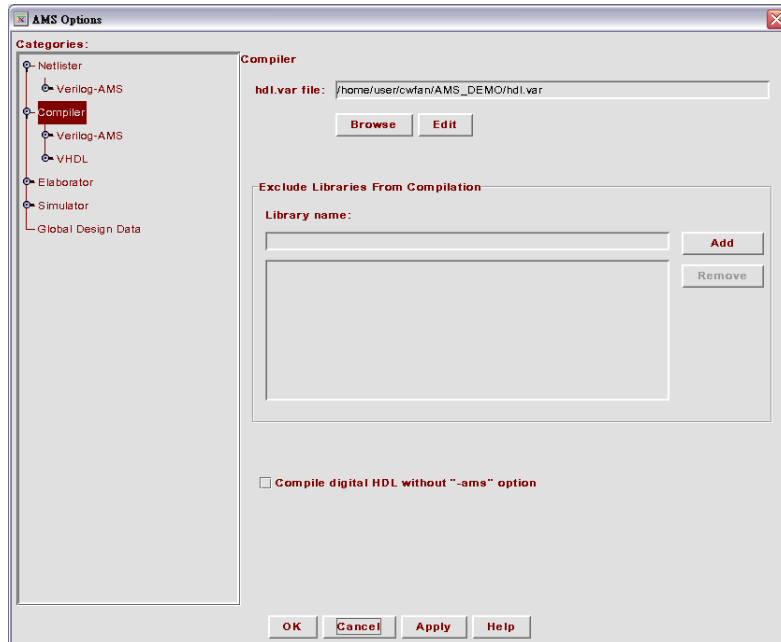


Fig. 10 AMS Options window

Click on **Elaborator** in AMS Option window, and modify it to **100ps/100ps**.

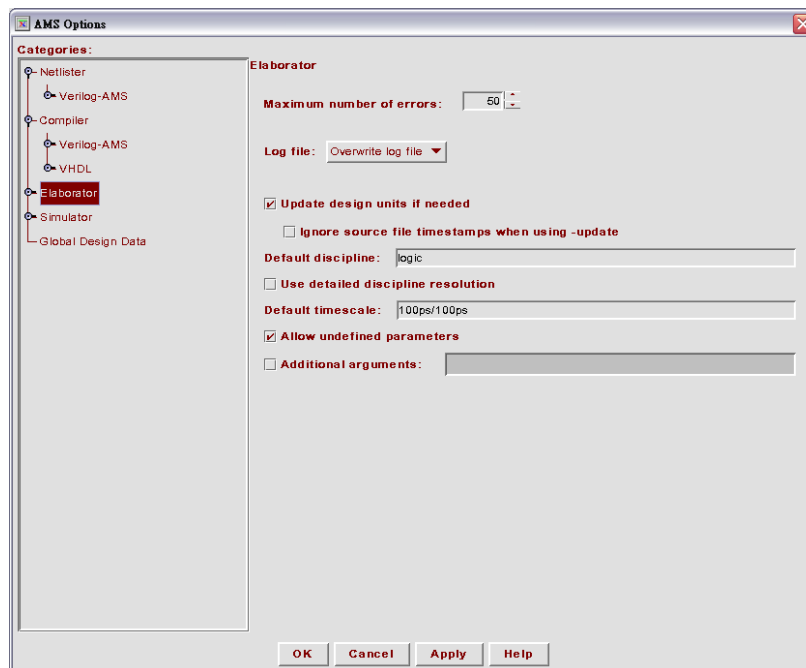


Fig. 11 Setting timescale

Click on **Simulator>Analog Solver>Tran Analysis**, enter 1u in the Stop time field.

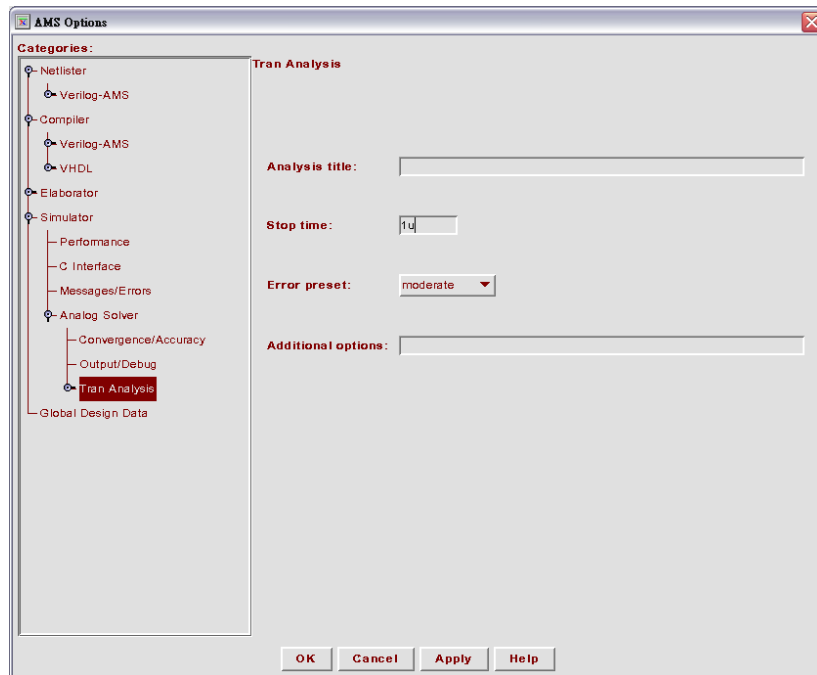


Fig. 12 Setting simulation time

Click on **Analog Solver>Tran Analysis>Convergence/Accuracy**
Modify **Maxstep** to **100p**.

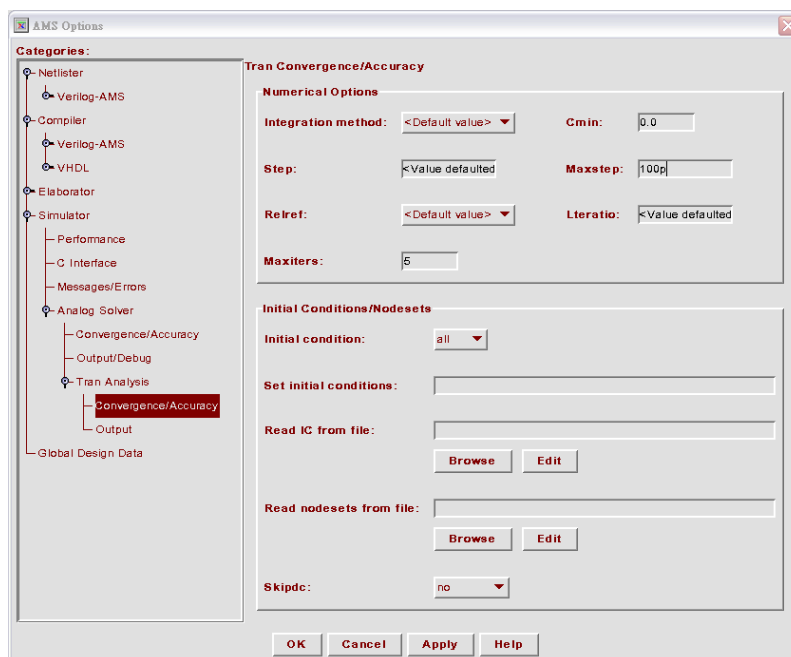


Fig. 13 Accuracy setting

Execute **AMS>Design Prep** in Hierarchy-Editor window, enable **Netlist - All** and **Compile - All** and then click **Run**.

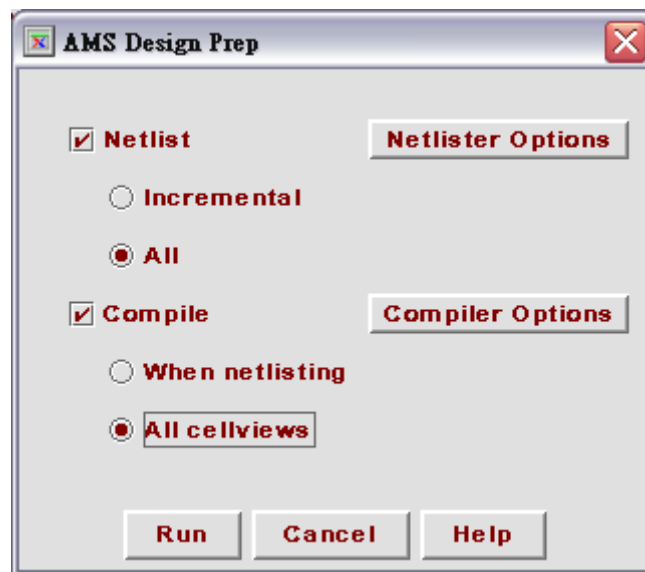


Fig. 14 AMS design Prep window

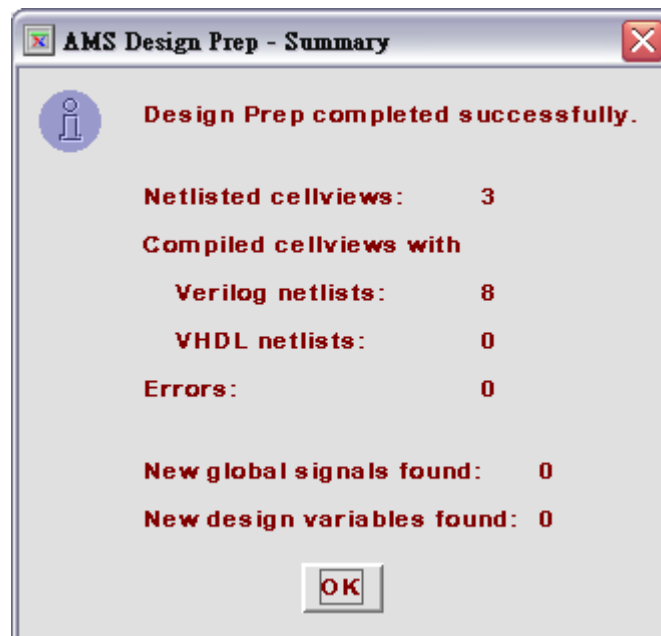


Fig. 15 AMS design Prep summary

When compiling completed, the Design Prep Summary message box appears.

Click on **AMS>Run Simulation** in Hierarchy-Editor window fill the blanks as show in Fig. 16.

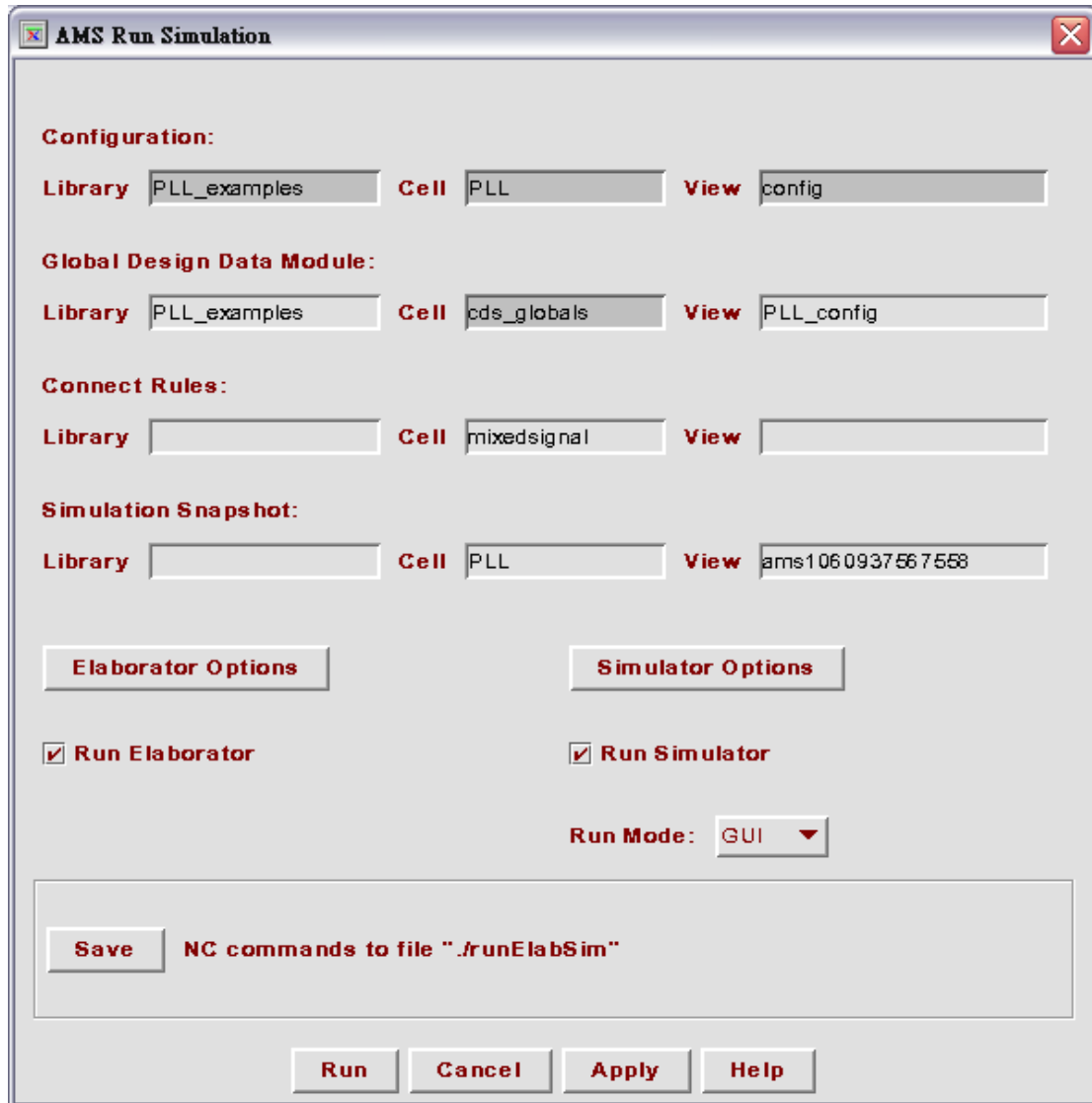


Fig. 16 AMS run simulation

When the Elaborator is finished, the Cadence AMS simulator window appears. Click on the **Navigator** icon to open the Navigator window.

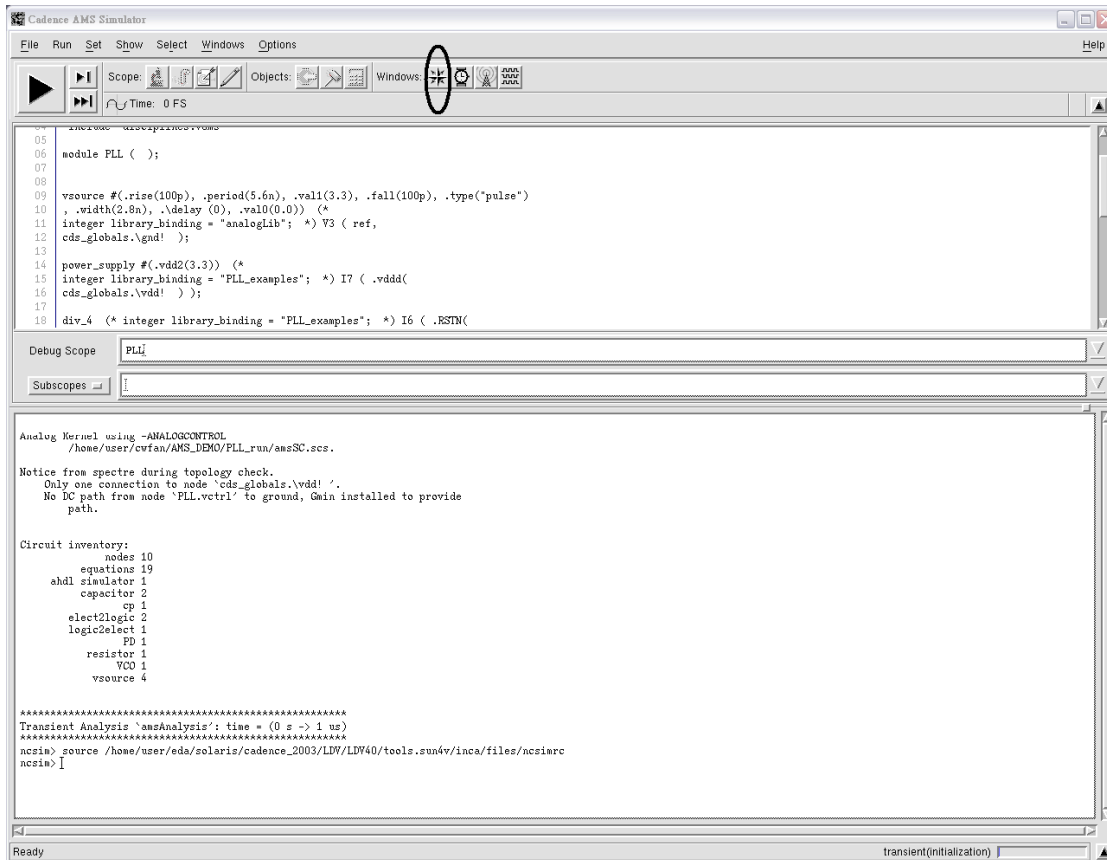


Fig. 17 AMS simulator window

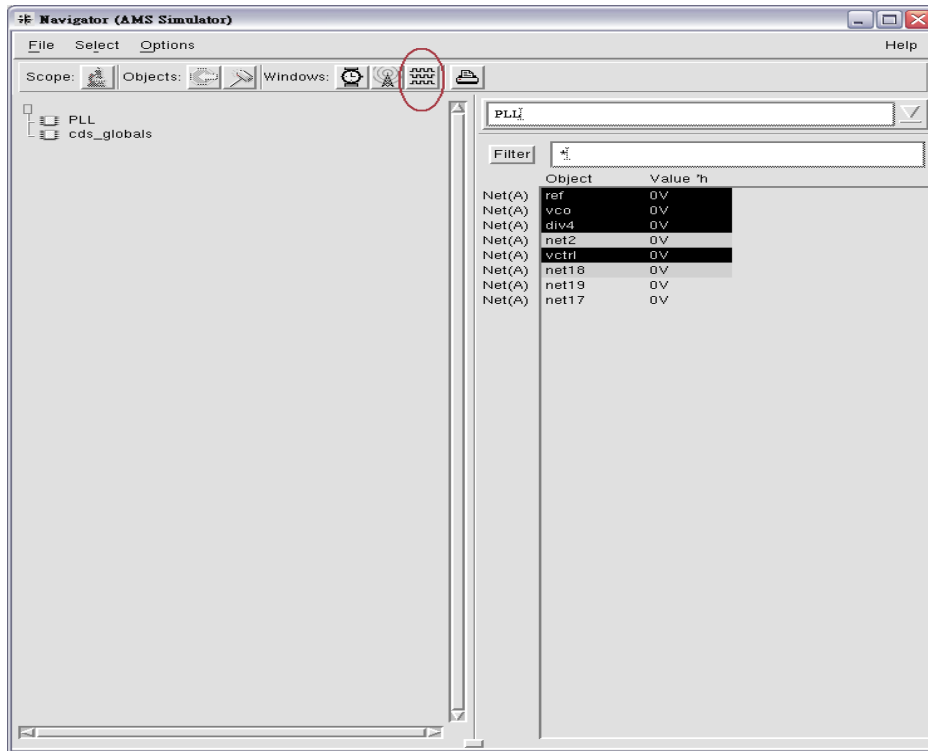


Fig. 18 Navigator window

Select signals you want to observe and click on the **Waveform View** icon, then SimVision window appears.

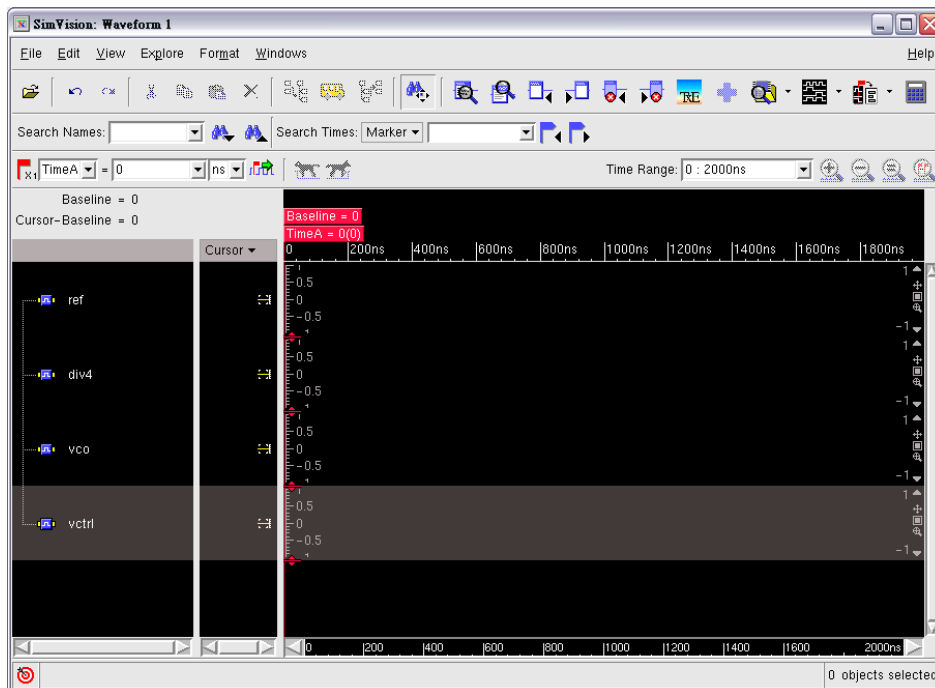


Fig. 19 SimVision window

Click on the **Run** button to start the simulation as show in Fig. 20.

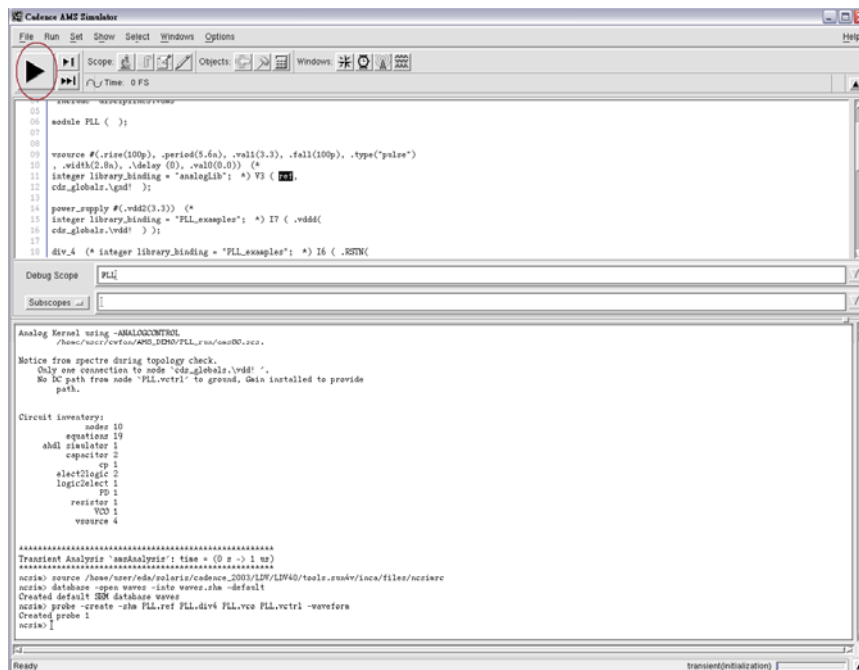


Fig. 20 Start simulation

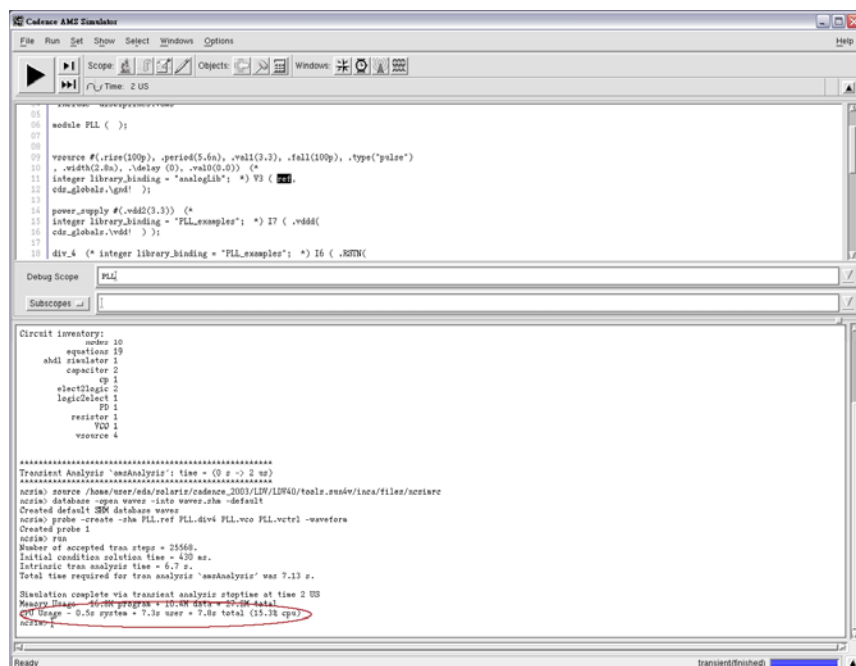


Fig. 21 Simulation complete

When simulation is completed, check the simulation time in the bottom of the AMS simulation window.

Back to Hierarchy Editor, and change PD, cp, VCO, div_4 to **schematic view**, **Run direction** to PLL_run2 and repeat these steps. Compare the simulation time difference.

Click on **File>Open Databas** in SimVision window and change the folder to PLL_run/waves.shm/waves.trn as show in Fig. 22.

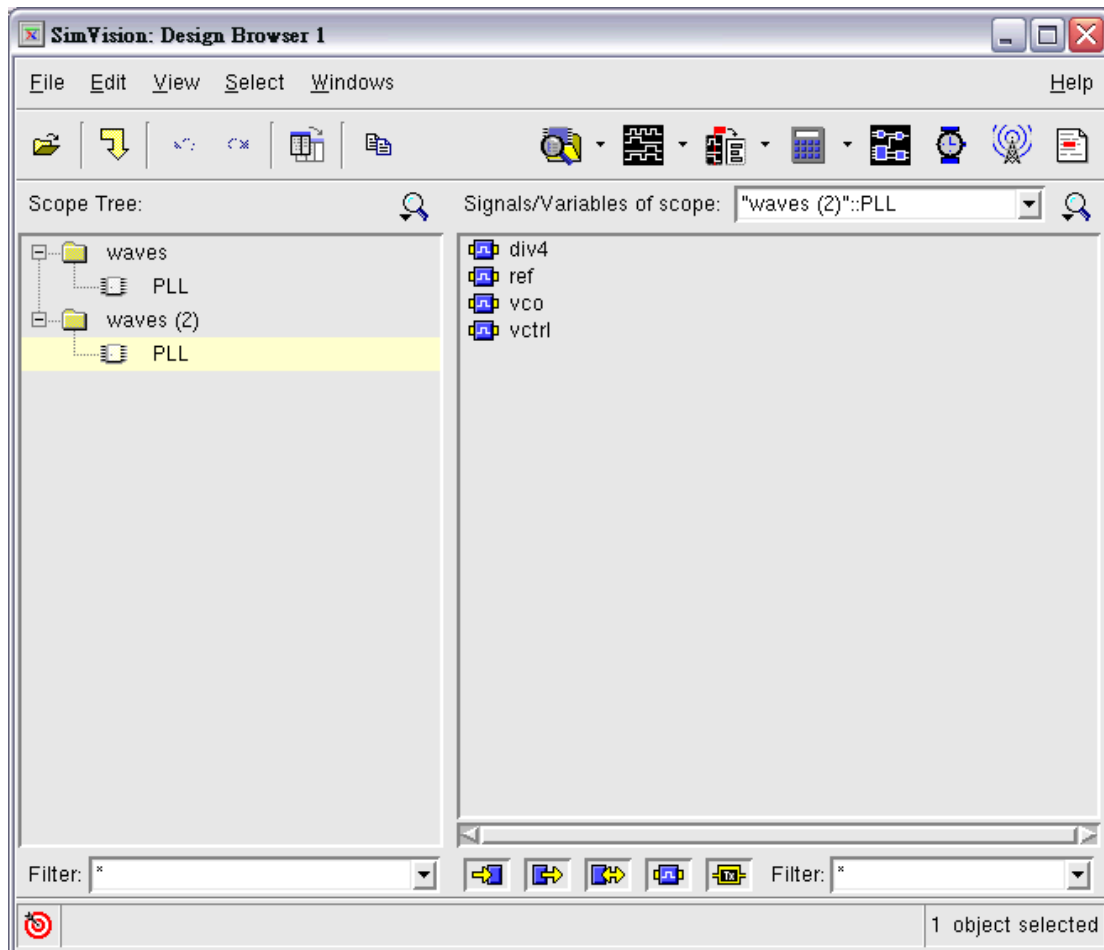


Fig. 22 SimVision design browser

Compare the waveform difference between two different simulations.