A CMOS 2.0-11.2 GHz UWB LNA Using Active Inductor Circuit

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Abstract—**A fully-active low-noise amplifier (LNA) for ultra-wideband application is presented. Passive on-chip inductor of conventional LNA design is replaced by low-noise active inductor, significantly reducing the total chip area of the proposed CMOS LNA. The core LNA circuit is a cascoded common-source amplifier loaded with an active inductor. Two buffer stages are used to provide the required input and output impedance matching. The amplifier is designed and simulated in 0.13-µm RF CMOS process. It exhibits a forward gain (S21) of 11.2 dB, a noise figure (NF) of 2.2-4.0 dB, and return losses (S11 and S22) of less than –10 dB over the frequency range of 2.0 to 11.2 GHz while consuming only 13.5mW from a power supply of 1.5 V. The proposed amplifier occupies 0.09mm^2 of chip area.**

I. INTRODUCTION

Ultra-Wideband (UWB) technology, a recently declassified short range wireless standard, have received great interest in academia and industry because of its capability of transmitting high data rate digital signal at very low power. As for other communication systems, CMOS is the technology of choice for low-cost system-on-chip (SOC) solution. One of the most important building block of UWB receiver is the low-noise amplifier needed immediately after antenna to boost the very limited received UWB signal power (we remind that PSD of transmitted signal should be not more than -41.3dBm per MHz at the distance of 3 m from antenna). It should exhibit a 50Ω input-output matching, a flat gain and a very low-noise figure over the entire bandwidth.

A number of UWB LNAs in CMOS processes have been reported in [1]-[5]. In these designs, on-chip passive inductors are used in the loads and input impedance matching circuits. To realize on-chip inductor in CMOS technology, the designer need to use several hundred micrometers of interconnects in a form of a rectangular or octagonal spiral. These on-chip passive inductors usually take up majority of the chip area of CMOS LNA. There are no inductorless LNAs operating in the range of 2-11.2 GHz. Moreover, some of the LNAs in [1]-[5] are not complete on-chip solutions, as they require external bias voltage(s) [1] or buffer amplifiers or both [5]. This requires large bypass capacitor at each bias point to suppress the noise, and increases the number of on-chip power pads.

In this paper, a novel fully-active UWB LNA is designed without any on-chip passive inductors. In the proposed amplifier, an active inductor circuit consisting of several transistors is used as the load for the cascoded common-source (CS) amplifier to realize the gain in the UWB bandwidth. This approach gives a very low chip area required for the amplifier. The reduction of power consumption was also pursued in the design. This dictated one gain-stage and separate buffers for output and feedback signals.

The proposed circuit is designed, simulated and implemented in UMC 0.13-µm RF CMOS process.

This paper is organized as follows. Section II presents the proposed UWB LNA. The design approach and circuit analysis is discussed in Section III. The design realization and simulation results are presented in Section IV. A brief conclusion is drawn in Section V.

II. LNA AND CIRCUIT DESCRIPTION

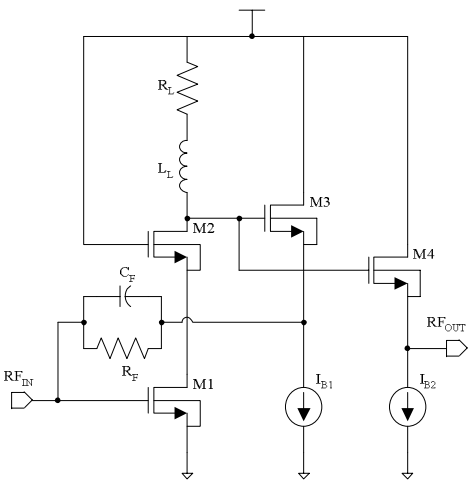


Fig.1 UWB LNA with passive inductor

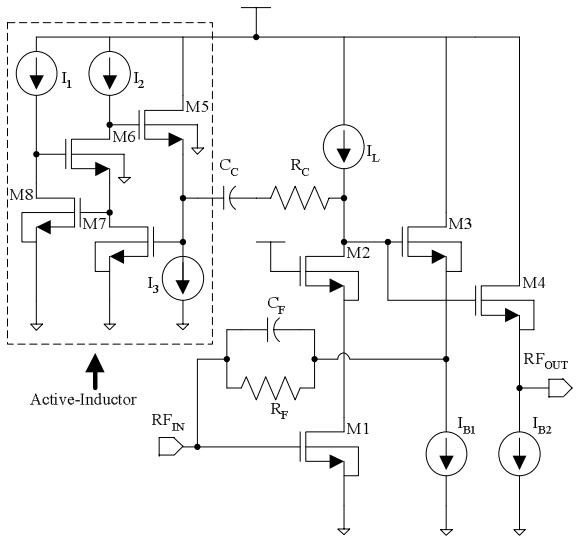


Fig.2 The proposed UWB LNA with active inductor

The idea of the proposed amplifier is shown in Fig. 1. It includes a cascode stage with passive inductor load, L_L and two parallel buffers. One buffer (M3, I_{B1}) is used to create a local parallel feedback (R_F, C_F). This gives the input impedance that is mostly defined by the feedback resistor R_F and the bias current I_{B1}, and can be adjusted by the capacitor C_F. This buffer also establishes the bias for M1 of the cascode stage. Another buffer (M4, I_{B2}) is providing the output signal. The output wideband matching is mostly achieved by adjusting I_{B2}. This buffer also boosts the gain of the overall loaded LNA. The design procedure shows that in the proposed circuit the input and output matching are practically independent.

The novelty of design is shown in Fig. 2 where active inductor circuit and the coupling circuit are replacing L_L. The resistance R_C controls damping in the series L_L, R_C, C_C circuit (see equivalent circuit shown below in Fig. 5) and helps to provide a more flat frequency response of the amplifier gain.

The cascode configuration, the most commonly used circuit topology for LNA, is used to reduce the Miller effect of the input device, M1, and to achieve the improved reverse isolation due to high output impedance at the drain of the cascoding device, M2. This configuration also allows one to have a good noise figure (NF). The complete circuit with all biasing networks is shown in Fig. 3.

III. Design Approach and Circuit Analysis

It is difficult to simultaneously satisfy all the requirements of UWB LNA. For most broadband amplifiers there is a severe trade-off [5] between input-impedance match and NF because for minimum NF, high input impedance Z_{in} of the amplifier is required whereas for maximum power transfer, Z_{in} needs to be matched with 50Ω. The preference is usually given to the maximum power transfer. Because of this trade off, most of the CMOS UWB LNAs show NF above 3dB when matched to 50Ω.

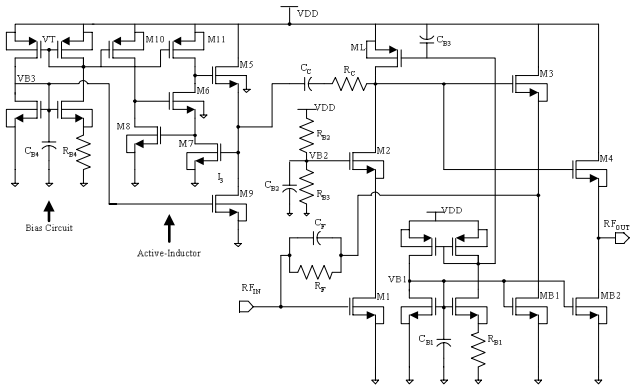


Fig.3 The complete on-chip proposed UWB LNA

A. Input Impedance Matching

As mentioned earlier, for maximum power transfer and least reflection, the input impedance of the first stage needs to be matched with source impedance R_S = 50Ω. This matching is achieved using the feedback network that consists of the resistance R_F and the output impedance of the source-follower. A small capacitance, C_F in parallel with R_F is used to suppress peaking.

B. Device Sizing in Cascode Stage

The cascoded stage provides a reasonably low (about 3 dB) noise figure. One relationship reducing NF should be mentioned. If the body effect is absent then the width of the cascoding transistor M2, should be chosen three times less (this ratio may slightly vary during simulations) than that of the input transistor M1. It is contrary to the common practice to use the devices of the same width. Yet, this ratio is well confirmed in experiments [6], and may be used when the transistors are in separate wells.

C. Active Inductor for UWB: Gain and Bandwidth

High-Q transistor-only active inductors in CMOS technology have been discussed in [7]-[8]. Using active inductor as the load, an LNA has been designed in [9] for narrowband frequency range. There the active inductor is used as a high-Q bandpass filter, and this solution is not suitable for UWB applications. Yet, this approach can be modified, and the design technique suitable for UWB is as following.

A simplified equivalent small-signal circuit of the active inductor is shown in Fig. 4.

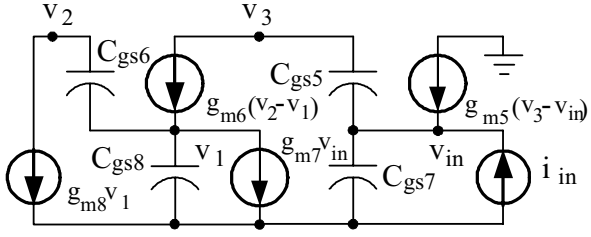


Fig. 4 Equivalent small-signal circuit of active inductor

First, one finds the input impedance, $z_{ain} = v_{in} / i_{in}$, of this circuit. The nodal analysis shows that z_{ain} is given by

$$z_{ain} = \frac{s}{C_{gs8}} \frac{(s^2 + \frac{C_{gs8}}{C_{gs7}}\omega_8 s + \frac{g_{m8}}{g_{m7}}\omega_7\omega_6)}{[s^4 + \omega_8 s^3 + \omega_8\omega_6 s^2 + \omega_7\omega_8\omega_6(s+\omega_5)]} \quad (1)$$

where $\omega_i = g_{mi} / C_{gsi}$ $(i = 5,6,7,8)$. At low frequencies this impedance may be approximated as $z_{ain}(j\omega_{low}) \approx j\omega C_{gs5} / (g_{m7} g_{m5}) = j\omega L_{oe}$, and is inductive. At high frequencies it is approximated as $z_{ain}(j\omega_{high}) \approx -1/(C_{gs8}\omega) = -1/(C_{oe}\omega)$, and is capacitive. These properties of z_{ain} frequency response are well known in simulations [8]. Using them one tries to reduce (1) to the input impedance of a simple parallel *RLC*-circuit. Indeed, if one represents z_{ain} as

$$z_{ain} = \frac{s}{C_{gs8}} \frac{(s^2 + \frac{C_{gs8}}{C_{gs7}}\omega_8 s + \frac{g_{m8}}{g_{m7}}\omega_7\omega_6)}{(s^2 + \frac{\omega_p}{Q}s + {\omega_p}^2)(s^2 + a_1 s + a_0)} \quad (2)$$

and finds the coefficients a_1 and a_0 in such a way (some tries and comparison with prepared templates is necessary) that the ratio

$$K(s) = \frac{(s^2 + \frac{C_{gs8}}{C_{gs7}}\omega_3 s + \frac{g_{m8}}{g_{m7}}\omega_7\omega_6)}{(s^2 + a_1 s + a_0)} \approx K \quad (3)$$

is nearly constant in the vicinity of $\omega_p = \sqrt{(g_{m7} g_{m5}) / (C_{gs7} C_{gs8})}$. Then z_{ain} can be approximated as

$$z_{ain} \approx \frac{Ks}{(s^2 + \frac{\omega_p}{Q}s + {\omega_p}^2)} \quad (4)$$

and is represented as in Fig. 5.

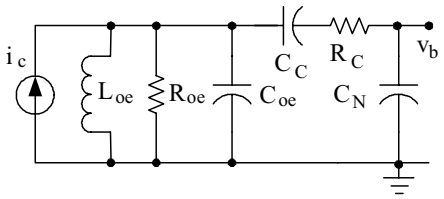


Fig. 5 Active inductor circuit and inter-stage circuit

This part of the design procedure may be done using MATLAB, and it will define the approximate value of *Q*. After that one can find the transconductances and the sizes of transistors in active inductor. The obtained values of L_{oe}, C_{oe} and *Q* can be now calculated. Then the required reduction of *Q*-factor and the bandwidth increase may be achieved by control of R_C (this can be done directly in Cadence design system). Switching between these two design tools one finds an optimal solution.

D. Output Impedance Matching

The achievable maximum power gain also depends on the output impedance matching. In the proposed circuit, a buffer provides a 50Ω match over the entire bandwidth. The gain of the source follower is always less than 0dB, and it reduces the overall gain of the LNA while slightly increasing NF. However, this is the simplest solution because the output impedance is defined by $1/g_m$. Hence, to match 50 Ω loads, transconductance g_{m4} (M4) needs to be about 20 milliohm^{-1}, and the optimization is achieved in simulation varying this device size and its biasing current.

IV. DESIGN REALIZATION AND SIMULATION

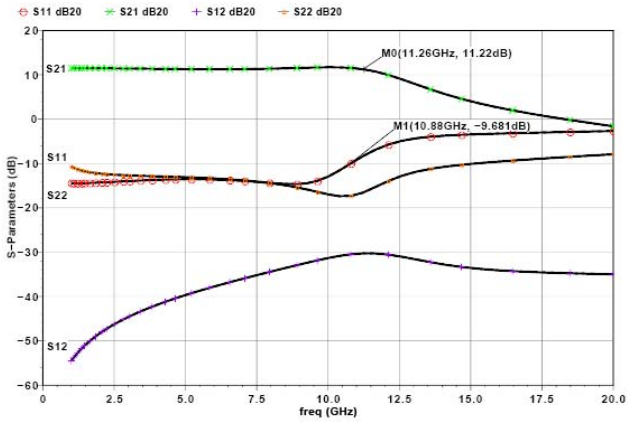
The proposed UWB LNA is designed and implemented in UMC 0.13-µm RF CMOS process.

The input transistor, M1 is sized to provide 4mA current to achieve required gain. The feedback resistor R_F in parallel with a small compensation capacitor, C_F for flat frequency response provides input matching at the cost of gain. The bias voltage *VB1* is set to 540mV to provide 2.7mA current through the output buffer amplifier (M4, MB2) to meet the condition of g_m = 20 miliohm^{-1} for output impedance 50Ω. A reasonable size MOS capacitor is used as the bypass capacitors (C_{B1}-C_{B5}) to filter out noise effect at the bias nodes. We also tried to reduce current in active inductor circuit.

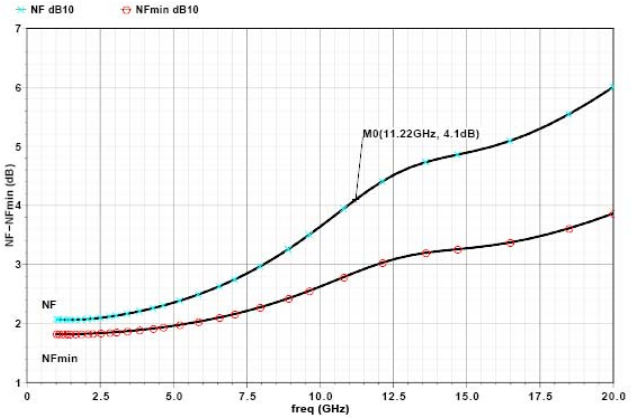
The transistor sizes are: M1(*W/L*) =150µm/0.13µm, M2(*W/L*) =50µm/0.12µm, ML*(W/L)* =60µm/0.12µm, M3(*W/L*) =10µm/0.12µm, MB1 (*W/L*) =10µm/0.12µm, M4(*W/L*) =60µm/0.12µm, MB2(*W/L*) =30µm/0.12µm, M5, M6, M8, M9=2.5µm/0.12µm, M7=12µm/0.12µm, M10-M11= 2µm/0.12µm. The approximate values of M5 to M8 are obtained from the previous analysis. The resistors are: R_F =225Ω, R_C=200Ω, R_{B1}=2.7KΩ, R_{B2}=4.0kΩ, R_{B3}=16kΩ, R_{B4}=2.9kΩ. The capacitances are C_C = 3.2pF, C_F = 50fF, C_{B1}-C_{B5} (MOSFET capacitors) =2.5pF. The bias voltages are: VB1= 535mV, VB2= 723mV and VT= 771mV.

The post-layout pad-to-pad simulations were performed in a 50-ohm system (R_S =50Ω and R_L=50Ω) with supply voltage of 1.5V, for forward and reverse gain (S21, S12), input and output return loss (S11, S22), and NF. The simulation results are given in Fig. 6. The forward gain shows 11.2 dB flat response, NF varies from 2.2 dB minimum to 4.0 dB maximum for the frequency 2.0 GHz to 11.2 GHz. S11 and S22 are less than -10 dB over the frequency spectrum of 2.0 to 11.2 GHz. Table 1 summarizes the performance of the proposed LNA and compares it with that of those in recent publications. Our circuit has higher power consumption than the circuits in [1]-[3], but has very low chip area as no passive inductors being used, and no external bias voltages are required.

The layout of the proposed LNA is shown in Fig.7. The core-chip occupies an area of 0.025mm^2 (180µm x 140µm). The overall real-estate of the chip including all the pads is 0.09mm^2 (350µm x 250µm).



(a)



(b)

Fig. 6 Simulated performance: (a) S-parameters (b) noise figure

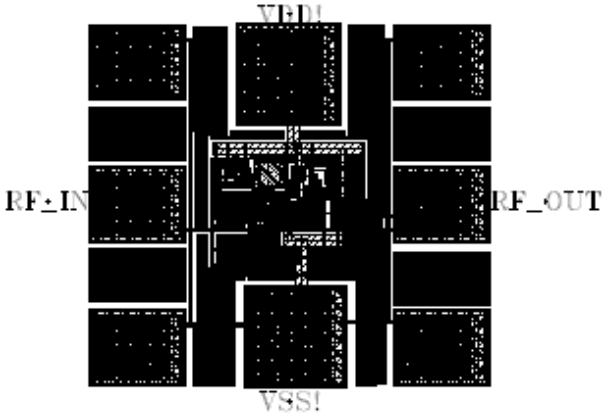


Fig. 7 Layout of the proposed UWB LNA

V. CONCLUSION

A new ultra-wideband LNA exhibiting a bandwidth of 2.0-11.2 GHz frequency range has been designed without using any passive area-inefficient on-chip inductors. A wideband active inductor is designed to replace passive on-chip inductor over the entire UWB spectrum. The amplifier does not need any external bias circuits, and uses only one DC supply. The proposed circuit is fully integrated on-chip and has a very low chip area of 0.09mm^2. This is the main advantage of the replacement. The noise figure is 2.2-4 dB. One may also expect that the NF obtained in measurements will be about 1 dB worse than in simulations. Another possible disadvantage may be wider spread performance characteristics: the amplifier is using the capacitances of active devices which have wider spread of values in comparison with that of the big inductances.

VI. REFERENCES

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Table-1: Performance summary and comparison

Ref.	Tech. (CMOS)	$S21_{min\text{-}max}$ (dB)	S11 (dB)	S22 (dB)	$NF_{min\text{-}max}$ (dB)	VDD (V)	Power (mW)	Chip Area (mm^2)
[1]	0.18µm	9.0-10.5	< -7.0	< -10	1.5-5.5	1.2	4.5	0.82
[2]	0.18µm	11.0-11.5	< -9.3	< -14	3.4-4.8	1.5	6.2	0.80
[3]	0.18µm	10.8-12.0	< -11.0	<-18.5	4.7~5.6	1.5	10.57	0.665
[4]	0.18µm	9.7	<-12.0	<-14.5	3-5.1	1.8	20	0.59
[This work]	0.13µm	11.2	< -10	< -14	2.0-4.0	1.5	13.5	0.09