# A CMOS 6-bit, 1 GHz ADC for IF Sampling Applications

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*Abstract* — **The design plan and measurement results of a very high speed 6-bit CMOS Flash Analog-to-digital converter (ADC) are presented. The very high acquisition speed is obtained by improved comparator design and optimized pre-amplifier design. At these high frequencies power-efficient error correction logic is necessary. Measurements show the high conversion speed of the ADC. Maximum acquisition speed is above 1 GHz.**

## I. INTRODUCTION

Analog-to-digital conversion and digital-to-analog conversion lie at the heart of modern signal processing systems where digital circuitry performs the bulk of the complex signal manipulation.

Applications such as IF sampling, fast Ethernet require ADC's with sampling rates in the order of 500 MHz and relatively low resolutions [3,6]. To reduce the cost of the "system-on-chip" the choice of technology is dictated by the digital technology, which is nowadays CMOS.

Not only the sampling speed is rising, also the maximum input frequency which has to be converted increases. Therefore, bandwidth-, distortion- and error rate-specifications are of utmost importance. Error rate is an aspect in the design of high-speed ADC's which is often overlooked or underestimated. When the error rate is extremely high, the digitized waveform appears to disintegrate and the Signal-to-Noise Ratio (SNR) deteriorates rapidly. Since the error rate increases exponentially with the acquisition frequency, the meta-stability errors might increase by orders of magnitude for very high-speed converters. Therefore, to achieve a good performance at high frequencies the problem of meta-stability must be tackled.

## II. ADC ARCHITECTURE

At these very-high conversion rates (> 500MHz), the only practical architecture to date is the flash ADC [2,3]. The implemented flash ADC, shown in figure 1, is not preceded by a sample-and-hold. As a consequence both the quantization and sampling is done in the comparator. To reduce the input-referred offset of the clocked comparator, a preamplifier is used in front of the comparator. The thermometer code produced by the comparators is processed by the digital error correction

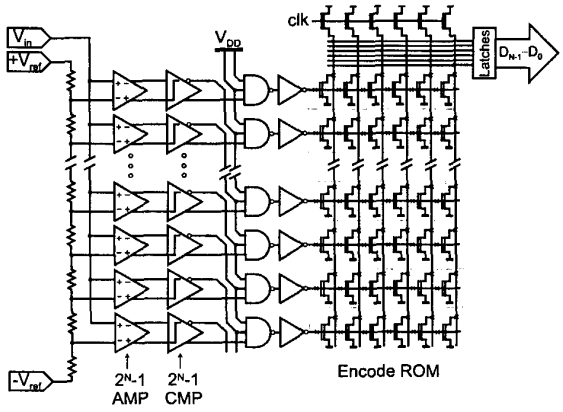


Figure 1: Flash ADC Architecture

logic before the thermometer-to-binary conversion is done by a pre-charged ROM with optimized pull-down transistors. The ROM outputs are held for a whole clock period with a high speed TSPC (True Single Phase Clocked) flip-flop and are brought off-chip by output-buffers.

## III. BUILDING BLOCKS

### A. ADC Front-end Circuitry

The comparator is the most critical block to achieve the very high acquisition speed. The regenerative comparator is preceded by a preamplifier to reduce the input referred offset of the comparator. The gain of the preamplifier is made small to achieve the high bandwidth requirement. This high bandwidth demand is necessary because of the signal dependent delay of the pre-amplifiers [1,4]. A formula has been derived in [1] for the third order distortion, due to this delay, as a function of the internal poles of preamplifier stages. Although the given formulas were derived for bipolar pre-amplifiers, similar equations can be derived for CMOS amplifier stages. The results of



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these calculations are depicted in Fig. 2 where the third order distortion is given as a function of the ratio [Pre-amplifier bandwidth/Input Frequency] and the $V_{gs}$-$V_t$ of the transistors of the pre-amplifier.

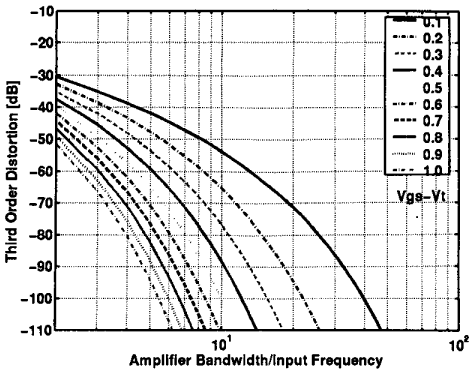


Figure 2: Third order Distortion due to Signal Dependent Delay as a function of $V_{gs}$-$V_t$ and ratio

In this design, a $V_{gs}$-$V_t$ of 0.3 V was chosen, resulting in a [Preamplifier Bandwidth/Input Frequency] ratio of 3. This means that for a sampling speed of 1GS/s (Nyquist rate 500 MHz), the internal poles of the pre-amplifier should be located above 1500MHz, in order to have e.g. 50dB third order distortion (≫ 6-bit).

The preamplifier is an optimized differential pair with resistive loads. The schematic of the comparator is shown

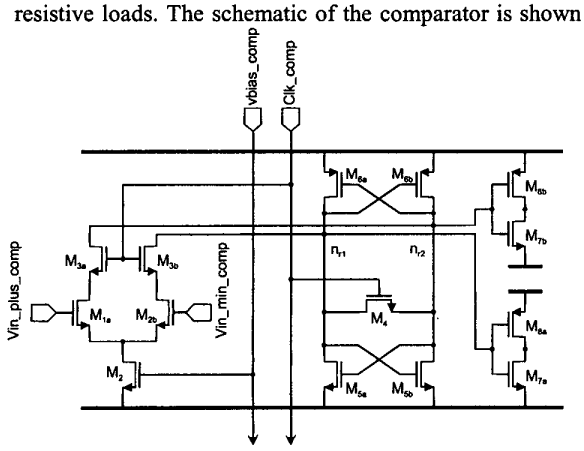


Figure 3: Comparator Schematic

in figure 3. The output of the preamplifier is converted into a current difference by *M1-M2*, which steers the regenerative latch. This latch is a cross coupling of two inverters to achieve the high conversion rate.

When the clock is high, the comparator is reset: the switch transistor *M4* is closed, short circuiting the regeneration nodes $n_{r1}$ and $n_{r2}$. During the same clock phase, the clocked differential pair *M2-M3* injects a current imbalance in the regeneration nodes $n_{r1}$ and $n_{r2}$ proportional to the pre-amplifier output signal.

In the next clock phase (when the clock is low), the voltage imbalance that exists between the two regeneration nodes is amplified to digital levels by the NMOS and PMOS regeneration loops. The clocked differential pair *M2-M3* is disconnected from the preamplifiers in this phase as the clocking transistors *M3* are switched off. Hereby the kick-back noise is reduced and will not deteriorate the targeted specifications.

The speed of the latch is governed by a positive pole given by:

$$p_{reg} \approx \frac{g_{m_5} + g_{m_6}}{C_{GS_5} + C_{GS_6} + C_{DB_5} + C_{DB_6} + C_{DB_3}} \quad (1)$$

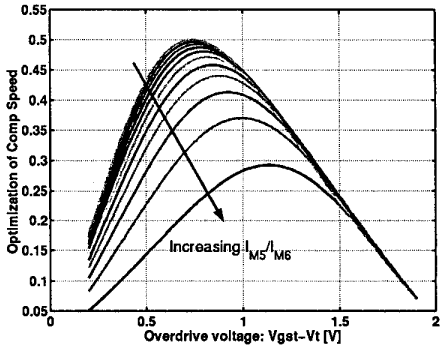


Figure 4: Optimization of Regeneration Speed

To achieve the very high acquisition speed of the converter this expression can be maximized (for a certain technology) as a function of the gate-overdrive voltage of the transistor M5 and the ratio $I_{M5}/I_{M6}$ as shown in figure 4. The clocked transistor M4 is used to have a reset phase after each decision (eliminate hysteresis). The outputs of the comparator are buffered by two invertors.

### *B. Error Correction Circuitry*

As stated in the beginning of this article, error correction is very important to achieve a good resolution at high input frequencies. The purpose of the digital backend is to convert the comparator outputs into a 6-bit code word and to reduce or eliminate the effects of errors in the comparators. Under perfect conditions, all comparator outputs below the input level are one the others are zero (thermometer code). Under such conditions, the thermometer code can easily be converted into a binary

code by transforming this code in a 1-of-n code followed by a ROM with a binary pattern. A flash converter with this type of structure typically suffers from two problems: bubbles (or sparkles) in the thermometer code and meta-stability [2][3][5].

*a. Bubbles*

Timing differences between the clock lines and signal lines can cause the effective sampling moments between comparators to be different. This can cause a bubble in the thermometer code where a one may be found among zeros or vice versa. A number of circuit techniques are used to suppress these bubbles. These techniques fall into three categories: preventing bubbles from occurring, preventing it from propagating towards the ROM and choosing a ROM coding scheme to minimize the resulting error at the ADC output (if the bubble still propagates). Therefore the comparators-layout is done very carefully to minimize the clock-skew (reduces first category). Secondly, a three-input NAND-gate is used after the comparators to prevent a bubble from propagating to the output and thirdly a Gray-encoded ROM is used to minimize the error at the output (see figure 1).

*b. Metastability Error Reduction*

Meta-stability in a flash converter can occur when the applied input signal is very close to one of the reference voltages. In this case, the comparator might be unable to toggle to a valid logic level. Therefore, the logic gates driven by this comparator output might interpret the input as different levels. As a consequence, zero, one or two ROM-lines might be selected leading to severe errors in the digital output code. At the end of the regeneration phase, the comparator output can be approximated by an expression of form:

$$V_{OUT} = (V_{IN} - V_{REF}).A.\exp(p_{reg}.T/2) \qquad (2)$$

with $A$ the gain of the comparator and $T$ the clock period. Therefore, the most effective way of reducing the meta-stability errors is to increase the regenerative pole. Although this provides an efficient way to reduce the error rate, other approaches can be used to reduce the meta-stability errors even further and to make the converter degrade smoothly in the presence of an error.

One possible approach consists in introducing pipelined latches immediately after the comparator outputs and before the logic decoder, increasing the regeneration gain of the comparator. However, each pipeline stage needs $2^n - 1$ latches, increasing the die area and the power consumption. An other approach consists of using Gray-encoded ROM's, which is an effective solution to reduce the effect of meta-stability errors provided that the case of having no lines selected is eliminated by design. This will be shown now. Figure 5 shows the comparison between a binary-encoded ROM and a Gray-encoded ROM in the case of a meta-stable state.

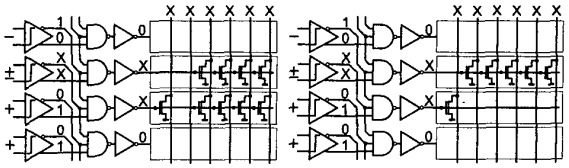

Figure 5: Error Propagation in Gray / Binary Encoded ROM

The output of the ROM is the logic OR-function of the two lines (if both X are one). In the case of the binary ROM, this leads to severe output errors and degradation in the SNDR of the converter. With a Gray-encoded ROM only one bit is wrong and this can be digitally recovered. However, if none of the ROM lines is selected, the Gray-ROM output bits are all one since they are determined by the ROM pull-up network, leading to a large error in the output code. It can be concluded from the previous discussion that a Gray-encoded ROM is an effective solution to reduce the meta-stability errors caused by an undecided comparator if the case of having no lines selected is eliminated by design [5]. In this design, this is guaranteed by putting two CMOS inverters at the output of the comparator (see figure 6, detail of figure 3). The ratio between the size of the PMOS and NMOS transistors used in this inverters has been made larger than the ratio between the size of PMOS and NMOS transistors used in the regenerative comparator. Consequently, the threshold

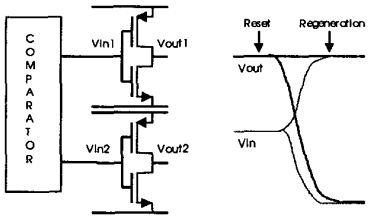


Figure 6: Avoiding meta-stability errors with a circuit that ensures one logic level and its corresponding signals

voltage of the inverters is higher than the threshold voltage of the comparator. This means that when the comparator remains undecided, the outputs of the comparator are at the meta-stable state and therefore the output of the inverters is a logic one.

After the error correction circuitry, only one output is high. This output is applied to the ROM to generate the digital output code. The pre-charged ROM has been layouted by hand to minimize the parasitic capacitance of the output ROM-lines. The ROM is Gray encoded to have a smooth performance role-off in the case a comparator error occurs.

## IV. LAYOUT

For the layout of the ROM special attention has been paid to the pull-down transistors. The drain-area of the ROM

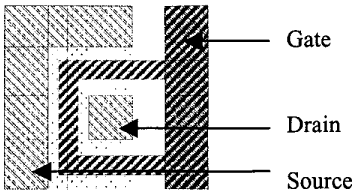


Figure 7: Rom Pull Down Transistor

transistors has been minimized to reduce the load of the ROM pull-up network. The transistors are routed around the drain-contact, so that each drain-area is equal to one contact area (smallest possible drain capacitance).

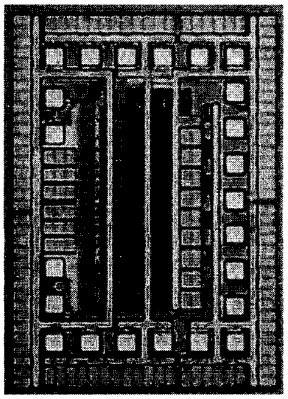

Figure 8: Chip Photograph

## IV. MEASUREMENTS

The ADC occupies only 0.8 $mm^2$ active area in a 0.35 µm digital SPTM CMOS process and is shown in figure 8. The converter consumes 240mA from a 3.3V power supply. Figure 9 shows the measured SNDR (Signal to Noise plus Distortion) of the converter as a function of the conversion speed with an input frequency of 183 kHz. The SNDR of the converter is higher than 30 dB with sampling speed up to 800 MS/s. The maximum sampling speed is

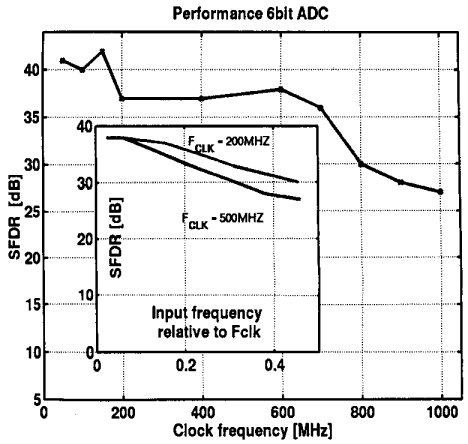


Figure 9: Measurement Results

higher than 1GHz. Figure 9 also shows the measured SFDR (Spurious Free Dynamic Range) of the converter as a function of the input frequency with sampling frequency of 200 MHz and 500 MHz.

## V. CONCLUSION

This paper clearly shows that sampling speeds above 1GHz can be achieved in CMOS technology for low-resolution analog-to-digital converters. Improved comparator and pre-amplifier design and careful layout is necessary to achieve the high acquisition speed.

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