**Saweth HONGPRASIT, Worawat SA-NGIAMVIBOOL, Apinan AURASOPON**

Mahasarakham University

# Design of Bandgap Core and Startup Circuits for All CMOS Bandgap Voltage Reference

***Abstract***. *This paper proposes a new self-biased op-amp's startup circuit design and improved bandgap core circuit for all CMOS bandgap voltage reference (BGR). In a conventional BGR circuit, the startup circuit may be designed either be required an external power on reset signal (POR) or composed of several MOS transistors for generating bias current and the bandgap core circuits has two nodes that are controlled currents and voltages by resistors of the same value. The new startup circuit presented here is designed by using only one NMOS transistor with circuit solutions suitable for low supply-voltage operation and achieved the correct bias point stability at the power on and the bandgap core circuit is defined the currents and voltages only one node which can be controlled by input voltages definition of op-amp are equalized for reducing the number of resistor. The simulation results indicate reference voltage of about 500.2 mV, temperature coefficient(TC) of 5ppm/◦C, which can be successfully operated with a minimum power supply of 1.2V at a temperature of 0-100◦C and a total power dissipation of 10.7 $\mu$W at room temperature.*

***Streszczenie.*** *W artykule zaproponowano nowe możliwości projektowania CMOS pasmowych wzorców napięcia. W obwodach konwencjonalnych wymaga ne jest użycie zewnętrznego sygnału resetu albo użycie kilku tranzystorów MOS generujących prąd polaryzacji. W nowej koncepcji wykorzystywane są tylko tranzystory NMOS co umożliwia pracę przy niskim napięciu zasilającym. (**Projektowanie pasmowego rdzenia i obwodu startowego pasmowych źródeł napięcia referencyjnego**)*

**Keywords:** Band gap voltage reference, BGR, CMOS, POR.
**Słowa kluczowe:** napięcie referrencyjne, CMOS..

## Introduction

Reference voltage generators are extensively used in many applications of analog and digital circuits such as A/D, D/A, DRAM and flash memories. The low-power and low-voltage operations are increasingly in demand for battery-operated portable devices. The output generators are designed to stabilize over supply voltage, process and temperature variations. Bandgap voltage reference is a reference voltage generator that can successfully achieve these requirements. However, in the conventional implementation of bandgap voltage reference [1], it generates an output voltage equal to the silicon energy gap voltage of around 1.25V, measured in electron volts. Its fixed output reference voltage, limited the low supply voltage and not suitable for low supply voltage operation. It cannot be used in the latest deep-submicron technologies. In the past, the start up circuits design methodology for BGR circuits, was designed either be required an external power on reset signal (POR) [2], or to be composed of several MOS transistors for generating bias current [3-5], and the bandgap core circuit has two nodes that are controlled currents and voltages by resistors of the same value for generating the CTAT and PTAT currents [1-6]. Therefore, this paper presents the all CMOS bandgap voltage reference circuit which is designed with a new startup circuit for self - biased op-amp by using only one NMOS transistor and the bandgap core circuit is designed by defining the current and voltage with only one node and another node set equal voltage which can be controlled by input voltages of op-amp. This method is able to reduce number of the resistor with a circuit solutions suitable for low supply voltage operation and achieve the correct biased point at power on and successfully operate with near 1V supply voltage.

## Working principle of Bandgap Voltage Reference circuit

The principle of a bandgap voltage reference can be illustrated by fig.1. The voltage across the base-emitter $(V_{BE})$ of bipolar junction transistor (BJT) has a negative temperature coefficient of about $-2mV/°C$, is called complementary to absolute temperature (CTAT).

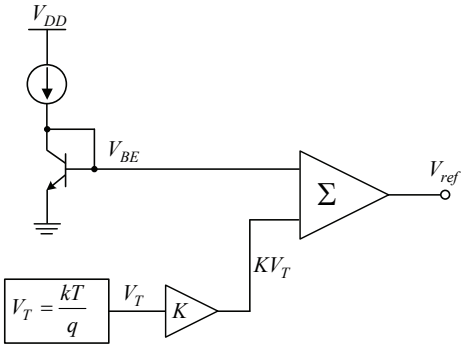


Fig.1. Block diagram of a bandgap voltage reference

The $V_T$ has a positive temperature coefficient of $0.086mV/°C$ is multiplied by gain $K$, which is proportional to absolute temperature (PTAT), so that $V_{ref}$ can be expressed as

$$V_{ref} = V_{BE} + KV_T \tag{1}$$

The output voltage $V_{ref}$ has low temperature dependence which is obtained by summation of CTAT voltage and PTAT voltage multiplied by gain $K$.

## Proposed all CMOS Band gap Voltage Reference circuit

The proposed concept of BGR is shown in fig.3. is based on topology proposed in [3]. This paper presents the all CMOS BGR circuit. The MOS transistors operating in weak inversion. There are two different points between in this paper presented here and another reports. First, in this paper presents the new design methodology for bandgap core circuit by defining the current and voltage with only one node and another node is set equal voltage which can be controlled by input voltages of op-amp. This method is able to reduce number of the resistor and second the start-up circuit is included in self-biased op-amp circuit by using only one NMOS transistor.

**Bandgap core circuit design**

The bandgap core circuit designed by voltage definition of $V_B$ only one node and node $V_A$ was set equal to $V_B$. The current $I_1$, $I_2$ and $I_3$ that are controlled by the same value due to the current mirror and the gate of PMOS $M_{10}$, $M_{11}$ and $M_{12}$ are connected to a common node.

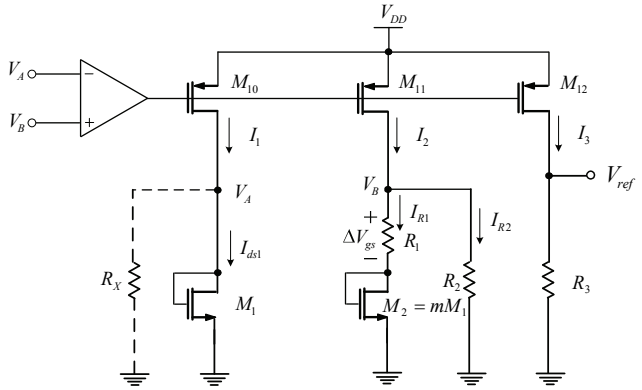


Fig.2. Proposed Band gap Voltage Reference circuit.

The current of $I_2$ is controlled by resistors of $R_1$, $R_2$ and $M_2$, the input voltage of op-amp are connected by nodes $V_A$ and $V_B$ are equalized. Then we have:

(2) $$V_A = V_B$$

(3) $$I_{ds_1} = I_1 = I_2 = I_3$$

(4) $$I_{ds_1} = I_{R_1} + I_{R_2}$$

As shown in fig. 3, the NMOS $M_1$ and $M_2$ are defined by operating in weak inversion regime, thus the drain-source current and $V_{gs}$ approximately is

(5) $$I_{ds_1} = I_t \frac{W}{L} e^{\frac{q(V_{gs_1} - V_{th})}{nkT}}$$

where

(6) $$I_t = 2n\mu_n C_{ox}\left(\frac{kT}{q}\right)^2$$

(7) $$V_{gs_1} = nV_T \ln\left[\frac{I_{ds1}.L_1}{I_t.W_1}\right] + V_{th}$$

(8) $$V_T = \frac{kT}{q}$$

Where $V_T$ is thermal voltage, $k$ is Boltzmann's constant $(1.38\times10^{-23}\,\mathrm{J/K})$, $q$ is magnitude of electron charge $(1.6\times10^{-19}\,\mathrm{C})$, $n$ is slope factor and $V_{th}$ is threshold voltage.

Substituting (5) and (6) into (7) then differentiating. We have

(9) $$\frac{\partial V_{gs}}{\partial T} = \frac{V_{gs}}{T} - 2n\frac{k}{q}$$

Equation (9) shows that the $V_{gs}$ falls with increasing temperature and $V_{gs}$ has a negative temperature coefficient of about $-2mV/°C$, whereas $V_T$ has a positive temperature coefficient of $0.086mV/°C$ can be written as

(10) $$\frac{\partial V_T}{\partial T} = \frac{k}{q}$$

The $V_{gs}$ of $M_1$ and $M_2$ can be written in terms of the current $I_{ds}$ as

(11) $$V_{gs1} = n\frac{kT}{q}\ln\left[\frac{I_{ds1}.L_1}{I_t.W_1}\right] + V_{th}$$

(12) $$V_{gs2} = n\frac{kT}{q}\ln\left[\frac{I_{ds2}.L_2}{I_t.W_2}\right] + V_{th}$$

In addition, we have

(13) $$V_{gs1} = V_{R_1} + V_{gs2}$$

Substituting (11) and (12) into (13) gives

(14) $$V_{R1} = \Delta V_{gs} = n\frac{kT}{q}\ln(m)$$

$I_{R_1}$ is proportional to $V_T$

(15) $$I_{R_1} = n\frac{kT}{q.R_1}\ln(m)$$

Where $m$ is a parallel multiple number and $I_{R_2}$ is proportional to $V_{gs1}$, which is set equal to $V_B$ are given by

(16) $$I_{R_2} = \frac{V_{gs1}}{R_2} = \frac{V_B}{R_2} = \frac{V_A}{R_2}$$

The $I_{R_1}$ and $I_{R_2}$ are used to produce the voltages, which has the positive temperature coefficient and has negative temperature coefficient, respectively.

The current $I_1$, $I_2$ and $I_3$ are controlled by PMOS $M_{10}$ $M_{11}$ and $M_{12}$. The gate of transistors connected to a common node can be written as

(17) $$I_1 = I_2 = I_3 = \frac{V_A}{R_2} + n\frac{kT}{qR_1}\ln(m)$$

As shown in fig.2. $I_2$ is sum of $I_{R_1}$ and $I_{R_2}$, the current $I_2$ is mirrored to $I_3$, in this design, the resistor $R_X$ can be cancelled. Thus, the $V_{ref}$ can be expressed as

(18) $$V_{ref} = \left[\frac{V_{gs1}}{R_2} + n\frac{kT}{q.R_1}\ln(m)\right]R_3$$

Therefore, the $V_{ref}$ for proposed BGR can be set any level between near 0 V and $V_{DD}$ by changing the resistance value of $R_3$.

**Self biased op-Amp included new startup circuit**

The self-biased structure for op-amp, included startup circuit with circuit solutions is suitable for low-supply-voltage operation and achieves the correct bias point at the power on, is shown in Fig.4.

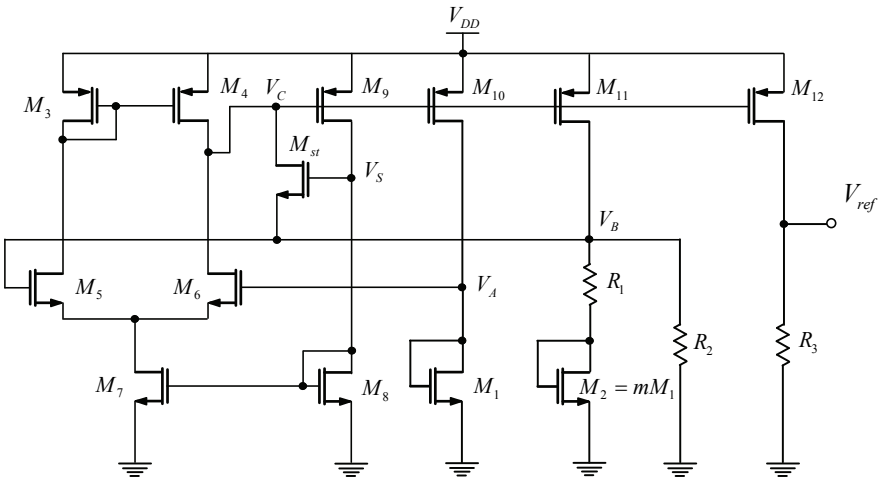


Fig.3. Complete Circuit of Band gap Voltage Reference

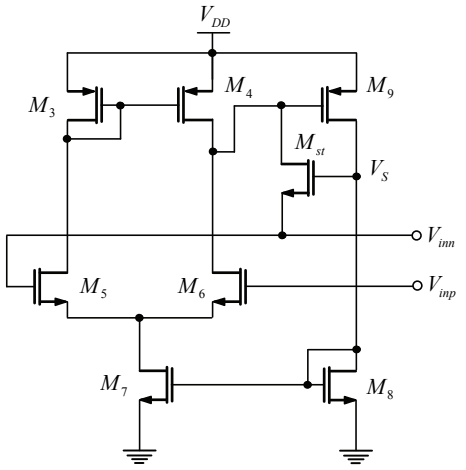


Fig. 4 Self bias op-amp included startup circuit

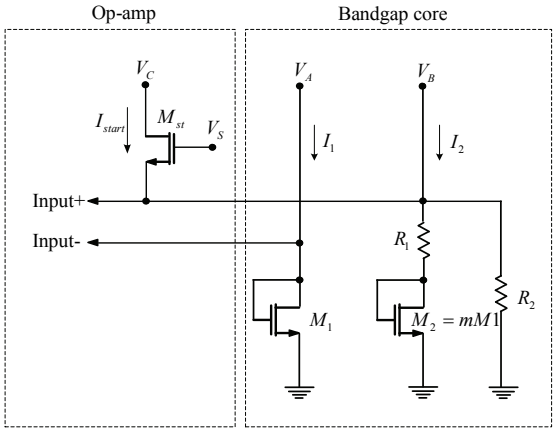


Fig.5. start-up circuit

**Start-up circuit**

Fig.3. shows the complete circuit of proposed bandgap voltage reference, when the circuit powered on. At first the BGR circuit is not operated, the node $V_B$ is almost ground level. The gate of $M_{st}$ will be pulled to high level until $V_{gs(M_{st})}$ is higher than the $V_{th}$, which to turns on $M_{st}$. After that, the voltage will drop across the resistors $R_2$, $R_1$ and $M_2$ due to the current $I_{start}$. When $V_B$ is high enough, the BGR circuit will start up. Then the voltage between nodes $V_S$ and $V_B$ becomes low. Thus, $M_{st}$ will be turned off. This structure ensures the op-amp has stable biased current as long as the output $V_{ref}$ keeps invariable.

**Simulation results**

The results of the proposed bandgap voltage reference circuit are verified by PSPICE simulations. Fig.6. shown reference voltage is about 500.2 mV and voltage variation less than 0.3 mV, when temperature varies from $0-100°\mathrm{C}$. The temperature coefficient is $5\ \mathrm{ppm}/°\mathrm{C}$ and power dissipation is only $10.7\ \mathrm{uW}$.

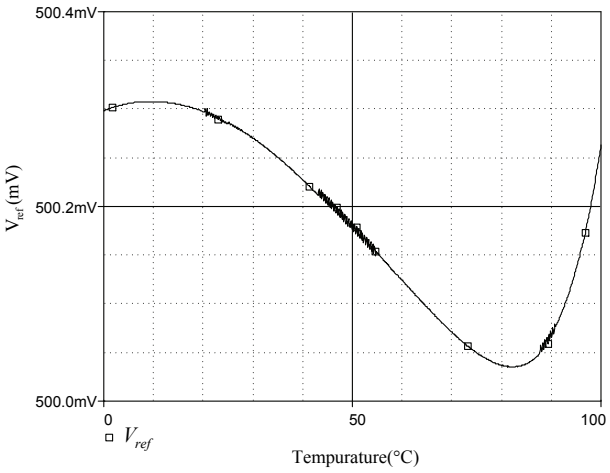


Fig.6. Temperature dependence of output reference voltage

Fig.7. shows the currents of $I_{R1}$ and $I_{R2}$ has a positive and negative temperature coefficient, respectively**.** At operating temperature from $0-100°\mathrm{C}$. The current $I_{R1}$ is combined with $I_{R2}$ to create a temperature-compensated current $(I_2)$, and is mirrored to $M_{12}$ to produce $I_3$, then flows through a resistor $(R_3)$ to create the $V_{ref}$.

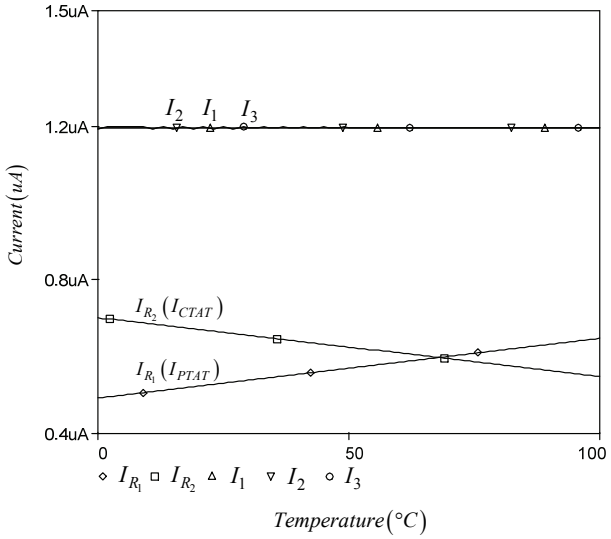


Fig.7. the current $I_1$, $I_2$ and $I_3$, which is sum of $I_{R_1}$ and $I_{R_2}$

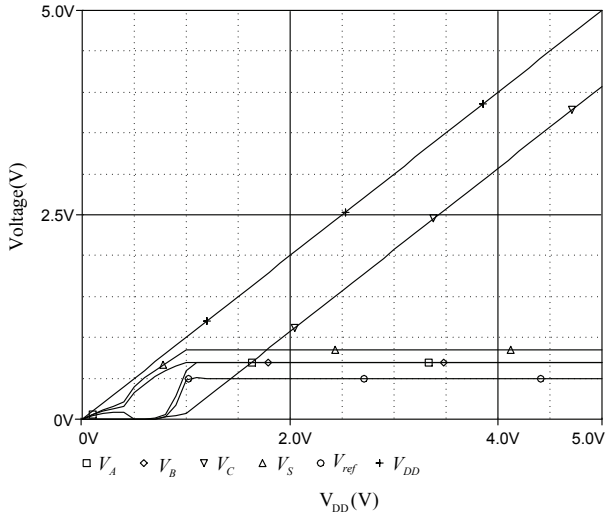


Fig.8. voltages at any node of proposed BGR

Fig.8. shows the voltage at any nodes of the BGR circuit. The BGR circuit operation was started up at 1.2V. The $V_A$ and $V_B$ were controlled to be same voltage and stable output voltage conditions, although the $V_{DD}$ are varied from 1.2V to 5.0V.

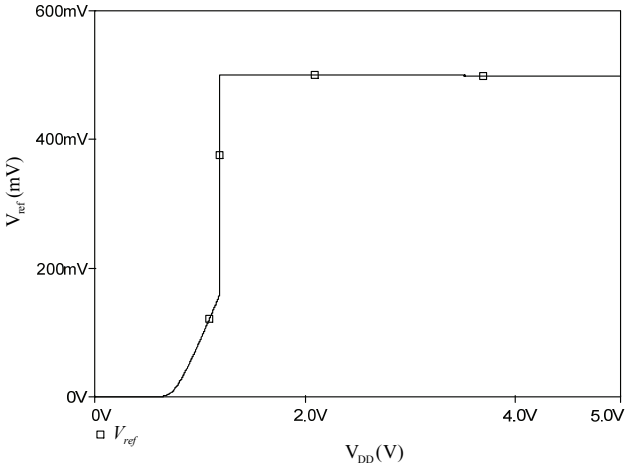


Fig.9. $V_{ref}$ as a function of supply voltage

Fig.9 shown the result of $V_{ref}$ as a function of supply voltage. The BGR can successfully operate from 1.2V to 5.0V supply voltage and reference voltage is set about 500 mV.

**Conclusion**

The all CMOS Bandgap voltage reference circuit without parasitic vertical bipolar transistors and diodes exhibited in this paper is to improve the bandgap core and self-biased op-amp included startup circuit. The $V_{ref}$ is generated by the sum of two currents with one feedback loop. The output voltage can be set at any level between near $0\text{V}$ to $V_{DD}$. The simulation results are shown that the performance is suitable for low-power and low voltage applications.

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The correspondence address is:
*Saweth Hongprasit, Faculty of Engineering, Mahasarakham University, Tambon Khamriang, Kantharawichai District, Maha Sarakham 44150 Thailand.*
*e-mail:saweth@psn.co.th*
*Worawat Sa-Ngiamvibool, Faculty of Engineering, Mahasarakham University, Tambon Khamriang, Kantharawichai District, Maha Sarakham 44150 Thailand. e-mail: wor_nui@yahoo.com*
*Apinan Aurasopon, Faculty of Engineering, Mahasarakham University, Tambon Khamriang, Kantharawichai District, Maha Sarakham 44150 Thailand.*
*e-mail: aurasopon@hotmail.com*

*e-mail: saweth@psn.co.th*