An Assura geometry extraction and Spectre re-simulation flow to simulate Shallow Trench Isolation (STI) stress effects in analogue circuits

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Xignal Technologies AG develops and markets mixed-signal ICs that enable new system architectures through significant improvements in performance and in power consumption.

Abstract

For CMOS technologies below 0.25µm Shallow Trench Isolation (STI) has become the standard device isolation scheme.

Despite its advantages, STI applies mechanical stress to the MOS transistor changing its electrical device characteristic. As the stress depends on local layout geometries, the stress has to be evaluated for each individual device. The bsim3v3 model has been enhanced and new instance parameters and equations were added to the model to cover this stress effects.

This presentation shows an approach how STI stress effects can be accounted for. The presented method is based on an Assura geometry extraction and Spectre re-simulation flow. For that the MOS transistors Component Description Format (CDF) were modified and additional commands were added to the Assura ‘extract rules‘.

Example layout geometries were extracted and simulated and the influence of the stress effects were evaluated. As a conclusion appropriate layout techniques will be demonstrated to minimise STI stress for sensitive analogue circuits.

This approach has been successfully proven at a 14Bit, 40MSps ADC design.

Contents

- Process Evolution form LOCOS to STI
- Model Enhancements (bsim3v3)
- Implementation in the CDF and Assura extract rule file
- Design Flow
- Example Layouts
- Conclusion

LOCOS

Local Oxidation of Silicon (LOCOS) has been the standard device isolation scheme of CMOS technologies down to ~0.25µm feature size.

Due to shrinking issues further device isolation with LOCOS is no longer practical and an alternative form of isolation was developed.

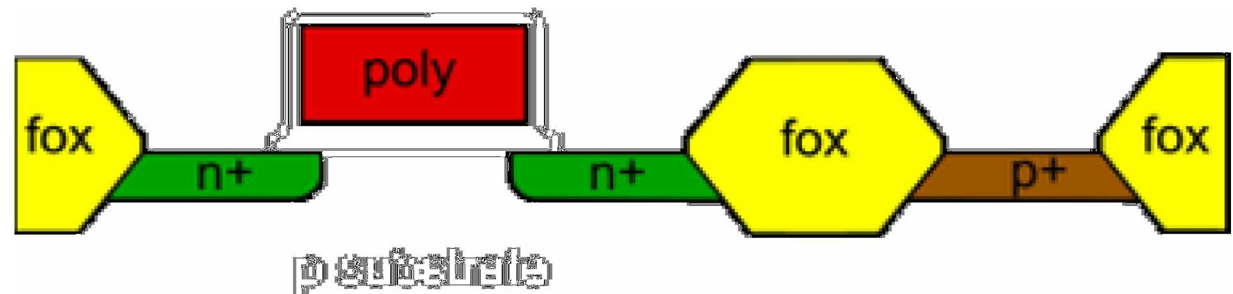


Figure 1: MOS cross section with field oxide

What is STI?

Shallow Trench Isolation (STI) is the device isolation scheme for modern CMOS technologies below 0.25µm.

STI allows further shrinking, higher device density, flatter surface topology and has less perimeter sidewall capacitance than LOCOS.

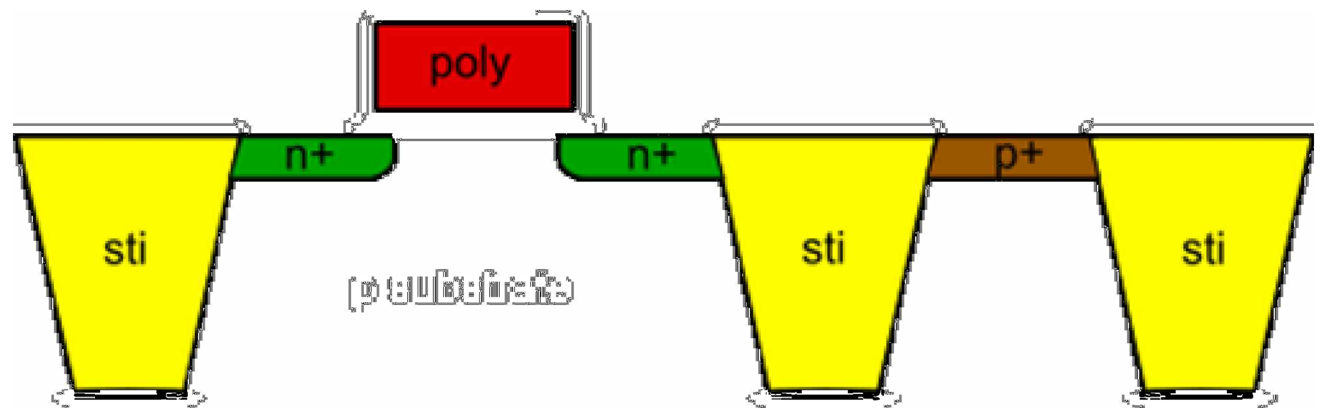


Figure 2: MOS cross section with STI

What is STI stress?

Despite its advantages, STI applies mechanical stress to the MOS transistor.

This effect, known as STI or Length of Oxide Definition (LOD) stress effect, influences the electrical characteristics of a MOS transistor, it impacts mobility (μeff), carrier saturation velocity (Vsat) , threshold voltage (Vth) and other second order effects [1] [2].

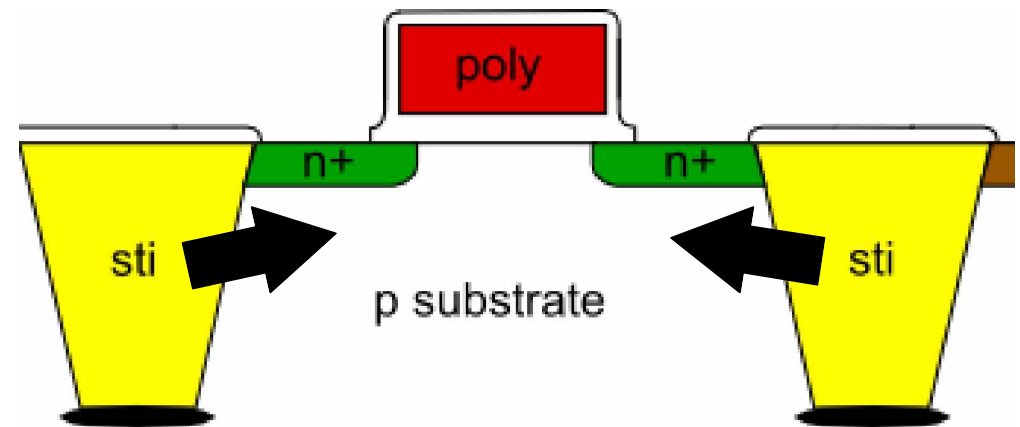
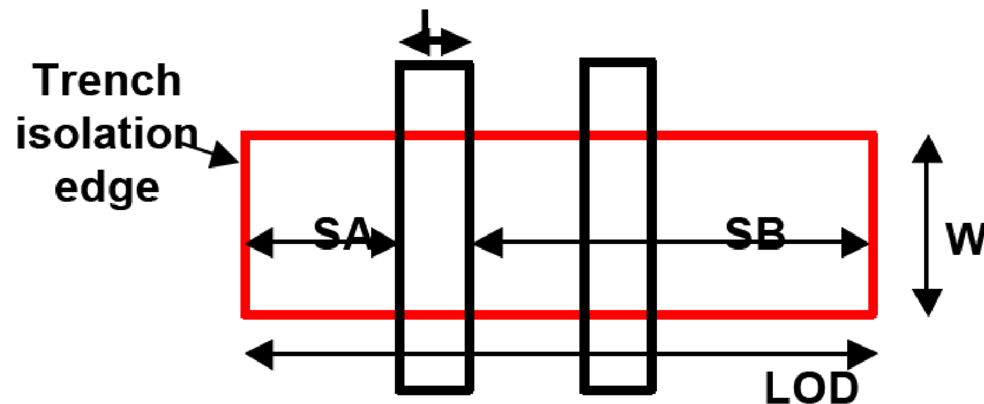


Figure 3: Stress induced by STI

New model parameters

To account for this stress, standard models like bsim3v3 were enhanced and new instance parameters and equations were added [1] [3].



$$LOD = SA + SB + L$$

OD: gate Oxide Definition

Figure 4: Typical MOS layout top view

The new instance parameters SA and SB are the distance between the Oxide Definition (OD) edge for one respectively the other side to the poly edge.

Model enhancements

The mobility (μeff) and saturation velocity (Vsat) parameters are used to demonstrate how the extracted layout information is fed into the enhanced bsim3v3 model equations.

$$\mu_{eff} = \frac{1 + \varrho_{\mu eff}(sa, sb)}{1 + \varrho_{\mu eff}(sa_{reff}, sb_{reff})} \cdot \mu_{eff0}$$

$$V_{sat} = \frac{1 + K \cdot \varrho_{\mu eff}(sa, sb)}{1 + K \cdot \varrho_{\mu eff}(sa_{reff}, sb_{reff})} \cdot V_{sat0}$$

Figure 5: Mobility and saturation velocity related equations

In the above equations μeff0 and Vsat0 are low filed mobility and saturation velocity at SAreff and SBreff. And SAreff and SBreff are reference distances between the OD edge to the poly edge form one and the other side.

MOS with irregular shapes

In general MOS transistors have irregular shapes. To fully describe the shape of their OD regions additional instance parameters are required. However this results in to many parameters for the simulator netlist. A way to overcome this is the concept of effective SA and SB (SAeff and SBeff) [1] [4].

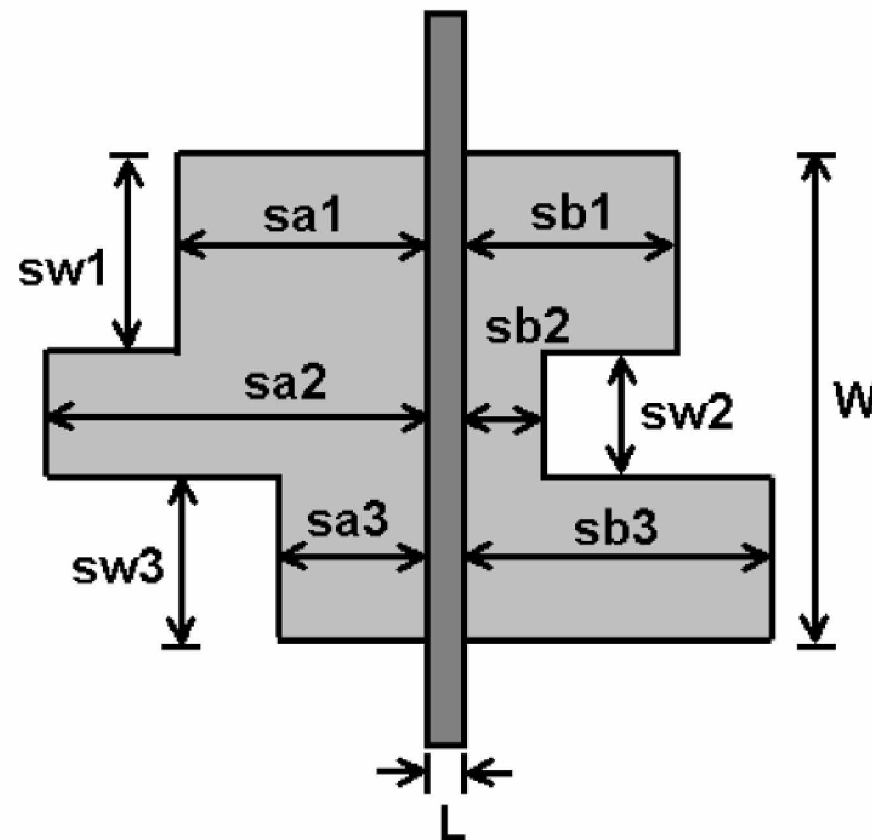


Figure 6: MOS layout with irregular shape

Concept of effective SA and SB

The concept of SAeff and SBeff allows an accurate and efficient layout extraction.

Only one set of SA and SB has to be extracted to completely describe the stress effects of irregular MOS layouts.

The resulting equations can then be implemented directly in a layout extraction tool like Cadence Assura.

$$\frac{1}{sa_{eff}+0.5\cdot l_{drawn}}=\sum_{i=i}^{n}\frac{sw_i}{w_{drawn}}\cdot\frac{1}{sa_i+0.5\cdot l_{drawn}}$$

$$\frac{1}{sb_{eff}+0.5\cdot l_{drawn}}=\sum_{i=i}^{n}\frac{sw_i}{w_{drawn}}\cdot\frac{1}{sb_i+0.5\cdot l_{drawn}}$$

$$Inv_sa=\frac{1}{sa_{eff}+0.5\cdot l_{drawn}}, Inv_sb=\frac{1}{sb_{eff}+0.5\cdot l_{drawn}}$$

Figure 7: Equations for layout extraction

The measureSTI command

- Assura offers the powerful command *measureSTI* to measure layout data associated with the STI stress effect. The ***measureSTI*** command can be used like the ***measureParameter*** command after the ***extractMOS*** statement.
- The ***calculateExpresion*** is an argument of the *measureSTI* which allows to calculate **Inv_sa** and **Inv_sb**.
- The *measureSTI* command **evaluates the equations** in the *calculateExpresion* argument **for each diffusion shape**.
- The **result** of the ***calculateExpresion*** equations is returned in a list of derived layers defined in the ***output*** argument.
- These output values can be further processed with the ***calculateParameter*** command to get **SAeff** and **SBeff** for the extracted MOS.

measureSTI in the extract.rul file

```
if( avSwitch( "Measure_STI" ) then
   measureSTI(
    nmos                                         ;; device recognition layer
    od                                           ;; diffusion layer
    60                                           ;; maximum distance to measure
    output( invSA  invSB )                       ;; <- output parameter values
    calculateExp(                                ;; calculation of output params.
        sw / w_NMOS / ( sa + 0.5 * l_NMOS )
        sw / w_NMOS / ( sb + 0.5 * l_NMOS )
                )
    )
SAeff = calculateParameter( 1e-6 / invSA - 0.5u * l_NMOS ) ;; SA <- invSA
nameParameter( SAeff "sa")
SBeff = calculateParameter( 1e-6 / invSB - 0.5u * l_NMOS ) ;; SB <- invSB
nameParameter( SBeff "sb")
)
```

Instance parameters in the CDF

The Component Description Format (CDF) of the MOS transistor has to be modified to reflect the two additional model instance parameters SA and SB.

For that reason the two parameters were added to the parameters section of the MOS CDF.

```
;;; Parameters
cdfCreateParam( cdfId
        ?name           "sa"
        ?prompt         "OD to Poly distance A (M)"
        ?units          "lengthMetric"
        ?defValue       "350.00n"
        ?type           "string"
        ?display        "artParameterInToolDisplay('sa)"
        ?parseAsNumber  "yes"
        ?parseAsCEL     "yes"
    )
    cdfCreateParam( cdfId
        ?name           "sb"
        ?prompt         "OD to Poly distance B (M)"
        ?units          "lengthMetric"
        ?defValue       "350.00n"
        ?type           "string"
        ?display        "artParameterInToolDisplay('sb)"
        ?parseAsNumber  "yes"
        ?parseAsCEL     "yes"
    )
```

Instance parameters in the CDF

The parameters SA and SB were added to the simulator information CDF section.
This causes the parameters to be included into the simulators netlist.

```
;;; Simulator Information
cdfId->simInfo->spectre = '( nil
        propMapping        nil
        namePrefix         ""
        otherParameters    (model)
        instParameters     (w l as ad ps pd nrd nrs m ... sa sb)
        termOrder          (D G S B)
        termMapping        (nil D \:d G \:g S \:s B \:b)
        componentName      nmos
    )
```

Design Flow

1 Create Designs

Schematic View
Configuration View

Layout View

3

Run Assura RCX
with output LVS extracted
?lvsExtractedCellView “t”

Output Lvs Extracted View

?lvsExtracted “t”
creates an extracted view
with device geometry and
connectivity information,
but without parasitics

Cell Bindings

Library	Cell	View Found	View to Use
analogLib	idc	spectre	
analogLib	vcvs	spectre	
analogLib	vdc	spectre	
wk_bernd	sti_n3b	sti_extracted	sti_extracted
wk_bernd	sti_top	schematic	
xigDev	n12	spectre	

The Measure_STI switch

The *measureSTI* command increases the runtime of the LVS run significantly. For a typical standard cell layout a LVS run takes about **8 times longer**.

Therefore an additional switch ***if(avSwitch("Measure_STI")*** is implemented, to enable the *measureSTI* command through the user interface for analog layouts only.

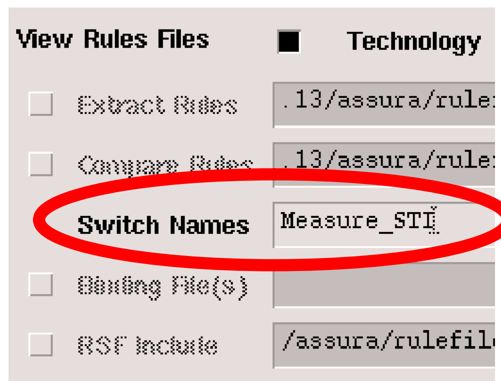


Figure 8: Measure_STI switch

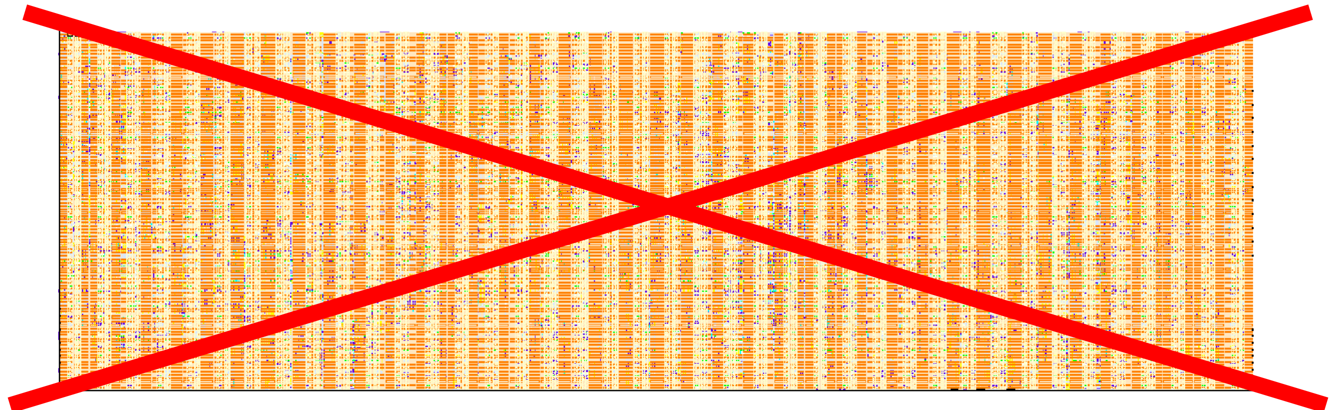


Figure 9: Typical standard cell layout

Id variation relative to SA and SB

In simulations the STI stress effect is noticeable as a drain current (Id) variation.

Id increases relative to SA and SB for NMOS and decreases relative to SA and SB for PMOS transitors.

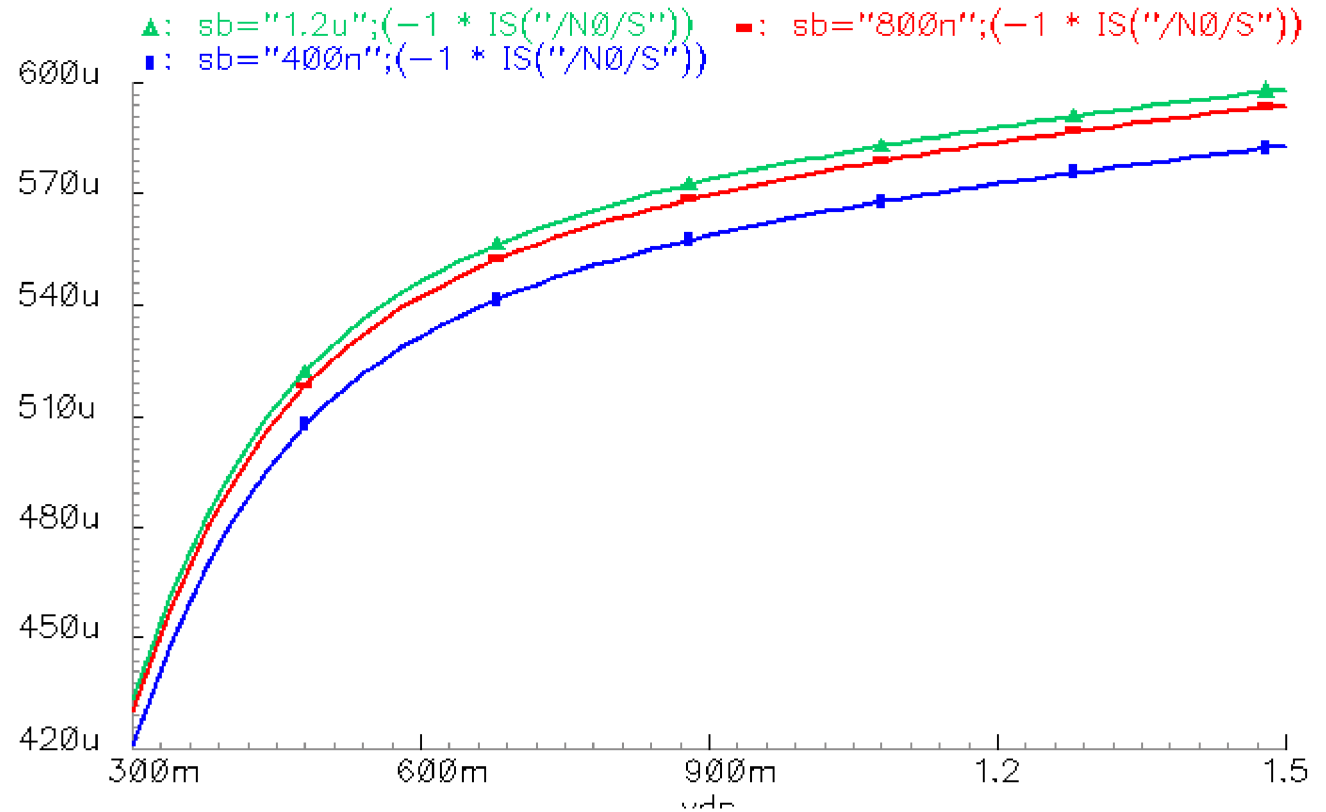


Figure 10: NMOS Ids/Vds for different SB's

Id variation in multifinger devices

In multifinger MOS devices Id variation is caused by different SA and SB per finger. But for sensitive cells like current mirrors where device matching is extremely important such multifinger layouts are state of the art.

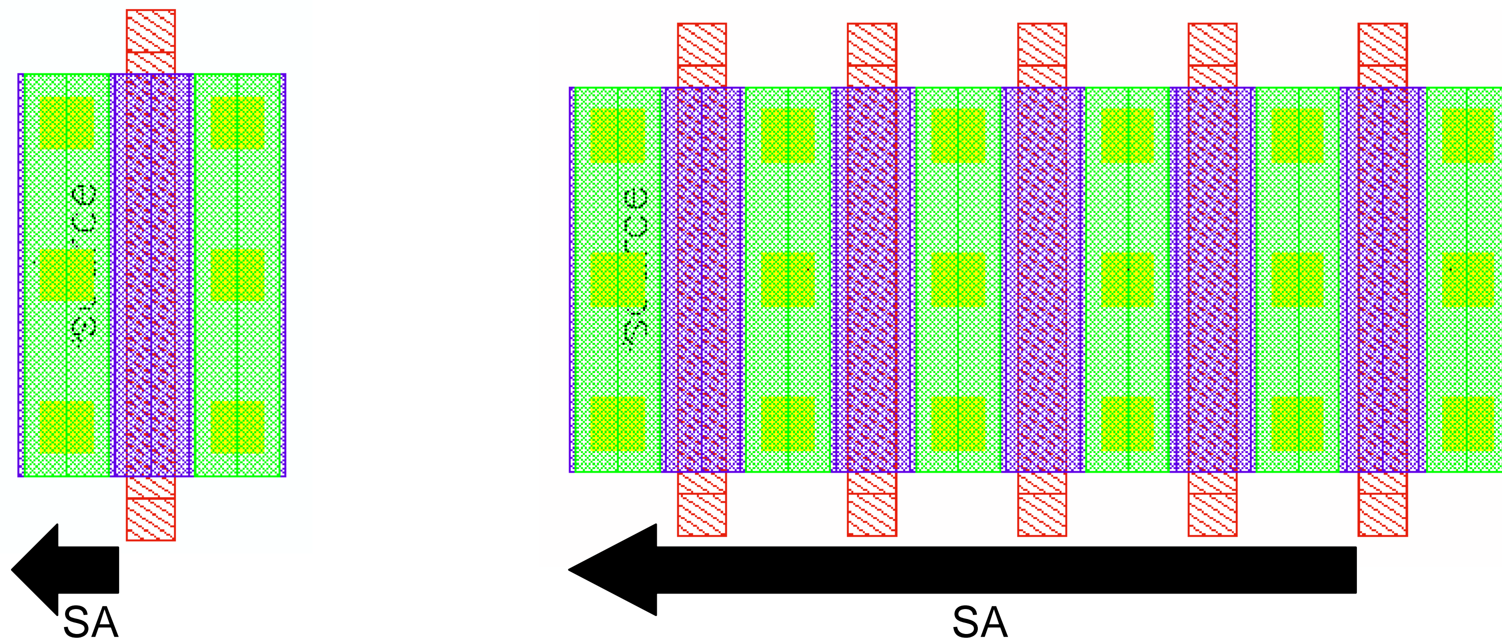


Figure 10: Single gate and multifinger MOS

cadence designer network

cdn LIVE

A NMOS current mirror example

High precision current mirrors are key elements in most analog building blocks like operational amplifiers [6].

The device sizes of the current mirror in Fig.10 have been chosen to demonstrate the STI effect.

Various layouts have been extracted with the presented *measureSTI* command and the matching of the extracted layouts compared.

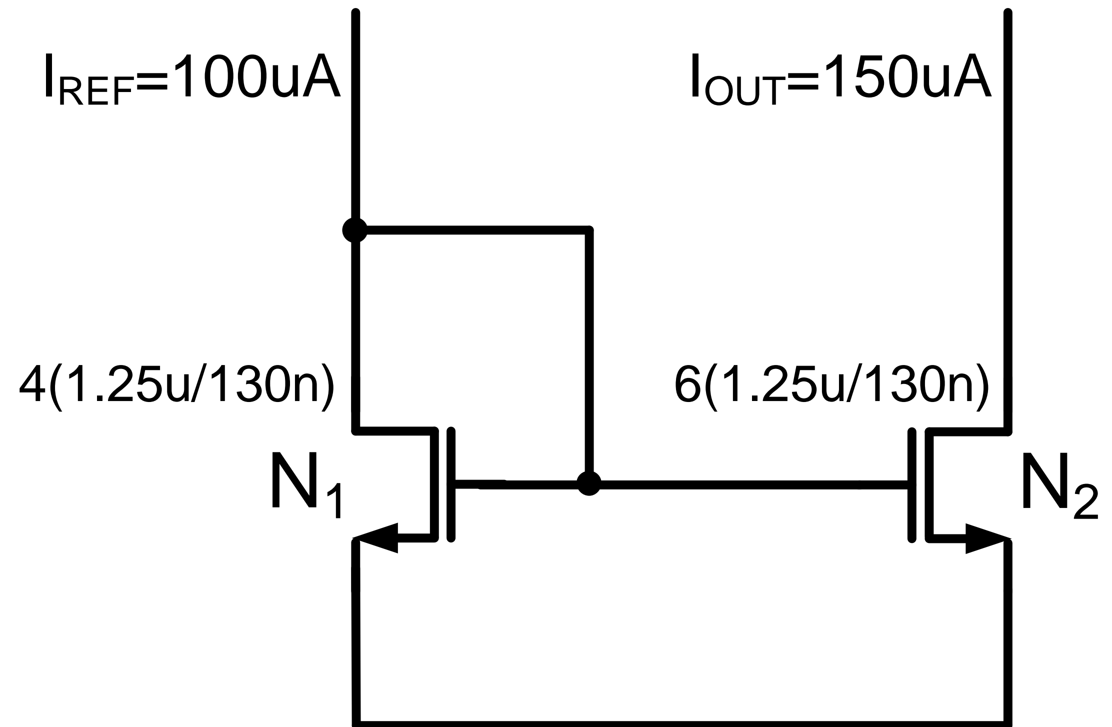


Figure 10: Typical NMOS current mirror

A current mirror layout

A common technique to achieve matching in current mirrors is to nest the transistors as pairs, $_{S}\mathbf{N2}_{D}\mathbf{N2}_{S}\mathbf{N1}_{D}\mathbf{N1}_{S}\mathbf{N2}_{S}\mathbf{N2}_{S}$ shown in Fig. 11.

STI stress causes additional asymmetry, therefore this technique is now not longer sufficient to achieve precise current matching.

The re-simulated layout shows an Id distribution form the lowest Id at corner transistors to the highest Id for the center transistors.

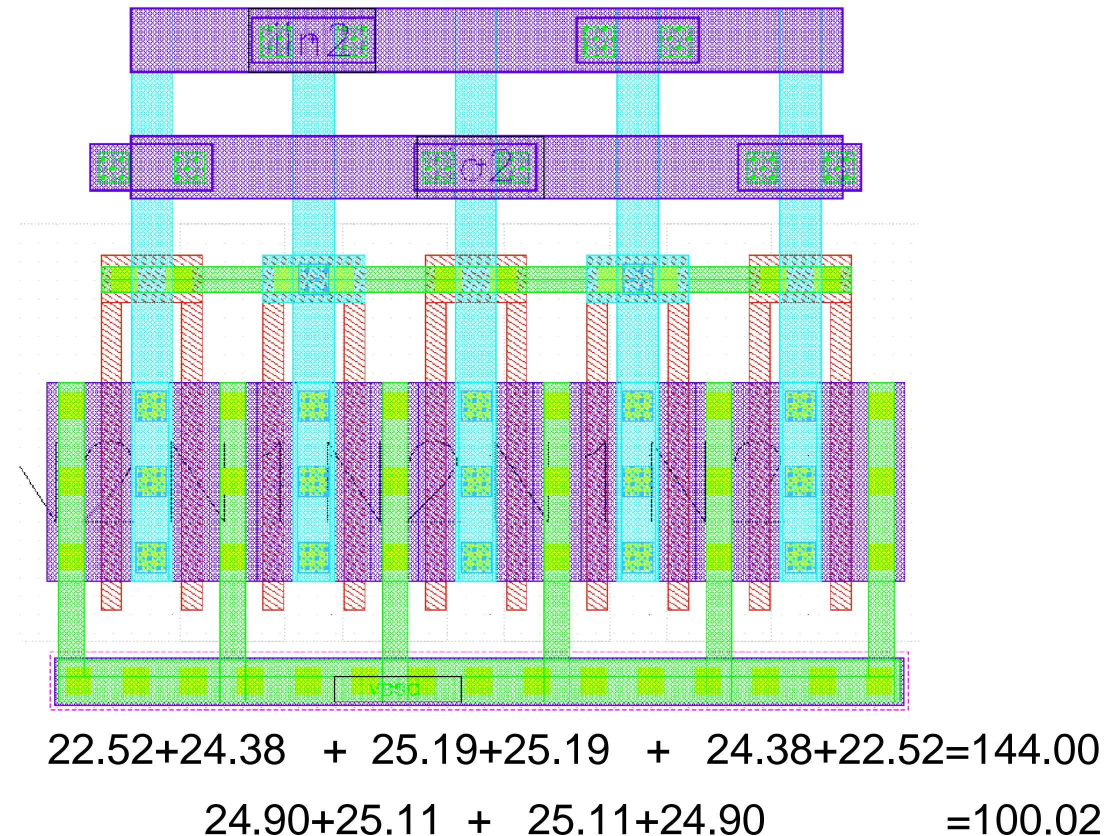
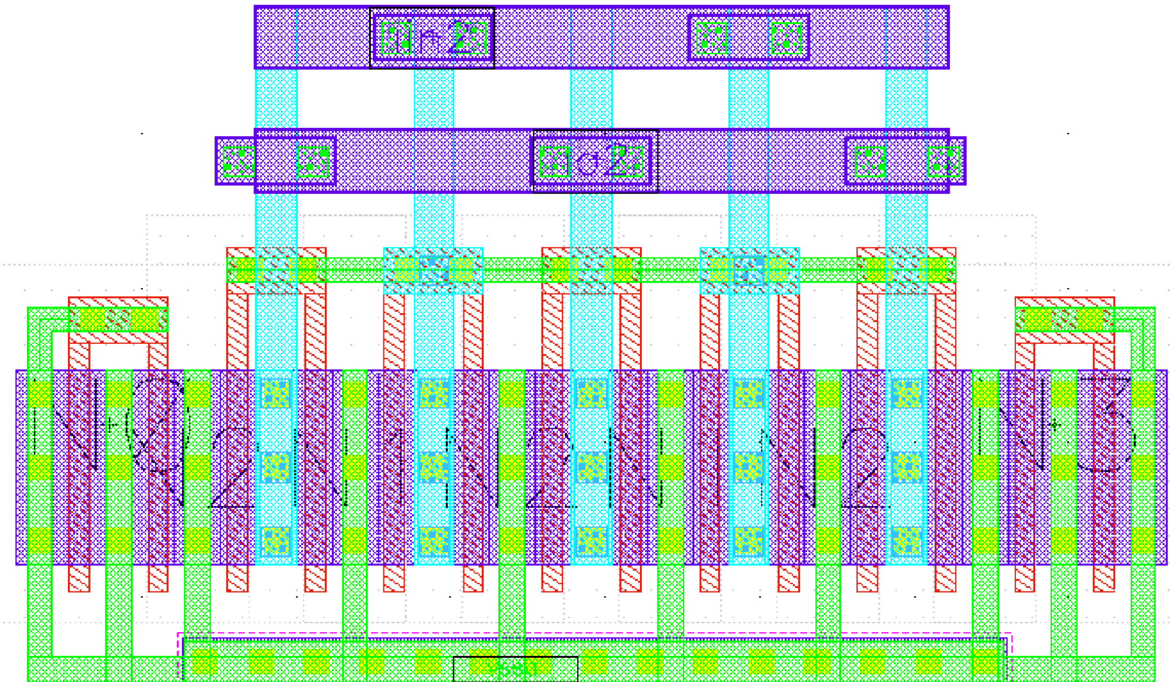


Figure 11: Typical layout of a NMOS current mirror

A current mirror layout with dummies

To get a uniform Id distribution in all transistors the **STI stress has to be identical** for all devices.

Therefore the distance of the poly to OD edge for the corner transistors has to be increased. This is achieved by placing dummy devices with shared diffusion next to the active device.



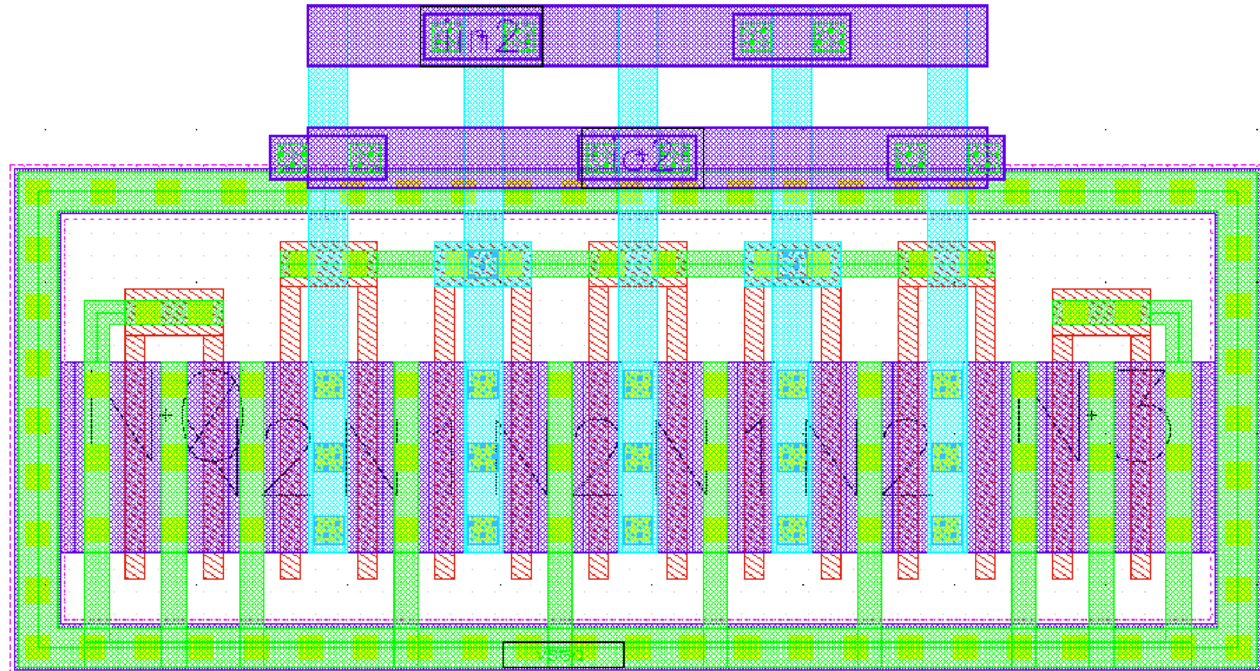
24.60+24.84 + 25.07+25.07 + 24.84+24.60=149.02

24.97+25.04 + 25.04+24.97 =100.02

Figure 12: NMOS current mirror with dummies

A current mirror layout with guardring

In addition to dummy transitors it is possible to increase the distance of the poly to OD edge by surounding the devices with a substrate guardring.



24.74+24.89 + 25.05+25.05 + 24.89+24.74 =149.36

24.98+25.03 + 25.03+24.98 =100.02

Figure 12: NMOS current mirror with dummies plus guardring

Proven approach

This approach has been successfully proven at a 14Bit, 40MSps ADC design [6].
The ADC was designed in a 0.13µm 1-poly 8-metal CMOS technology.

Conclusion

- A design flow has been demonstrated to simulate parameter mismatch of MOS devices which originate from STI stress.
- This is realized with an Assura layout extraction and a Spectre post-layout simulation.
- The flow enables the optimisation of layout structures to achieve the matching performance required by analog building blocks.

References

[1] Xuemei (Jane) Xi et al., “ BSIM4.3.0 MOSFET Model – User‘s Manual“, University of California, Berkley, Sept. 2003.

[2] Silvaco International, “Stress Effect Model in BSIM3v3 Model“ , The Simulation Standard, pp. 5 – 6, Jan. 2004.

[3] Cadence Design Systems, “Spectre Circuit Simulator Device Models and Circuit Components“, Chapter 20, BSIM3v3 Level 11 Model (bsim3v3), LOD Model and Stress Effect.

[4] Ke-Wei Su et al., “A Scaleable Model for STI Mechanical Stress Effect on Layout Dependence of MOS Electrical Characteristics“, IEEE Custom Integrated Circuits Conference, pp. 245 – 248, Sept. 2003.

[5] Cadence Design Systems, “Assura Physical Verification Command Reference“, Chapter 3, LVS Commands.

[6] G. Mitteregger et al., “A 14b 20mW 640MHz CMOS CT ΔΣ ADC with 20MHz Signal Bandwidth and 12b ENOB“, Proc. of ISSCC 2006.