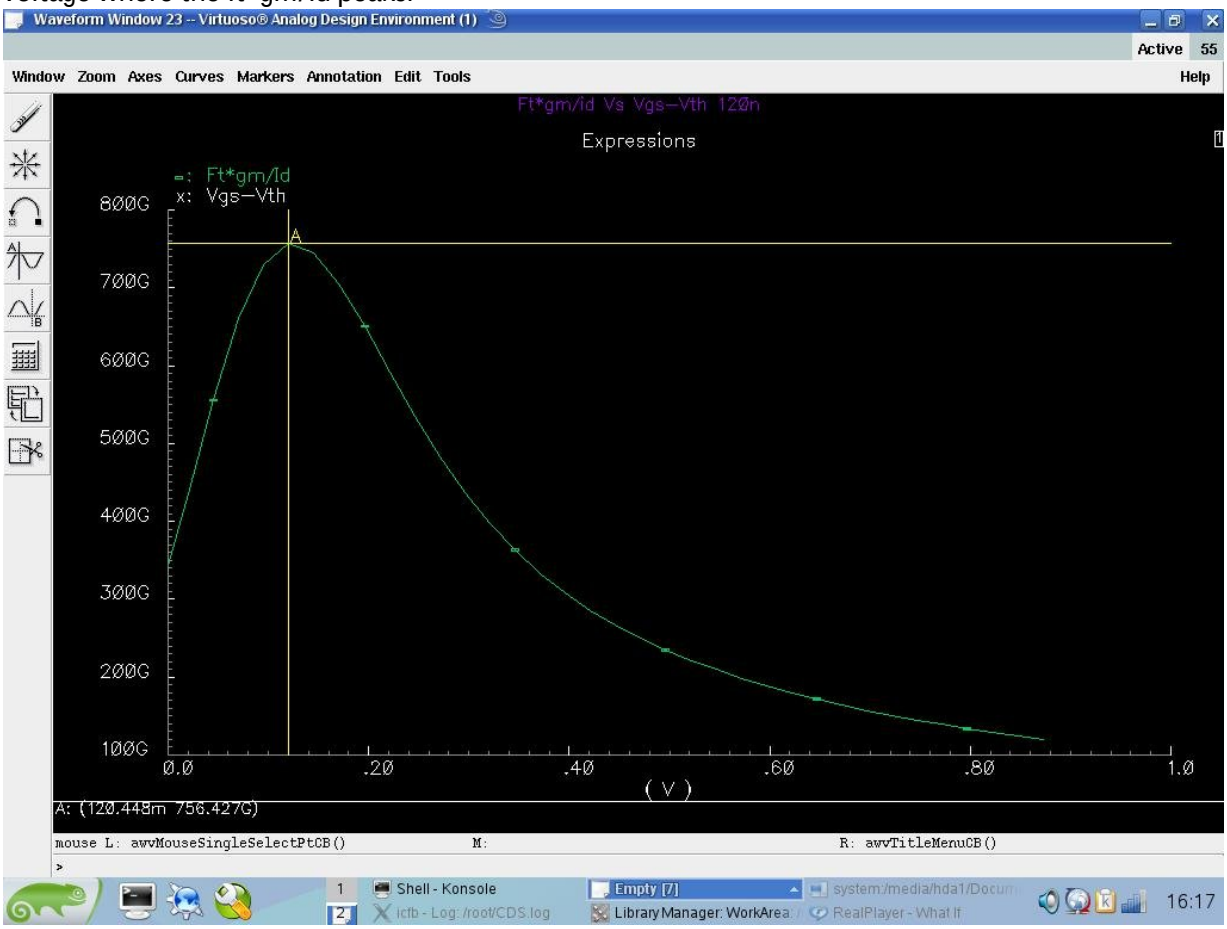
I am having a problem with designing a simple common source amplifier. The design meets the specs only at the nominal bias point, but when I plot the gain (dVout/dVin) vs Vin I get a really strange curve that is shown below. Below is the design example and how I approached it.

"Design an NMOS common-source stage driving a 1pF load with 500MHz unity-gain bandwidth. Choose a sufficiently long L to achieve an open-loop gain of at least 30 for output voltages between 0.3V and 0.9V and minimize the power dissipation of the circuit. Determine the device width and bias current, and verify the gain and bandwidth with SPICE. Also, plot the small-signal gain $a_{v0}=dV_o/dV_i$ as a function of the output DC level."

First of all I decided that a Vdsat of 120mV is good for this design because simulations show that this is the voltage where the ft*gm/id peaks.



The gm can be decided according to the unity gain bandwidth spec :

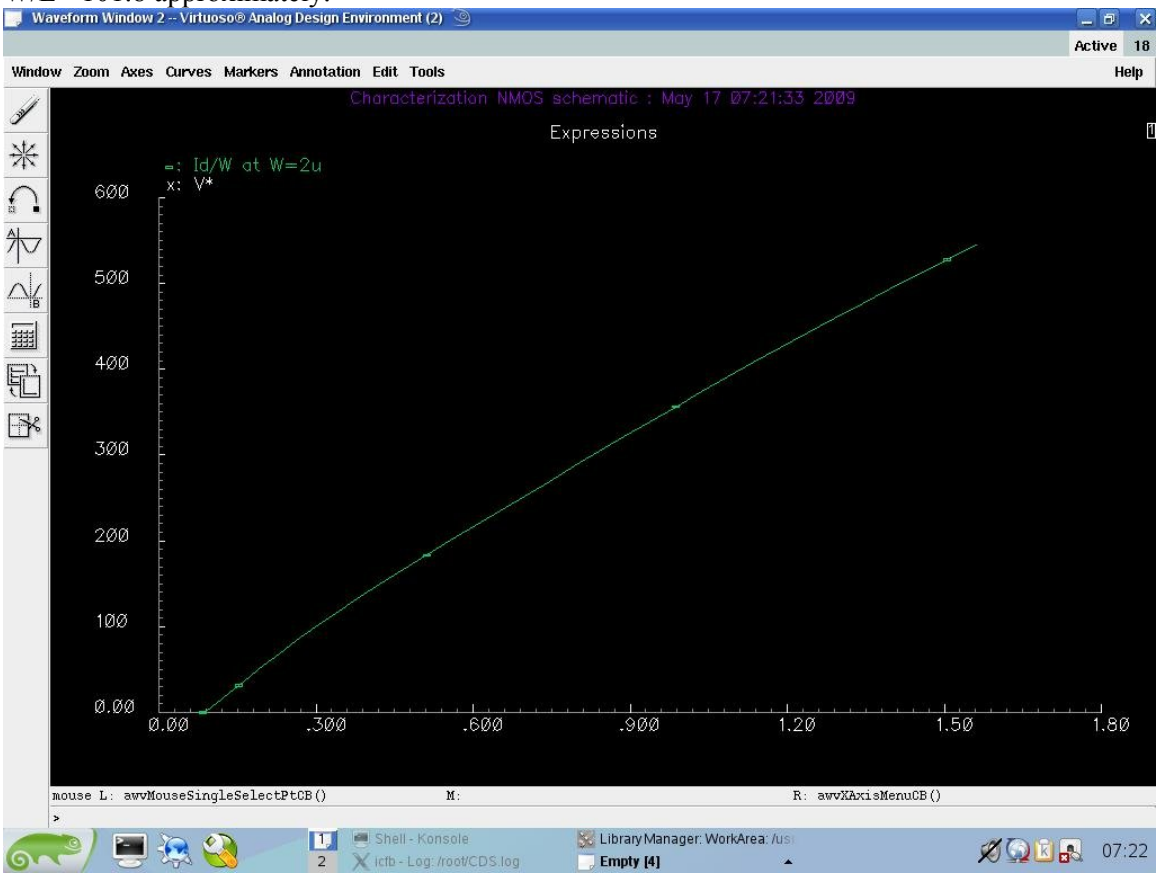
$g_m = 2\pi f_u C_L = 2\pi * 500M * 1pF = 3.14mS$

From gm and Vdsat I can determine the current :

$I_D = g_m Vdsat/2 = 188.4uA$

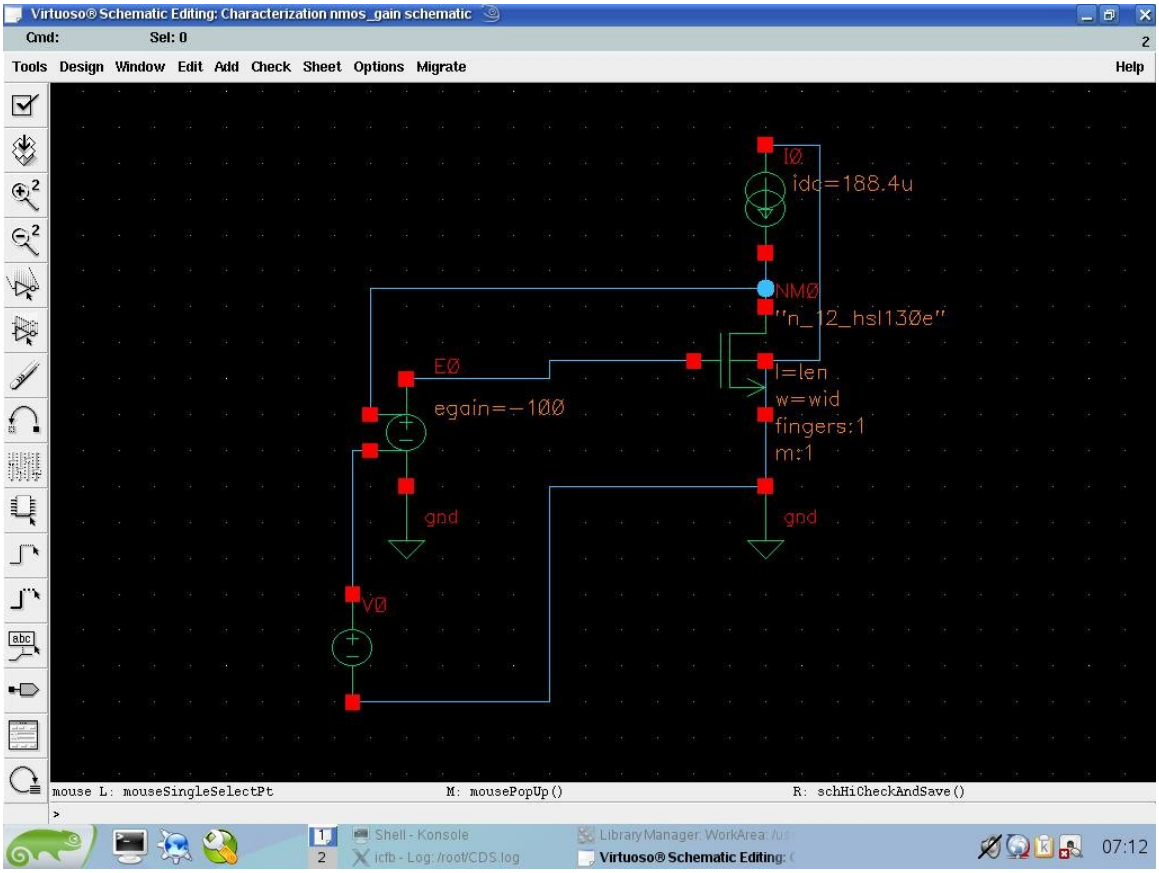
Now I need to know the value of L that satisfies the gain/swing spec :

I first used the current density chart to see the value of W/L that gives the Vdsat and Id I want.
W/L= 101.8 approximately.

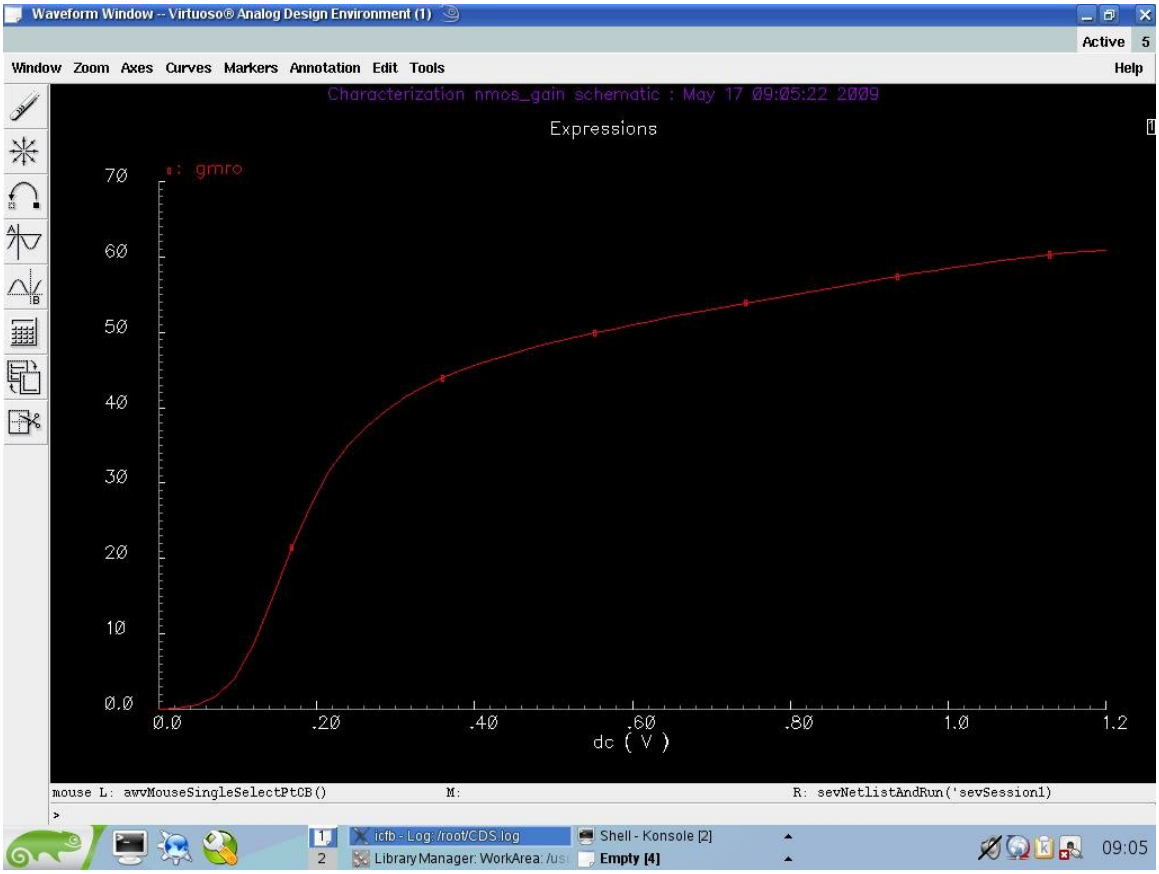


Id/W vs Vdsat

I then turned on to a test bench that shows me the gmro vs Vds of the transistor. I start by L=0.12u and keep increasing it until I find the suitable L. L=0.3u W=30.54u was more than enough.

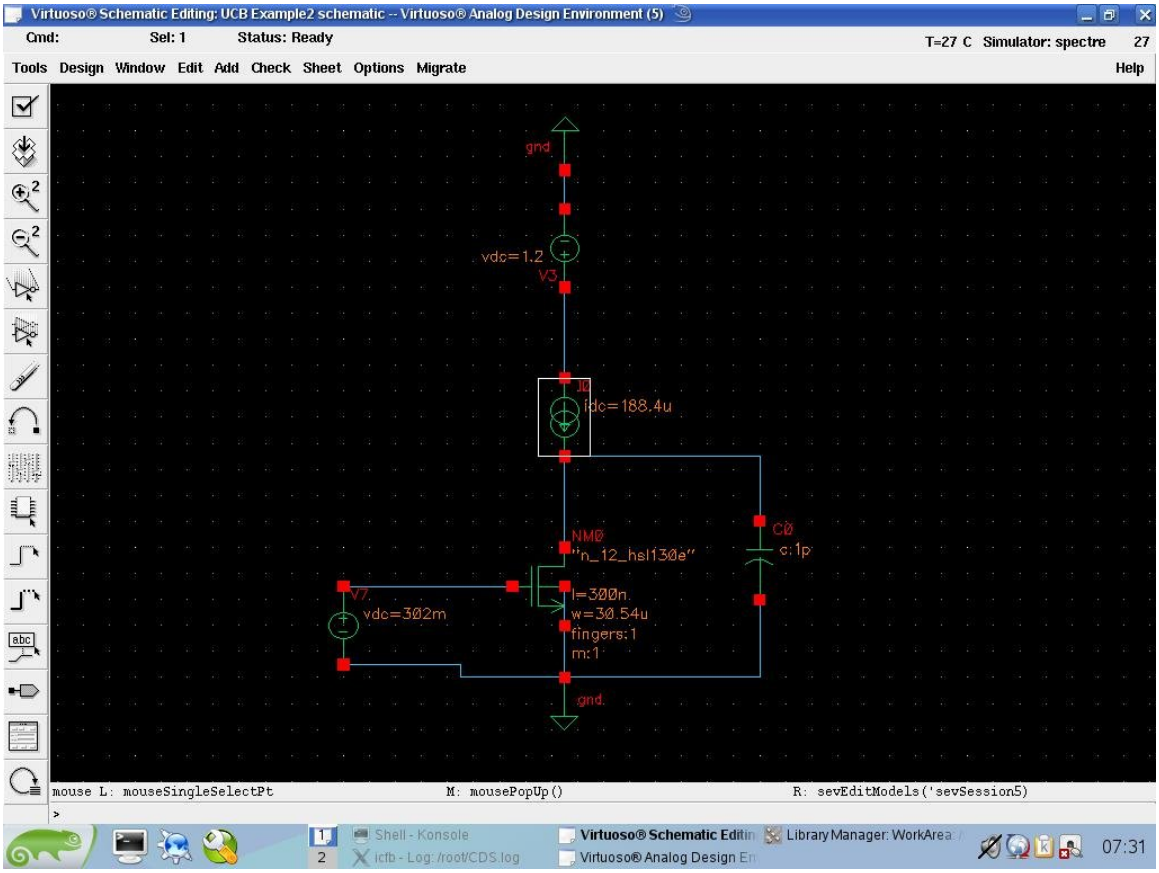


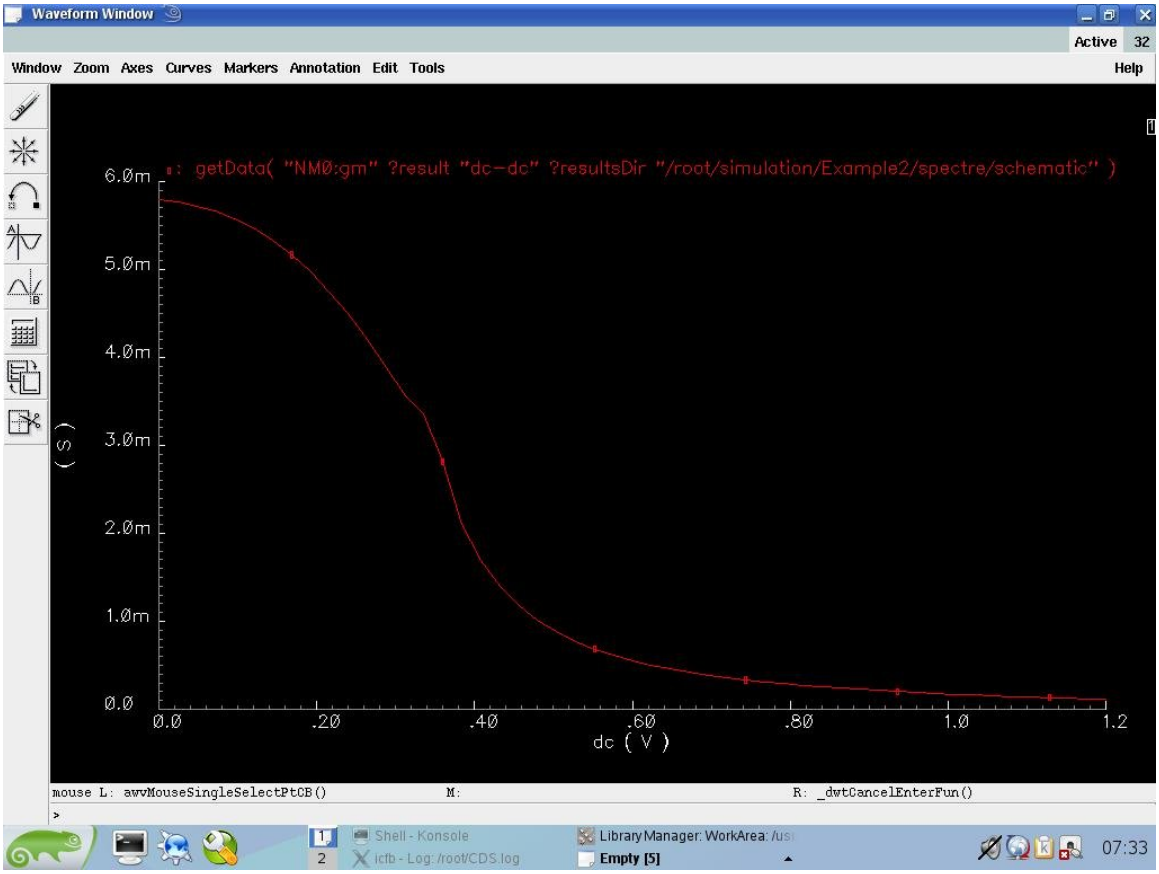
Test bench : the opamp is used to set the value of Vgs that keeps the current of the transistor equal to the desired current.



gmro(intrinsic gain) vs Vds

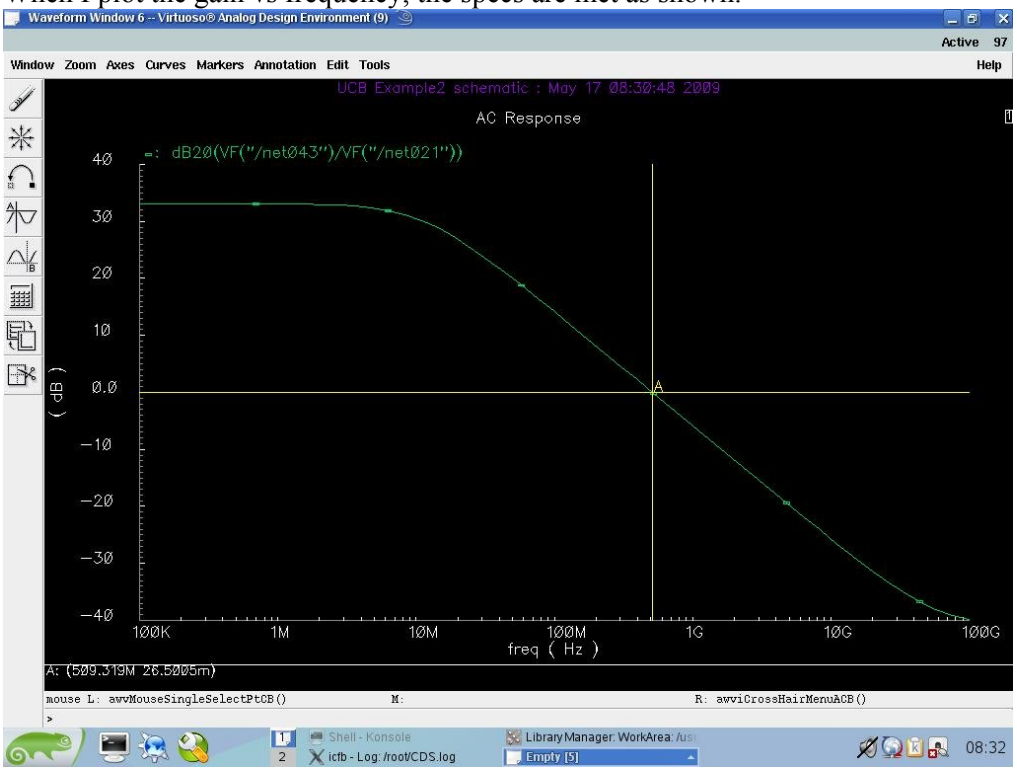
After that I put the transistor into the circuit shown below and plot gm vs Vgs to determine the suitable bias point. The bias point where gm & Vdsat are as needed is at 345.612mV.





gm vs Vgs

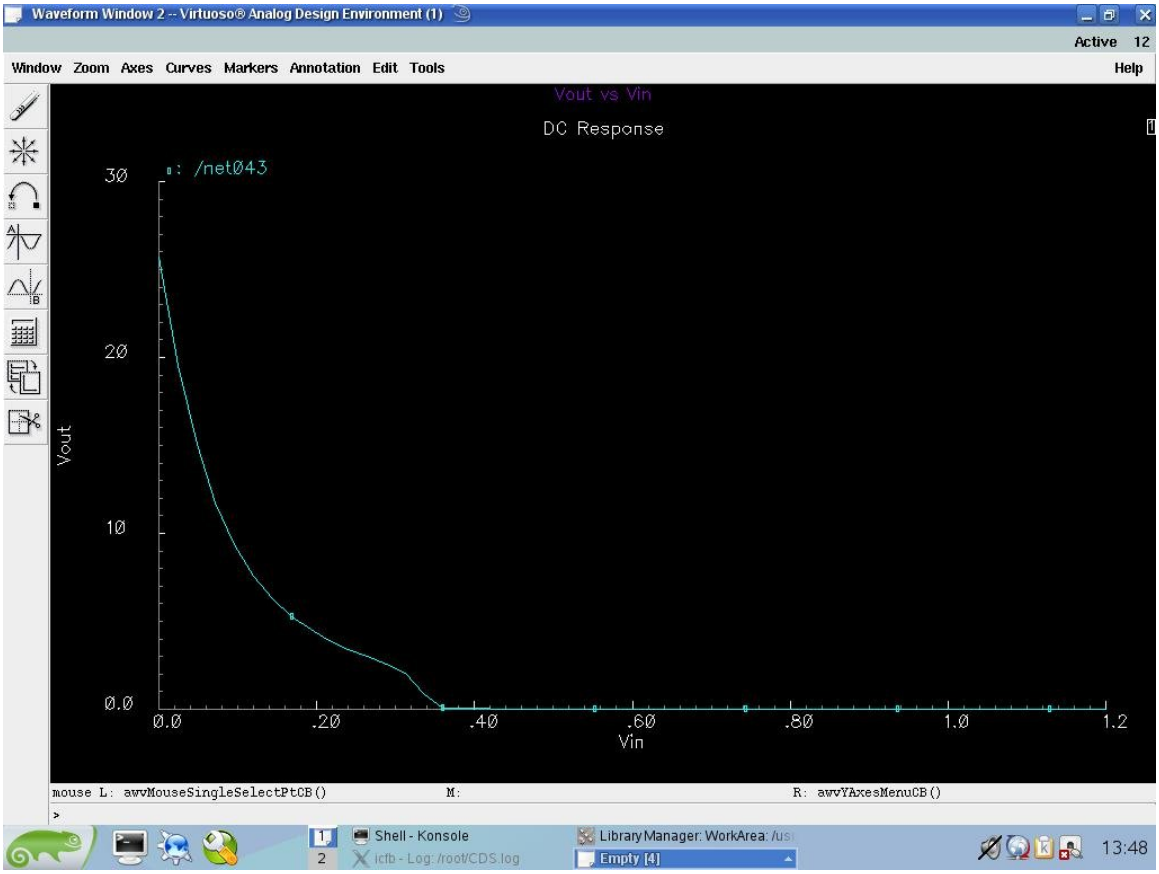
When I plot the gain vs frequency, the specs are met as shown.



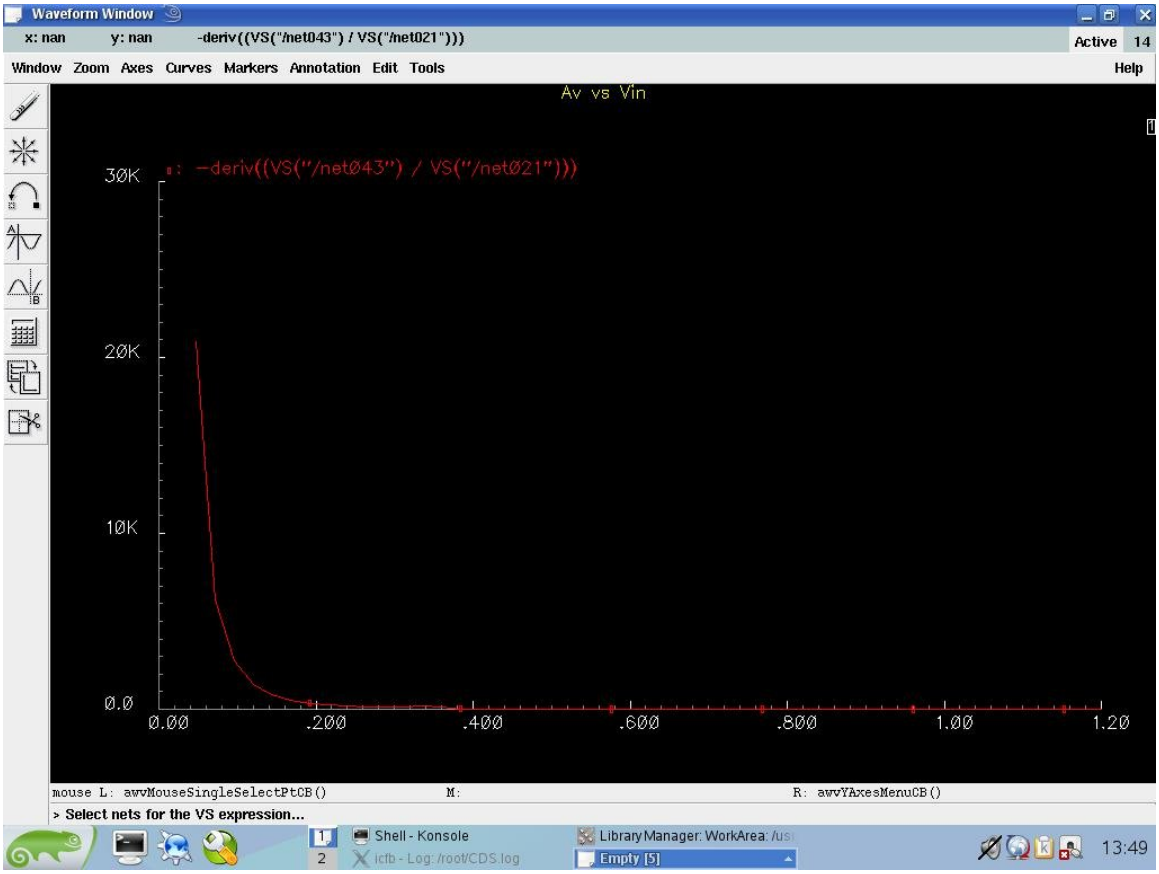
But the problem comes when I plot Vout vs Vin because I get the strange curve as shown. And when I plot (dVout/dVin) vs Vin I get a stranger curve.

I will repeat the plots 2 times : once with an ideal current source and the other with a pmos current source load.

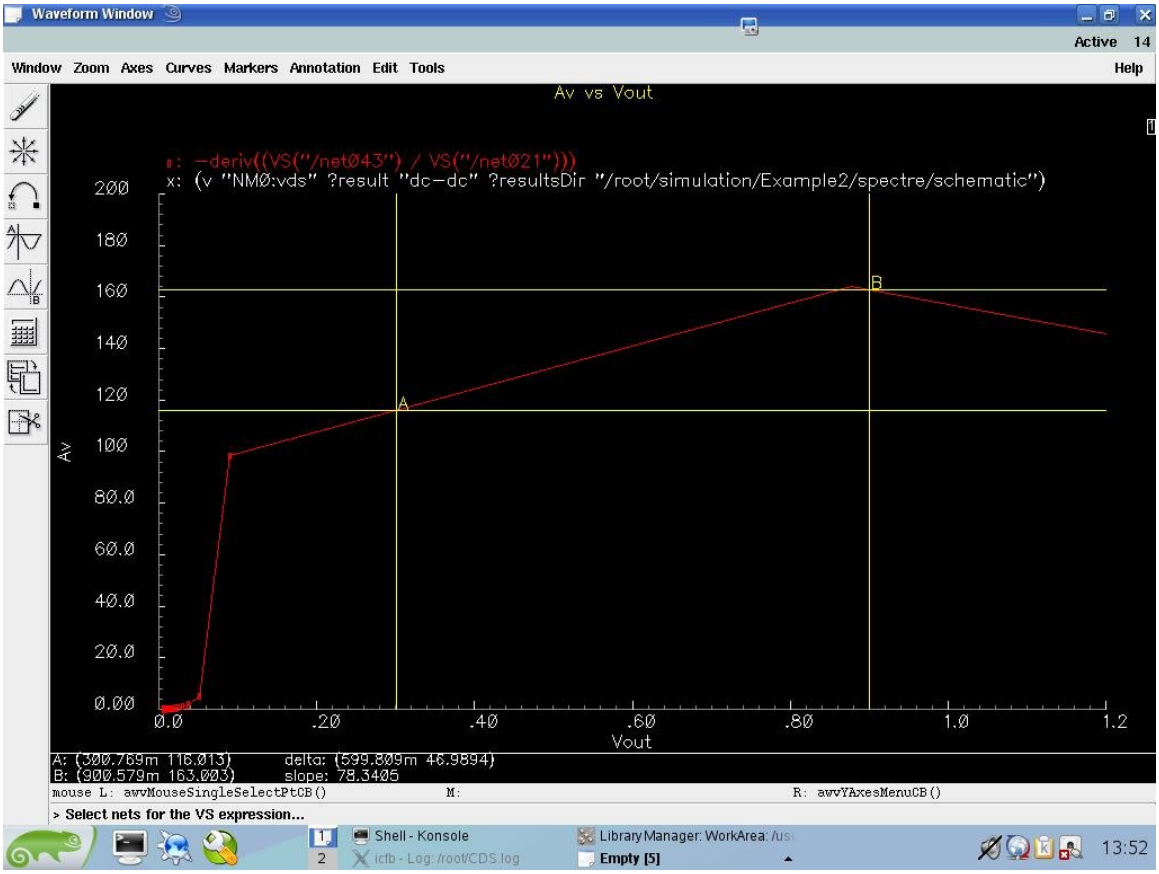
Ideal Current Source :



Vout vs Vin (notice how strange it is)

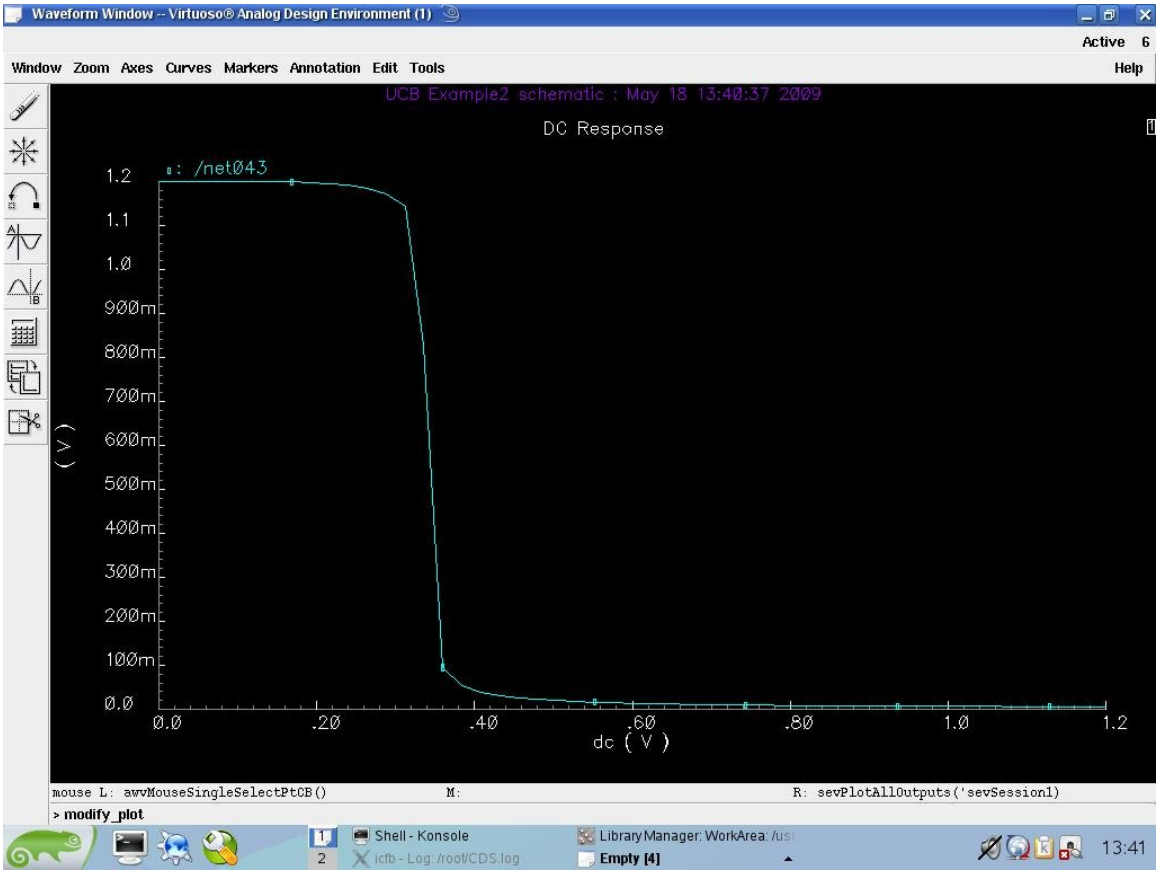

Waveform Window
x: nan
y: nan
-deriv((VS("/net043") / VS("/net021")))
Active
14
Window Zoom Axes Curves Markers Annotation Edit Tools
Help
Av vs Vin
-deriv((VS("/net043") / VS("/net021")))
30K
20K
10K
0.0
0.00
.200
.400
.600
.800
1.00
1.20
mouse L: awvMouseSingleSelectPtCB()
M:
R: awvYAxesMenuCB()
> Select nets for the VS expression...
Shell - Konsole
icfb - Log: /root/CDS.log
Empty [5]
13:49

Av vs Vin

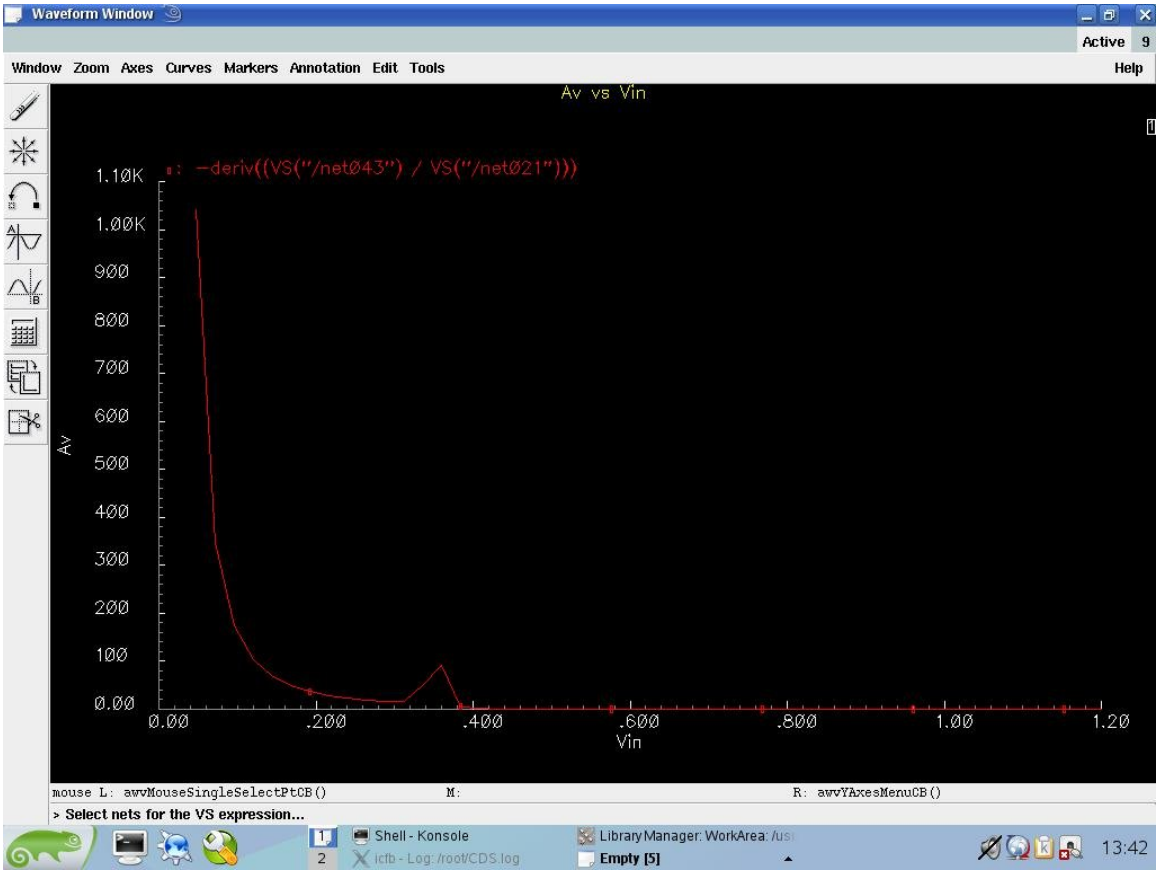


Av vs Vout (although the curve is all filled with break points, it meets the spec but it also exceeds it by far ; a gain of 116 at 300mv although I designed it to have a gain for only 30-40 at that point)

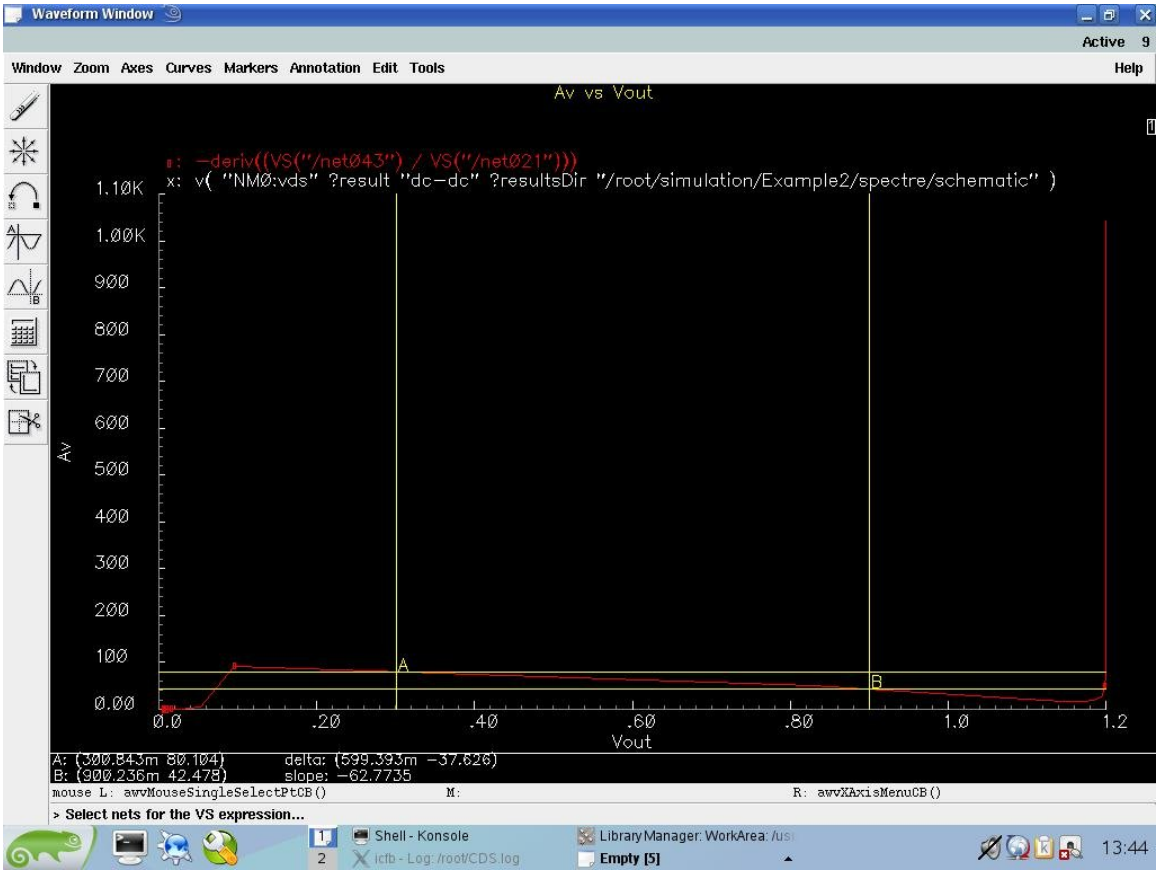
With transistor load :



Vout vs Vin (notice how the curve is shifted to the left)


Waveform Window
Active 9
Window Zoom Axes Curves Markers Annotation Edit Tools Help
Av vs Vin
1: -deriv((VS("/net043") / VS("/net021")))
1.10K
1.00K
900
800
700
600
500
400
300
200
100
0.00
Av
0.00
.200
.400
.600
.800
1.00
1.20
Vin
mouse L: awvMouseSingleSelectPtCB() M: R: awvYAxesMenuCB()
> Select nets for the VS expression...
Shell - Konsole
icfb - Log: /root/CDS.log
LibraryManager: WorkArea: /us
Empty [5]
13:42

Av vs Vin



Av vs Vout (again the specs are met but at 300mv I have a gain of 80 and not 30-40 as I designed it). Also notice how the curve isn't smooth as it should be at all.

Please I want to know what is the problem. Thanks