Design of 2.1GHz RF CMOS Power Amplifier for 3G

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***Abstract*—In the radio frequency (RF) transceiver system, the integration of CMOS power amplifier (PA) remains to be a challenge. In this paper, a PA module is designed, which can be used for 3G mobile communications. A single-ended two-stage Class AB PA is adopted for its higher power efficiency and better linearity. The circuit is simulated by Cadence SpectreS in TSMC 0.25μm CMOS process. As shown by the simulation results: at 2.1GHz under 2.5V, the output power is 1W (30.1dBm) while input power signal is 0dBm, the power gains more than 20dB of broadband within 1.1GHz to 3GHz, and the power added efficiency（PAE）is 51.98%. The layout of the related circuit is drawn by means of the Virtuoso Layout Editor with total size of 1227×1181μm^2.**

Keywords-3G; power amplifier; on-chip inductor; CMOS; RFIC

I. INTRODUCTION

Recently, with rapid development of 3rd generation (3G) mobile communication [1], GPS, WLAN and Bluetooth, CMOS RFIC is recognized as a fascinating candidate to meet the demands of low cost, low power and high capacity technologies. With the unceasing progress of CMOS process technology, most modules in transceiver system can be implemented as monolithic. More and more basic units of RF circuits can be integrated into a single chip [2, 3].

Power amplifier (PA) is an important unit of the wireless transceiver, so designing a high performance PA is the key to improve performance of wireless receivers [4]. However, the designing and implementation of CMOS PA is very difficult. Demands in different aspects of the PA require designers to consider comprehensively how indicators can compromise between one another. In this article, Class AB PA is selected as it displays higher power efficiency as well as linearity. Single-ended two-stage amplification form is used in this design. In order to achieve more efficient match, the monolithic spiral inductor with high quality factor is adopted in the impedance match of RF ports. A good trade-off between linearity and efficiency is obtained at 2.1GHz under 2.5V. This design has demonstrated a simple structure, but with high stability, as well as superior overall performance, which can be used as a transmitter for 3G mobile communication system.

II. POWER AMPLIFIER DESIGN

Power amplifiers involve a balancing of many different parameters, including power added efficiency (PAE), maximum output power, linearity, maximum stable gain, heat dissipation, stability, input/output matching, and breakdown voltage. As with many RF component designs, these requirements are often in conflict with one another. For example, achieving good linearity usually comes at a cost in PAE. Although many such trade-offs face a PA designer, amplifier circuits have been well researched over the years with many different design approaches documented [5, 6]. Single-ended Class AB PAs have been reliable performers in a wide range of applications for a period [7-9]. The arrangement is actually a hybrid combination of Class A and Class B approaches.

Common source structure is used in this circuit. Meanwhile, in order to achieve the gain of more than 20 dB, power amplifier use single-ended two-stage amplification form. Single-ended topology can be avoided application of the balanced-unbalanced transformer [10], which could simplify the integration process and improve the cost efficiency per unit of PA.

Fig.1 shows the overall PA circuit, it includes bias circuit, input matching network, output matching network and inter-stage matching network. A two-stage amplifier bias circuit is composed of L_2, L_3 and DC power V_{GG1}, V_{GG0}.

A suitable quiescent point is provided, so the amplifier works at the mode of Class AB. By improving the input matching, it is possible to achieve the maximum power and

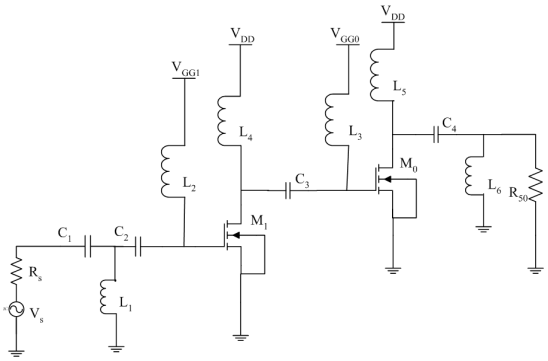

Fig.1. The completed schematic of power amplifier.

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efficiency, diminish signal distortions caused by reflection, and hence enhance linearity, further stabilize the circuit. T-circuit network is composed of C_1, C_2 and L_1, which could be achieved by using input impedance and source impedance (50Ω) match. By simulation, the reflection coefficient of input S_{11} is -24.08 dB. It is small enough to indicate a satisfactory input matching. The high pass L-type output matching network is composed of C_4 and L_6, so load impedance of 50 Ω is transformed to the best load value, thus the required output power can be obtained.

Selecting on-chip inductor is the key to design a matching network, because it determines the quality of the matching network. In view of the factors of self-resonant frequency, Q value and occupied area, then two inductors with 5.5 and 2.5 turns are chosen as L_1 and L_6 respectively, which locate at the input and output matching network [11]. The inter-stage L-type matching network is composed by choke inductance L_4 of the first stage amplifying circuit and MIM (Metal-Insulator-Metal) capacitor C_3 [12]. The best power transmission is achieved by inter-stage matching between the first stage and the second stage. This matching network could also be used to adjust the amplifier gain flatness [13]. The maximum of S_{21} is reached nearby the centre frequency of 2.1GHz by adjusting capacitance, thus the best power transmission can be achieved.

III. Simulation Results

The circuit is simulated by Cadence SpectreS in TSMC 0.25μm CMOS process. As shown in Fig.2, at 2.1GHz, output power is 30.1dBm while input power signal is 0dBm. Moreover, when input power is less than 0dBm, with the increase of input power, output power also increases. But output power stops increasing to a saturation point, once the input power is greater than 0dBm.

Simulation results of the DC current are given in Fig.3. When input power is 0dBm, drain DC current of drive stage is 94.28mA, drain DC current of output stage is 692.4mA, and PAE is about 51.98%. With input power increasing, PAE also increase, as shown in Fig.4.

Fig.5 shows, as two-stage amplification is used, power gain S_{21} is more than 20dB of broadband at the range of 1.1GHz to 3GHz, which meet the design requirements better. 1dB compression point is -26.23dBm and IP3 point is -22.87dBm, as shown in Fig.6.

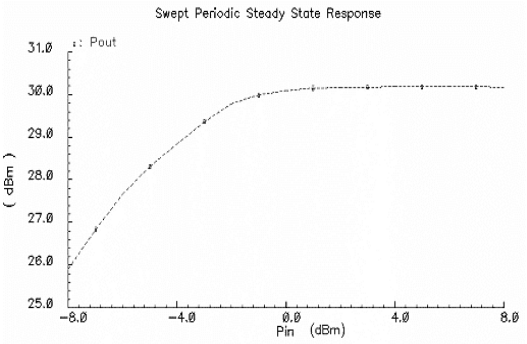
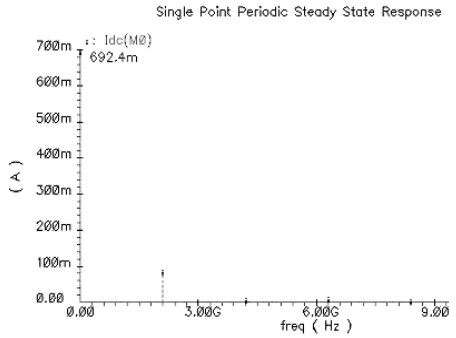
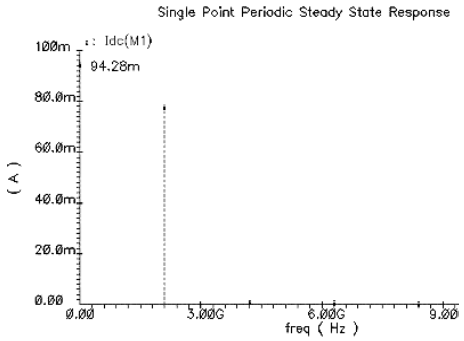


Fig.2. Output Power vs. Input Power.



(a)



(b)

Fig.3. (a) DC current of output stage.
(b) DC current of driver stage.

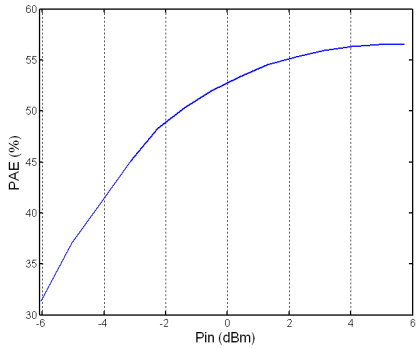


Fig.4. PAE vs. Input Power.

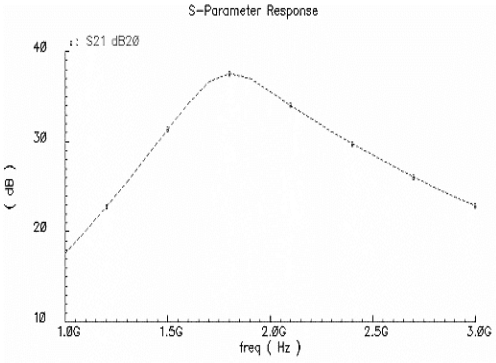
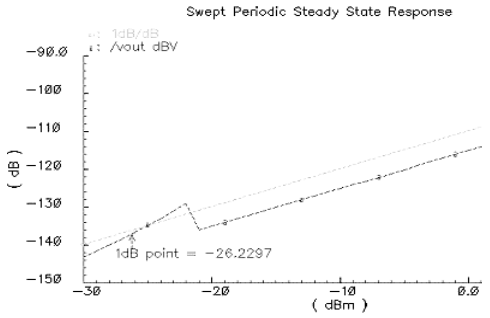
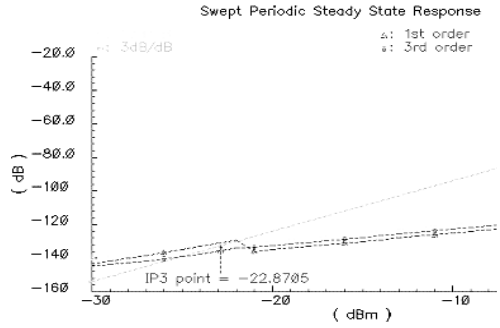


Fig.5. S_{21}.



(a)



(b)

Fig.6. (a) Simulated result of 1dB compression point. (b) Simulated result of the 3rd intermodulation.

IV. Layout of PA with Quadrature Outputs

The layout of the PA is drawn by Virtuoso Layout Editor. Main modules of the layout include MOS transistors, inductors and capacitors. In order to reduce parasitic parameters, interdigital layout is used for MOS transistors designing. Due to restrictions of the design technology, interdigital of MOS transistors should not be too many; otherwise the current density would be too high. Therefore, more MOS transistors are paralleled to meet requirements.

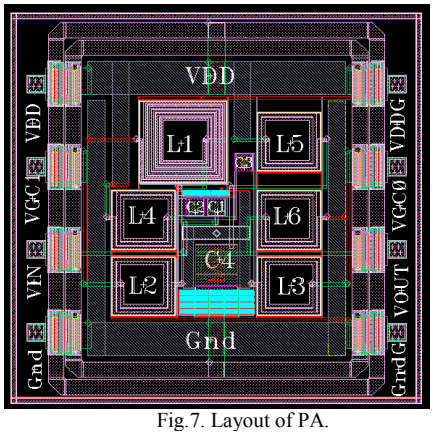


Fig.7. Layout of PA.

There are many inductances within the circuit, so the surrounding components would be interfered due to the function of inductance alternating magnetic field. During the process of the layout, in order to improve the separation of each component, guard ring is used for MOS transistors and on-chip inductors, such method can prevent crosstalk between one another through substrate. MIM plate capacitor is used in this circuit. In addition, ESD protection is deployed at chip-pin department to further stabile performance. Fig.7 is the whole layout of the PA, the final area is $1227\times1181\mu m^2$.

V. Conclusions

A PA module is designed in this paper, based on TSMC 0.25μm CMOS technology for the 3G mobile communications. Common source structure and single-ended two-stage amplification form are used in this circuit. Performance standards are met for the PA. Simulation results by Cadence SpectreS show that at centre frequency of 2.1GHz, the output power is 1 W (30.1dBm), the power gains more than 20dB of broadband at the range of 1.1GHz to 3GHz and the PAE is 51.98%.

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[11] 0.25μm RFCMOS Spiral Inductors Model, T-025-MM-SP-005 Rev.1.6 TSMC 0.25μm Mixed-Signal Salicide (1P5M+ 2.5V/3.3V) RF Spice Models.

[12] 0.25μm RFCMOS MIM Capacitor Model, T-025-MM-SP-005 Rev.1.6 TSMC 0.25μm Mixed-Signal Salicide (1P5M+ 2.5V/3.3V) RF Spice Models.

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