Dear guys,

I would be very happy, if you could help me a little bit further and give me an advice, because I am stuck at the moment. PLEASE!

I did the following:

1. Noise of a Track & Hold stand-alone.

I first built a simple switched-cap (SC) circuit in Cadence together with a Track & Hold (T&H), did a PNoise analysis and compared the results to the theory = your formulas what you provide in your papers (thanks a lot for that! "Simulating switched-capacitor - filters with Cadence SpectreRF").

We see out of Figure 2, not only the integrated noise but also the Root-Spectral-Density (RSD) of the Matlab model of the kT/C noise with a Track & Hold (blue) matches very well to the Cadence circuit results (green).

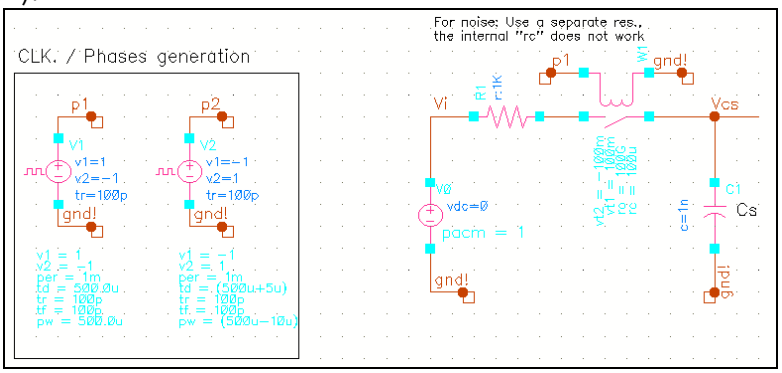


Figure 1 – Test-bench circuit for kT/Cs noise with a Track & Hold (T&H) alone (no subsequent nodes connected where current could flow)

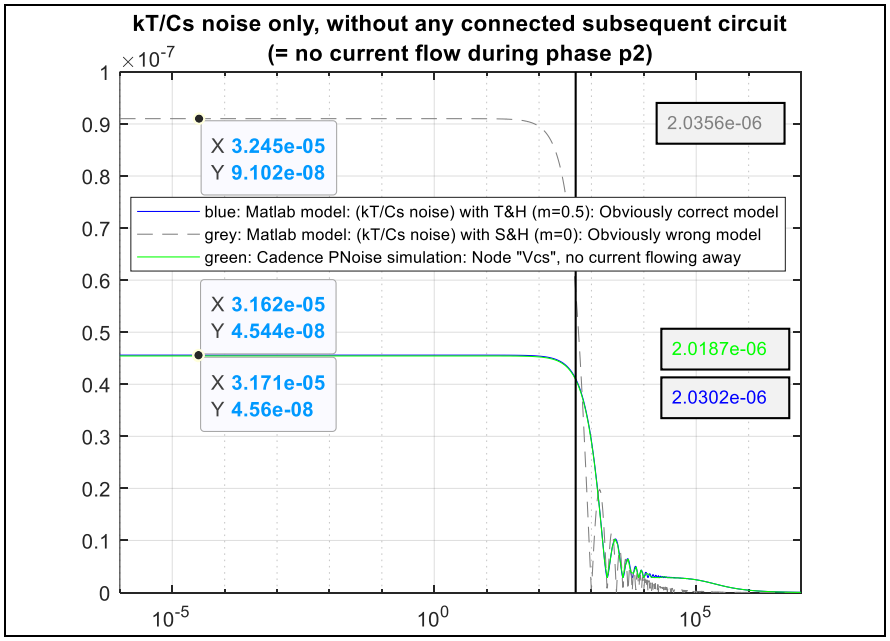


Figure 2 – Matlab model (blue) and Cadence results (green) for kT/Cs noise with a Track & Hold (T&H) alone (no subsequent nodes connected where current could flow)

2. Transfer-function of the switched-cap integrator

I also compared the transfer function of the Cadence circuit reference with the Matlab model of the complete integrator:

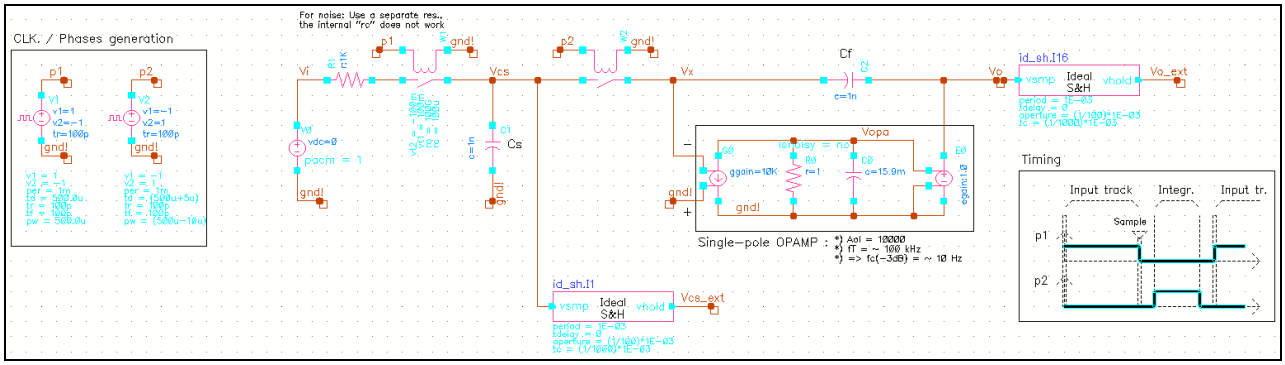


Figure 3 – Test-bench circuit and results for Cadence PAC sampled sim. for a parasitic sensitive SC integrator with data read-out at rising edge of phase "p1"

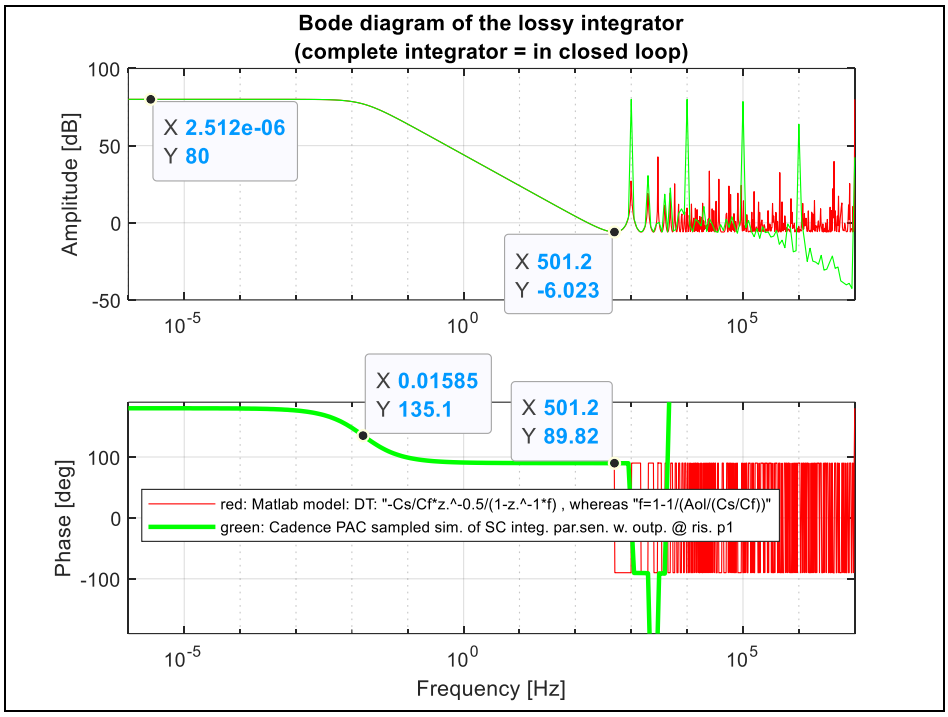


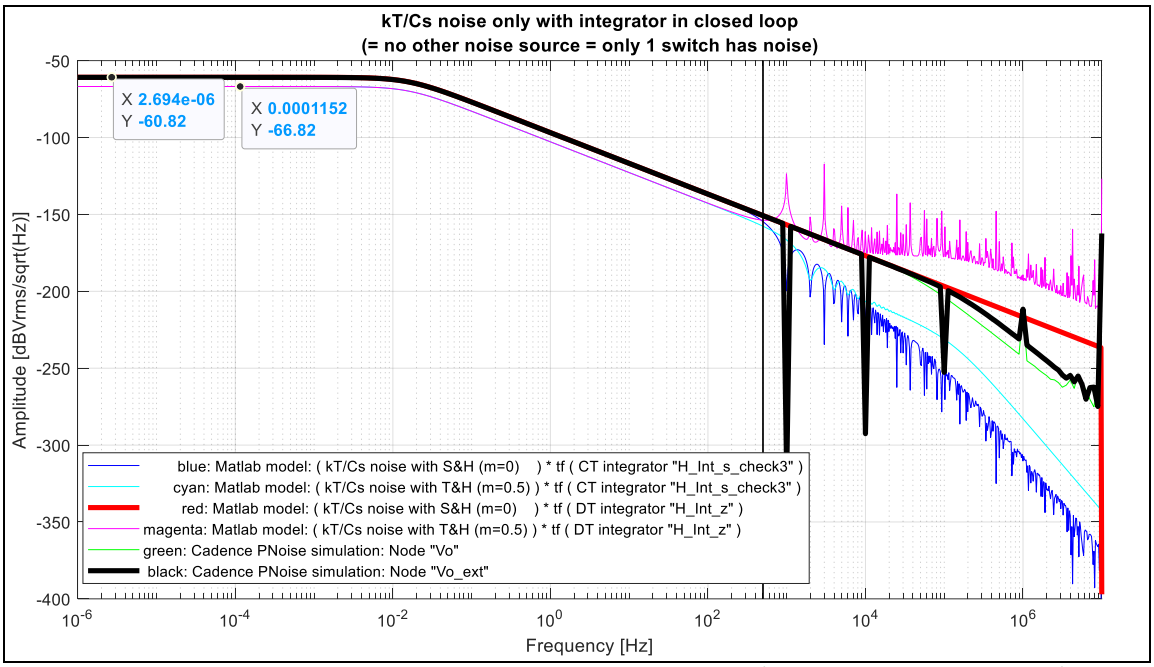
Figure 4 – Transfer functions of Matlab model (red) and Cadence (green) of the lossy integrator; The Cadence SC circuit is with the data read-out at rising edge of phase "p1"

We see out of Figure 4, the DT Matlab model (red) matches perfectly to the Cadence SC circuit (green) up to fs/2.

3. Output-referred noise of the complete SC integrator with kT/C-noise (only)

Now, I tried to obtain the output-referred noise of the complete SC integrator.

The only active noise source is the “kT/Cs”-noise (of the sampling capacitor = only one switch resistance for simplicity). The same schematic is used as in Figure 3 but a PNoise analysis was done (instead of the PAC sampled).

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m_SH = 0;   % The less the duty-cycle, the less components from the track mode & thus it resembles more & more a S&H instead of a T&H
Vn_SH_RSD_vec = sqrt( ((1-m_SH)*sinc(f_vec.*(1-m_SH)*Ts)).^2*2*k*T/(Cs*fs) );          % [Vrms/sqrt(Hz)]
f = 1 - 1 / ( Aol / ( Cs / Cf ) );      % Should model a lossy ( = limited DC-gain) integrator.
Int_z = - Cs / Cf * z.^-0.5 ./ ( 1 - z.^-1 * f);  % This is the exact model (with "z^-0.5") for this type of circuit
kTCs_only_SH_times_tf_Integrator_DT = Vn_SH_RSD_vec' .* abs(Int_z');
semilogx( f_vec , 20*log10( kTCs_only_SH_times_tf_Integrator_DT ) , 'r' , 'LineWidth' , 3 );
```

Figure 5 – Total integrator output-referred noise for the only active kT/Cs noise source (= only one switch resistance for simplicity): Matlab models (with a T&H and S&H, multiplied with CT and DT integrator transfer functions) and Cadence PNoise sim. results

We see out of Figure 5, the DT Matlab model (red) matches very well to the Cadence SC circuit (black) up to fs/2.

My 2 questions = ToBeClarified:

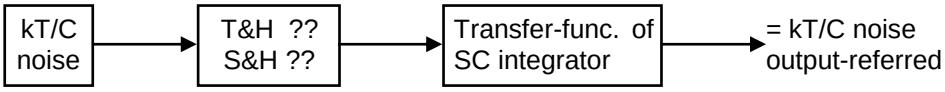
1. Sampling the output with your "Ideal S&H" in the circuit even gives "better matching" results (when compared to Matlab). In the PAC, I can chose specialized "PAC sampled" analysis, but for PNoise it seems there isn't this option. **Is therefore for a correct result of the PNoise analysis your "Ideal S&H" in the circuitry requried additionally and thus to plot the output-referred noise from that (so take node "Vo_ext" instead of just "Vo")**, as shown in the figure? I am interested in the Discrete-Time (DT) behavior since all this then should be part of a delta-sigma ADC.

2. **Why for the "stand-alone" kT/Cs noise connected with a T&H circuit** (= without subsequent integrator where a current could flow in phase p2) **the root-spectral-density (RSD) for the T&H Matlab model gives correct results compared to the Cadence reference** (see Figure 2)**, whereas for the complete = with subsequent integrator, the S&H Matlab model gives correct results** (see Figure 5) **(and here now the T&H model is wrong!) ??**

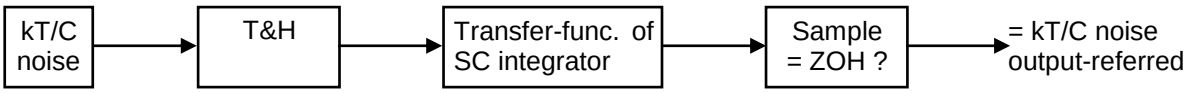
   So from the theory:

   What is from the concept point of view the correct procedure / flow diagram for obtaining the correct discrete-time total integrator output-referred kT/Cs noise and why?

   a) Generate kT/C noise ==> Process it with the T&H and/or S&H (??) ==> Multiply by integrator transfer function ?!



   b) Generate kT/C noise ==> Process it with the T&H ==> Multiply by integrator transfer function ==> Do sampling (again) ??



   But how to do the "sampling" / Zero-Order-Hold mathematically alone? From your paper it seems, just take the PSD output from the previous block and multiply it by the sinc.-function.

   c) …

As said, I would be VERY happy if you could bring some light into this topic!

Many 1000 thanks in advance and best regards from Austria,

Bernd Cettl