Device Mismatch: An Analog Design Perspective

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Abstract— **Device variability is receiving a lot of interest recently due to its important impact on the design of digital integrated systems. In analog integrated circuits, the variability of identically designed devices has long been a concern since it directly affects the attainable precision. This paper reviews the mismatch device models that are widely used in analog design as well as the fundamental impact of device mismatch on the trade-off between different performance parameters.**

I. Introduction

The precision of analog integrated circuit blocks most often depends on the matching of pairs of identically designed devices (see e.g., [1], [2], [3], [4]). For example, the offset of comparators is typically determined by the matching of the gate-source voltage of two nominally identical transistors in a differential input pair; the precision of current-mode digital-to-analog converters depends on the accurate matching of currents in nominally identical transistors biased as current sources; the accuracy of the gain of amplifiers with resistive feedback is set by the matching of resistor ratios, whereas the accuracy of the gain of switched-capacitor based amplifiers relies on the accurate matching of ratioed capacitors. Additionally, contemporary analog circuits use fully differential configurations in order to improve their signal swing under limited supply voltage operation as well as to increase their robustness to supply or substrate interference. As such, many performance parameters of analog circuits depend on the matching between identically designed components.

This has resulted in a long history of investigations over many technology nodes on characterizing and modeling the mismatch of devices, including some of the underlying physical causes. In this paper we briefly review the models used in analog design to model device mismatch. We further discuss how device mismatch affects the design of analog circuit blocks and how it fundamentally impacts the trade-off between different performance parameters of analog circuits [3], [4].

II. Device mismatch models

The mismatch of two closely spaced, identical MOS transistors has been extensively investigated down to deep-submicron device sizes. The experimental data shows that threshold voltage differences ΔV_T and current factor differences $\Delta\beta$ ($\beta = \mu C_{ox} W/L$) are the dominant sources underlying the drain-source current or gate-source voltage mismatch for a matched pair of MOS transistors. These random differences have a normal distribution with zero mean and a variance dependent

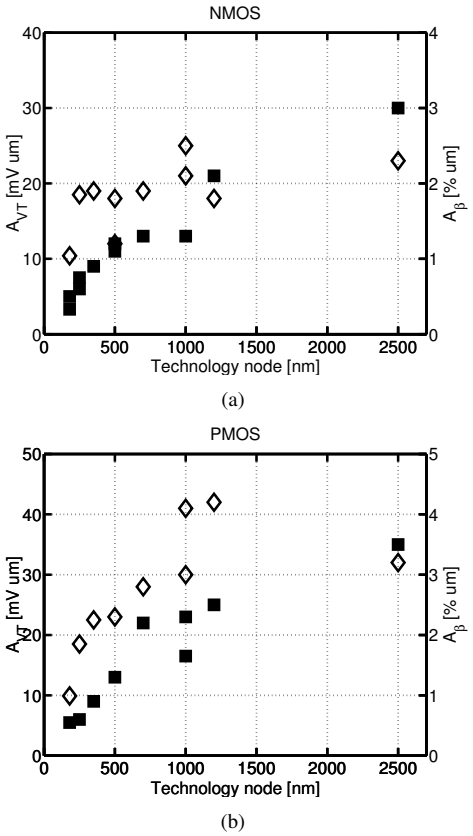

Fig. 1. Matching parameters A_{VT} (■) and A_β (◇) from different technology nodes for nMOS (a) and pMOS (b) devices.

on the device area $W \cdot L$ [5], [6]:

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{W \cdot L}, \tag{1}$$

$$\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 = \frac{A_\beta^2}{W \cdot L}, \tag{2}$$

where W is the gate-width and L the gate-length, and the proportionality constants A_{VT} and A_β are technology-dependent. Although V_T and β have some common process parameter dependencies, the experimental data further shows a low correlation between ΔV_T and $\Delta\beta$ and the assumption that they can be modeled as *independent* random variables is generally accepted [6]. Fig. 1 summarizes the proportionality constants for several industrial CMOS processes published in open literature [4].

The validity of the area dependence for parameter matching

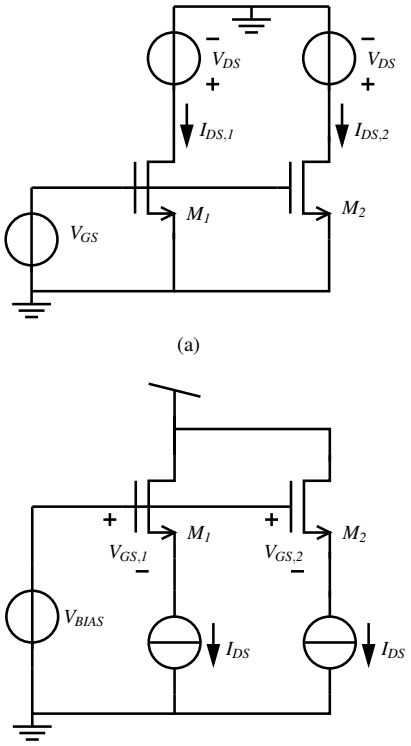

Fig. 2. Two basic biasing arrangements for a pair of nMOS devices: voltage biasing (a), where transistor variations result in variations in the drain-source currents I_{DS}; or current biasing (b), where transistor variations result in variations in the gate-source voltages V_{GS}.

has been demonstrated for a wide range of technologies and device sizes. However in deep sub-micron technologies, the matching of very narrow devices or very short devices deviates from the simple area dependence and more extensive models are required. Down to sub-micron technologies, the width and length edge variations were sufficiently small that they could be largely neglected in the models shown in (1) and (2), but recent results from poly gate variation studies in deep sub-micron technologies could indicate that a more extensive mismatch models might be required in the future.

III. Effect of device mismatch on analog design

In analog circuit applications, two types of errors are typically of interest. For the voltage biased pair in Fig. 2(a), the current matching error, $\Delta I_{DS} = I_{DS,2} - I_{DS,1}$ between the respective drain-source currents $I_{DS,1}$ and $I_{DS,2}$ of M_1 and M_2 determines the circuit accuracy. The gate-source voltage error, $\Delta V_{GS} = V_{GS,2} - V_{GS,1}$, sets the accuracy in a current biased configuration shown in Fig. 2(b). These errors can be expressed in terms of the ΔV_T and $\Delta\beta$ of the matched device pair biased in saturation:

$$\left(\frac{\sigma(\Delta I_{DS})}{I_{DS}}\right)^2 = \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + (g_m/I)^2\sigma^2(\Delta V_T), \quad (3)$$

$$\sigma^2(\Delta V_{GS}) = \sigma^2(\Delta V_T) + \left(\frac{1}{(g_m/I)}\right)^2\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 \quad (4)$$

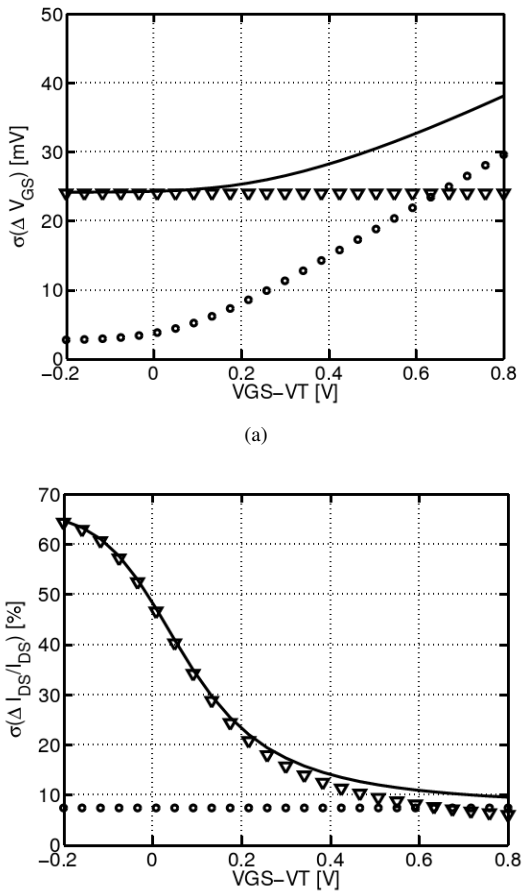

Fig. 3. Drain source current (-) (a) and gate-source voltage (-) (b) mismatch for a 0.25 μm/0.25 μm nMOS transistor in a 0.25 μm CMOS technology with $A_{VT} = 6\ mV\mu m$ and $A_\beta = 1.85\%\mu m$ [4]; the contributions from V_T mismatch ($-\triangledown-$) and β mismatch (-o-) are also shown separately.

where (g_m/I) depends on the bias point chosen by the designer. These current and voltage errors and the contributions of the threshold voltage and current factor mismatches are plotted in Fig. 3 for bias points ranging from weak inversion to strong inversion[1].

The best voltage matching can be achieved for bias points with a low gate-source overdrive, i.e. for operation towards weak inversion; the best current matching can be achieved by using a bias point with a large gate-source overdrive, i.e. deep into strong inversion[2]. It is further important to note, that for gate-source overdrive voltages of up to several hunderd milivolts, the contribution of the threshold voltage mismatch to

[1]Expressions (1) and (2) only provide first order models for the parameter mismatches and do not take into account the possible bias dependence of these parameters. This can affect the accuracy of the error calculations in (3) and in (4), but for the purpose of the development of design insights and the trade-off analysis presented in this paper, their accuracy is sufficient.

[2]The possible higher threshold voltage mismatch coefficient A_{VT} in weak inversion could require the use of a bias point more towards moderate inversion; the possibly adverse effect of velocity saturation has also not been accounted for in these first order models; however, these second-order effects will most likely not substantially change the trends in optimal bias point selection.

the voltage or current matching errors strongly dominates over the current factor mismatch contribution. As such, the effect of threshold mismatch is the most prominent effect, especially in view of the decreasing supply voltages of scaled CMOS technologies.

IV. Fundamental impact of device mismatch on analog performance trade-offs

In analog design three primary performance specifications are often the operation speed (or bandwidth, BW) of the circuit, its accuracy and the associated power consumption, P. Significant design effort is focused on reducing the power consumption for the required speed and accuracy.

The operation speed of a circuit or functional block is typically related to the transit frequency f_T of the devices; for a device with a width W, a length L and biased in saturation with a drain-source current I_{DS}, $BW \propto f_T = g_m/(2\pi C_{gs}) \propto ((g_m/I)I_{DS})/(C_{ox}W \cdot L)$. The power consumption of the circuit operating from a power supply V_{DD} is proportional to $I_{DS}V_{DD}$ and the power-bandwidth trade-off is set by

$$\frac{P}{BW} \propto \frac{C_{ox}V_{DD}}{(g_m/I)} \cdot W \cdot L, \tag{5}$$

and is directly linked to the area of the device. If low power consumption and high operation speed are the only concerns, the designer will use minimum size devices[3]. However, when minimum size devices are used, the device mismatch increases and the accuracy of the circuit will degrade. The accuracy, Acc_v, for a voltage processing circuit is set by the ratio of the signal swing $V_{s,RMS}$ and the offset voltage V_{os}; $V_{s,RMS}$ is a fraction of the available power supply so that $Acc_v \propto (V_{DD}/\sigma(V_{os}))$. For typical operating points in sub-micron CMOS circuits, the threshold voltage mismatches are the dominant source of the offset so that, using (1) $\sigma(V_{os}) \propto A_{VT}/\sqrt{WL}$. The impact of the accuracy specifications on the power-speed trade-off can now be clearly established in

$$\frac{P}{BWAcc_v^2} \propto C_{ox}A_{VT}^2 \cdot \frac{1}{(g_m/I)V_{DD}}, \tag{6}$$

and we find that the power-speed-accuracy trade-off is largely fixed by a technology dependent constant $C_{ox}A_{VT}^2$ sometimes called the "matching energy" [1]. Apart from some optimization in (g_m/I) through the bias point selection, the required power consumption for an analog circuit to achieve a given speed and accuracy performance is fixed by technology constants.

In analog circuits the achievable precision can also be limited by the effect of thermal noise on the smallest signal that can be processed. The power spectral density of the equivalent voltage noise source at the input of a MOS device is $S_{Vn} = 4kT \cdot (2/3) \cdot 1/gm$ and assuming that the circuit bandwidth is a fraction of the device f_T, the variance of the noise voltage becomes $\sigma^2(V_{n,RMS}) \propto kT/(C_{ox}WL)$. When we want to compare the effect of thermal noise on the circuit operation versus the effect of mismatch errors, we can evaluate

$$\frac{\sigma^2(V_{os})}{\sigma^2(V_{n,RMS})} \propto \frac{C_{ox}A_{VT}^2}{kT}. \tag{7}$$

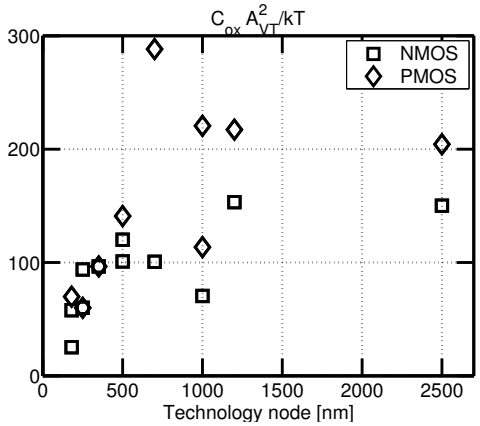

Fig. 4. Ratio of the 'matching energy' to the 'noise energy' over several MOS technology nodes.

Fig. 4 shows the ratio of the matching energy, $C_{ox}A_{VT}^2$, to the noise energy, kT, for several technology generations [4]. The effect of mismatch is clearly dominant over the effect of noise by one or several orders of magnitude. This analysis quantifies the design intuition which existed among analog designers for a long time, that the device sizing and circuit performancce in offset sensitive circuits is set by mismatch requirements rather than noise considerations.

This trade-off between operation speed, accuracy and power consumption can be worked out from the building block circuit level (see e.g., [4]) to the level of analog systems (see e.g., [3], [1]). The resulting strong power constraints imposed by mismatch have resulted in the development of several architectural solutions for analog systems to ease the impact of device mismatch. Once the devices are fabricated, the mismatch is stationary over time, which is the underlying property that is exploited in all such solutions. For example, the cricital devices in each IC can be trimmed after fabrication before using the IC. This is a very expensive solution often requiring special technology options as well as test equipment and can only be applied in high-end applications. Auto-zero calibration is a circuit technique that relies on temporarily shutting of the signal processing function of the circuit to perform an automatic calibration and thus requires sampled data operation or the availability of dead times in the operation. Several other circuit or system level techniques have been used to address the mismatch of components. From the overall system level perspective, the overhead of these techniques is typically sufficiently small compared to the substantial power savings that can be achieved.

V. Device mismatch scaling with technology

A reduction in the A_{VT} for the smaller technology nodes can be observed in Fig. 1 and can be related the impact of random dopant fluctuations which is the dominant physical

[3]In this derivation we are only considering the on-chip loads in the circuits; it does not apply to circuits whose load is set by fixed (off-chip) elements that do not scale with the transistor sizing.

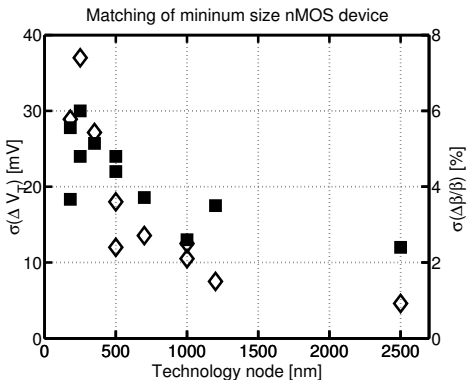

Fig. 5. $\sigma(\Delta V_T)$ (■) and $\sigma(\Delta\beta/\beta)$ (◇) for a minimal nMOS device in different technology nodes.

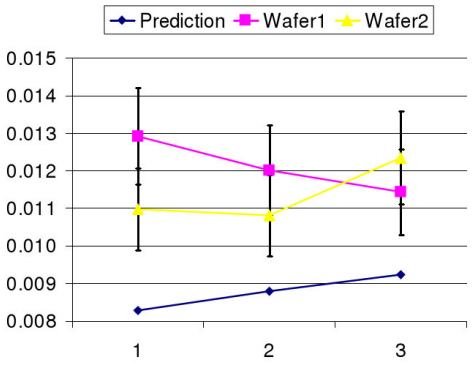

Fig. 6. Measured relative frequency mismatch of closely spaced ring oscillator pairs and the predictions based on DC mismatch parameters for V_T and β only.

cause of V_T mismatch. The A_β on the other hand is not changing significantly with technology node scaling for the data available in the same Figure.

The matching energy $C_{ox}A_{VT}^2$ reduces for smaller technology nodes (see Fig. 4) due to a stronger influence of the A_{VT} reduction compared to the C_{ox} increase. Consequently, a device with a constant area fabricated in finer technology nodes will have a lower mismatch. However, with technology scaling, the area of the circuits and the size of the devices is typically reduced. Fig. 5 shows the mismatch of a minimum size nMOS device w.r.t. technology node feature size; this mismatch of minimum size devices is degrading substantially as we are moving into deep-sub-micron CMOS technologies. Traditionally for the design of digital systems, circuit designers did not have to deal with the effects of device variability or mismatch. The increasing mismatch of minimum size devices combined with the impact of poly gate variations and other variability phenomena which are becoming more prominent as technology scales further, help to explain the strong impact device variations are having on the design of digital systems in deep-sub-micron CMOS technologies.

VI. Matching of non-static circuit operation

In many applications we need to know the matching of the non-static operation of devices. Whereas the mismatches in the DC characteristics will automatically lead to mismatches in the transient or AC behavior of circuit blocks, an open question is if additional mismatch effects will occur under these operating conditions. Given that digital circuits operate non-statically, this question needs to be answered in order to fully understand the effect of device mismatches on digital design.

Modern RF transceivers often rely on parallel signal paths that need to be matched to obtain accurate signal processing. For example, the matching between the I and Q signal path in a direct-conversion receiver directly impacts the attainable image rejection. A thorough understanding the matching of the non-static operation of circuits is thus also required to enable the accurate prediction of the matching of RF circuits.

In Fig. 6 the measured relative mismatch of 3 pairs of closely spaced matched ring oscillators with respectively 3, 5 and 7 stages in a 0.25um CMOS technology is shown [7]. The oscillator stages are sized appropriately to obtain a identical frequency operation for all pairs close to 1.4 GHz. The shorter rings use larger active devices with lower intrinsic mismatch but have less averaging over the stages; the longer rings average the mismatch errors over more stages but the stages use smaller devices to maintain the same operation frequency and have more mismatch. The measured mismatch of the 3 pairs is statistically equivalent which indicates that the averaging by using more stages is equivalent to the averaging by using larger devices.

The predicted frequency mismatch based on the DC mismatch parameters for the V_T and β mismatch is also shown in Fig. 6. There is a statistically significant difference between predicted and measured results. Several possible underlying causes are being investigated. In contrast to circuits which require matching of static circuit operation around a fixed bias point, the matching of the ring oscillators requires a matching of the devices at several bias points. Additionally, it is possible that mismatch of device or parasitic capacitors are significant enough to introduce extra mismatch errors.

References

[1] M. Pelgrom, "Low-power high-speed AD and DA conversion," in *Low Power - Low Voltage Workshop (ESSCIRC'94)*, September 1994.

[2] P. Kinget and M. Steyaert, "Impact of transistor mismatch on the speed-accuracy-power trade-off of analog CMOS circuits," in *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, May 1996, pp. 333–336.

[3] K. Bult, "Analog design in deep sub-micron CMOS," in *Proceedings European Solid-State Circuits Conference (ESSCIRC)*, September 2000, pp. 11–17.

[4] P. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1212–1224, June 2002.

[5] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. 21, no. 6, pp. 1057–1066, December 1986.

[6] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, 1989.

[7] A. Balankutty, T. Chih, C. Chen, and P. Kinget, "Mismatch characterization of ring oscillators," submitted.