**Specifications:** An audio amplifier is to deliver an average power of 0.1 W to an 8 Ω speaker from a microphone that produces a 10 mV peak sinusoidal signal and has a source resistance of 10 kΩ.

**Design Approach:** A direct, perhaps brute force, approach will be taken in this design. The generalized multistage amplifier configuration that will be designed is shown in Figure 6.76. An input buffer stage, which will be an emitter-follower circuit, is to be used to reduce the loading effect of the 10 kΩ source resistance. The output stage will also be an emitter-follower circuit to provide the necessary output current and output signal power. The gain stage will actually be composed of a 2-stage common-emitter amplifier that will provide the necessary voltage gain. We will assume that the entire amplifier system is biased with a 12 volt power supply.

**Solution (Input Buffer Stage):** The input buffer stage, an emitter-follower amplifier, is shown in Figure 6.77. We will assume that the transistor has a current gain of $\beta_1 = 100$. We will design the circuit so that the quiescent collector current is $I_{CQ1} = 1$ mA, the quiescent collector-emitter voltage is $V_{CEQ1} = 6$ V, and $R_1 \| R_2 = 100$ kΩ.

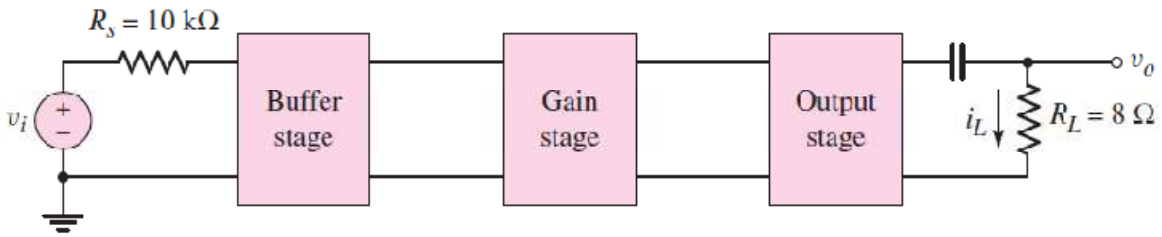


Figure 6.76 Generalized multistage amplifier for design application

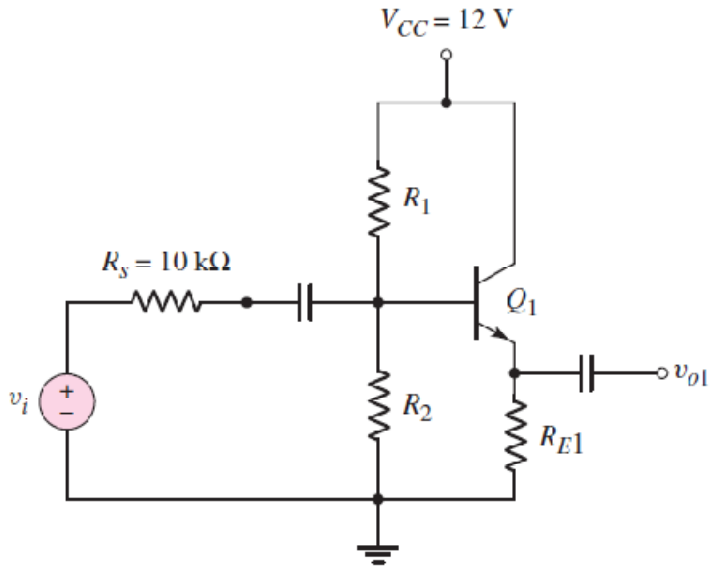


**Figure 6.77** Input signal source and input buffer stage (emitter-follower) for design application

We find

$$R_{E1} \cong \frac{V_{CC} - V_{CEQ1}}{I_{CQ1}} = \frac{12 - 6}{1} = 6 \text{ k}\Omega$$

We obtain

$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{CQ1}} = \frac{(100)(0.026)}{1} = 2.6\,\text{k}\Omega$$

We also have, neglecting the loading effect of the next stage,

$$\begin{aligned} R_{i1} &= R_1 \| R_2 \| [r_{\pi 1} + (1+\beta_1) R_{E1}] \\ &= 100 \| [2.6 + (101)(6)] = 85.9\,\text{k}\Omega \end{aligned}$$

The small-signal voltage gain, from Equation (6.68) and assuming that $r_o = \infty$, is (again neglecting the loading effect from the next stage)

$$\begin{aligned} A_{v1} &= \frac{v_{o1}}{v_i} = \frac{(1+\beta_1)R_{E1}}{r_{\pi 1} + (1+\beta_1)R_{E1}} \cdot \left( \frac{R_{i1}}{R_{i1} + R_S} \right) \\ &= \frac{(101)(6)}{2.6 + (101)(6)} \cdot \left( \frac{85.9}{85.9 + 10} \right) \end{aligned}$$

or

$$A_{v1} = 0.892$$

For a 10 mV peak input signal voltage, the peak voltage at the output of the buffer stage is now $v_{o1} = 8.92$ mV.

We find the bias resistors to be $R_1 = 155\,\text{k}\Omega$ and $R_2 = 282\,\text{k}\Omega$.

**Solution (Output Stage):** The output stage, another emitter-follower amplifier circuit, is shown in Figure 6.78. The 8 Ω speaker is capacitively coupled to the output of the amplifier. The coupling capacitor ensures that no dc current flows through the speaker.

For an average power of 0.1 W to be delivered to the load, the rms value of the load current is found from $P_L = i_L^2(\text{rms}) \cdot R_L$ or $0.1 = i_L^2(\text{rms}) \cdot 8$ which yields $i_L(\text{rms}) = 0.112$ A. For a sinusoidal signal, the peak output current is then

$$i_L(\text{peak}) = 0.158\ \text{A}$$

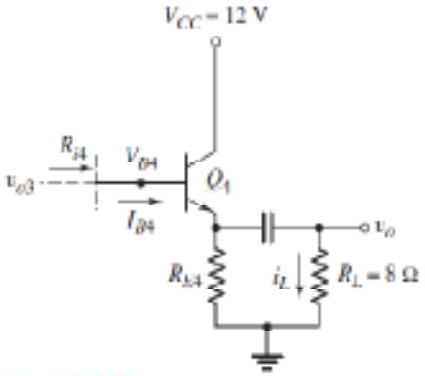


Figure 6.78 Output stage (emitter follower) for design application

and the peak output voltage is

$$v_o(\text{peak}) = (0.158)(8) = 1.26 \text{ V}$$

We will assume that the output power transistor has a current gain of $\beta_4 = 50$. We will set the quiescent transistor parameters at

$$I_{EQ4} = 0.3 \text{ A} \qquad \text{and} \qquad V_{CEQ4} = 6 \text{ V}$$

Then

$$R_{E4} = \frac{V_{CC} - V_{CEQ4}}{I_{EQ4}} = \frac{12 - 6}{0.3} = 20\ \Omega$$

We find

$$I_{CQ4} = \left(\frac{\beta_4}{1 + \beta_4}\right) \cdot I_{EQ4} = \left(\frac{50}{51}\right)(0.3) = 0.294 \text{ A}$$

Then

$$r_{\pi 4} = \frac{\beta_4 V_T}{I_{CQ4}} = \frac{(50)(0.026)}{0.294} = 4.42\ \Omega$$

The small-signal voltage gain of the output stage is

$$A_{v4} = \frac{v_o}{v_{o3}} = \frac{(1 + \beta_4)(R_{E4} \| R_L)}{r_{\pi 4} + (1 + \beta_4)(R_{E4} \| R_L)}$$

$$= \frac{(51)(20 \| 8)}{4.42 + (51)(20 \| 8)} = 0.985$$

which is very close to unity, as we would expect. For a required peak output voltage of $v_o = 1.26$ V, we then need a peak voltage at the output of the gain stage to be $v_{o3} = 1.28$ V.