IMTC 2006 – Instrumentation and Measurement
Technology Conference
Sorrento, Italy 24-27 April 2006

Some Critical Notes on DAC Time Domain Specifications

Eulalia Balestrieri
Department of Engineering, University of Sannio,
Corso Garibaldi 107, 82100, Benevento, Italy
Phone: +39-0824-305817, Fax: +39-0824-305840, E-mail: balestrieri@unisannio.it

Abstract *– The paper analyzes a set of DAC time domain specifications including DAC settling time, rise time and fall time, glitch energy. Some useful comments are provided in order to highlight ambiguity in the mostly used definitions and new definitions are suggested when it is necessary.*

Keywords *– DAC, settling time, rise time, fall time, glitch.*

I. INTRODUCTION

Digital-to-Analog Converters (DACs) are essential components providing a link between digital and analog sections of a mixed-signal system. Optical networking, 3G cellular and 802.16 base stations, high-end medical imaging, cellular and smart-phones, MP3 players, digital video camcorders are only a few examples of applications requiring a DAC.

The interest in these devices is growing, both from the scientific and the industrial worlds. A large number of scientific papers has been published during the last years [1-5] and the Waveform Measurement and Analysis Technical Committee (TC-10) of the IEEE Instrumentation and Measurement Society started a project for publishing a new standard on DAC terminology and test methods [6].

Standardization plays an important role for the evaluation and comparison of existing devices that are made by different manufacturers in different parts of the world. Unique and unambiguous DAC parameter definitions avoid possible misinterpretations of the real device performance and make the right selection of a DAC for a specified application easy and properly done.

The main aim of this paper is to give contributions and ideas for discussion related to the new DAC standard. The research described has been carried out to provide a unified approach to DAC standardization concerning terminology. Therefore, a comprehensive overview on DAC terminology taken from existing standards, scientific literature and manufacturers' documentation has been done highlighting similarities, ambiguities and lacks in the parameter definitions. Then, DAC specifications have been chosen considering that each parameter has to be unambiguously defined and practically measurable.

The already existing or the most used definitions coming from the collected references have been entirely adopted, if possible, or modified or completely rewritten to provide a final set of DAC specifications to satisfy the above reported requirements.

Previous work [7] provided some critical notes on DAC static parameter definitions, suggesting definitions for resolution, full scale range, LSB (Least Significant Bit), offset and gain, INL (Integral NonLinearity) and DNL (Differential NonLinearity).

This paper describes the continuation of the previous work considering DAC dynamic parameter definitions in the time domain. Each proposed definition, since referred to a parameter that has to be measurable, is joined with its measurement unit taking as reference the International System of Units (SI). Since some DAC specifications (where possible), could be derived from the ADC ones with the appropriate changes, the IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters (IEEE Std. 1241) [8] has been used as guideline.

The paper considers a set of DAC time domain specifications including DAC settling time, rise time and fall time and glitch energy. Some useful comments to highlight ambiguity in the mostly used definitions are provided and new definitions are suggested and discussed.

II. SETTLING TIME

The importance of settling time in a data conversion system is that certain analog operations must be performed in sequence, and one operation may be accurately settled before the next operation can be initiated [9]. In DACs this parameter gives information about the time required by the converter to meet the right output value after a change in the input code.

DAC settling time has three distinct components (Fig.1). The *delay* (or *dead*) *time* is very small and during this interval there is no output change. During *slew time*, instead, the output amplifier moves at its highest possible speed towards the final value. *Ring time* (also referred to as *recovery time* plus *linear settling*) defi nes the region where the amplifier recovers from slewing and ceases movement within some defined error band [10].

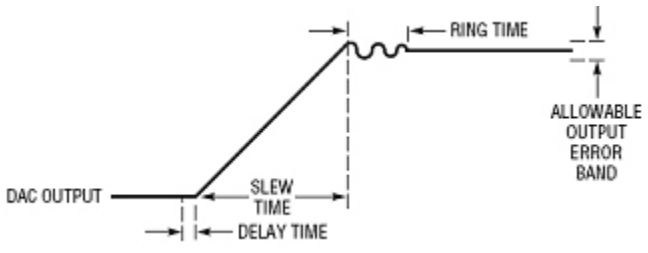

Fig. 1. DAC Settling Time Components [10].

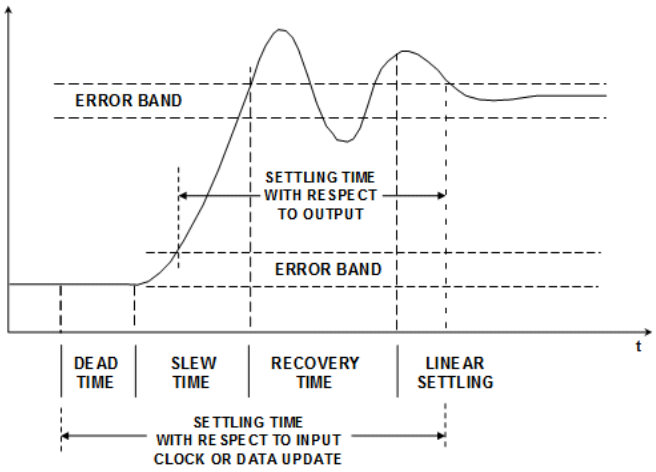

Fig. 2. DAC settling time [11].

A. Definitions in technical standards

Several different definitions for this parameter can be found, mostly depending on the beginning and ending instants chosen that can include or not the delay time or only a part of the slew time, or the considered error band amplitude. The most traditional definition is "*the amount of time required for the output to settle with the specified error band measured with respect to the 50% point of either the data strobe to the DAC (if it has a parallel register driving the DAC switches) or the time when the input data to the switches changes (if there is no internal register)*" [11], (Fig.2). Another definition considers the settling time with respect to the instant when the output leaves the initial error band excluding the dead time from the measurement [11], (Fig.2).

IEC Standard 60748-4 [12] reports three definitions: *digital*, *reference, and steady-state ramp settling time* taking into account also the reference voltage variations in multiplying DACs. The former is included in the digital characteristics of a linear or multiplying DAC considering as starting instant a "*change at the digital input, the reference voltage being constant*". The latter two are, instead, included in the reference signal characteristics of a multiplying DAC, referring to a "*change of the reference voltage, the digital input being constant*". So the *digital settling time* is "*the time interval between the instant when the digital input changes and the instant when the analog output value enters for the last time a specified error band about its final value*". The *reference settling time* is "*the time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output enters for the last time a specified error band about its final value*".

The *settling time to steady-state ramp* is "*the time interval between the instant a ramp in the reference voltage starts and the instant when the analog output value enters for the last time a specified error band about the final ramp in the output*", (Fig. 3).

The same three definitions quoted above are reported in the JEDEC Standard No.99 A.01 [13], together with the definition of *analog settling time* as "*the time interval between the instant when the analog output passes a specified value and the instant when the analog output enters for the last time a specified error band about its final value*".

The *final value* is not really determined in many cases. Long tails due to thermal or dielectric absorption effects can led to long term settling phenomena. Aware of this, IEEE Std. 1241 defines the *settling time* as "*the time at which the step response enters and subsequently remains within a specified error band around the final value, measured from the mesial point (50%) of the response. The final value is defined to occur 1s after the beginning of the step*". IEEE Std. 1241 limits the observation time to 1s because changes in the final value occurring after this time interval are considered drift and may be due to room temperature fluctuations, component aging and similar effects. However, for some application, taking measurements after 1 s is impossible or doesn't make sense. For this reason IEEE Std. 1241 introduces the *short-time settling time* "*measured from the first mesial point (50%) of the output, is the time at which the step response enters and subsequently remains within a specified error band around the final value. The final value is defined to occur at a specified time less than 1s after the beginning of the step*". In this case, the measurement of the final value is made before 1s but the measurement time should be specified by the operator.

The more recently released IEEE Std. 181 [14] states that the word time refers exclusively to an instant and not an interval. So the term settling time, although widely used, is deprecated because ambiguous and confusing. Despite of settling time IEEE Std. 181 defines the *transition settling duration* as "*the time interval between the 50% reference level instant, unless otherwise specified, and the final instant the waveform crosses the state boundary of a specified state in its approach to that state*". This standard considers as a deprecated term also the word "mesial" which is replaced with the 50% reference level.

B. Defining step amplitude

All the definitions discussed until now don't give information about which code has to be chosen to produce the

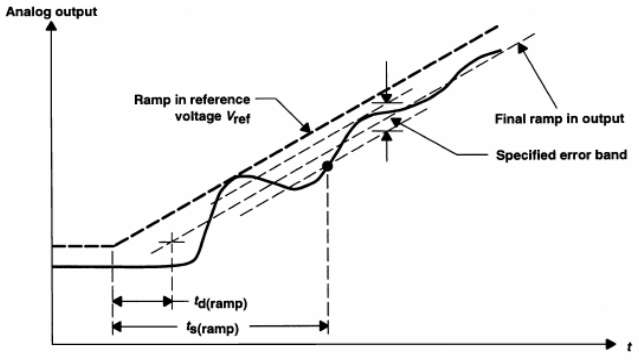

Fig. 3. DAC settling time to steady-state ramp [13].

initial and final output levels. Clearly the greater the output step change, the longer the settling time. Reference [15] states that "*the DAC must settle from any output level to any other level within the specified time*", this means that millions of transitions on a typical DAC should be measured.
Obviously, this solution is very time consuming and economically unacceptable, so the suggested approach consists in determining and measuring the codes representing the worst-case transitions.
Some converters settle faster in one direction than the other, if bipolar operation is considered, voltage output in the negative going direction can settle much more slowly than in the positive direction [16]. Therefore, the DAC transitions typically considered for the settling time measurement are "*those from minus full-scale to plus full-scale and viceversa, since they represent the larger voltage swing*" [15]. However, the worst-case transitions could not be always these. In a binary-weighted DAC, for example, the mid-scale settling time is also of interest, because, the transition between the 0111…1 code and the 1000…0 code produces the largest transient [11].

C. Defining error band

Concerning the error band, it could be expressed as a percentage "*of the full-scale range, of the final voltage or of a fixed voltage*" [15] or in terms of an LSB [11].
Clearly the greater the error band, the shorter the settling time. Establishing a unique value for the error band involves some considerations about DACs with different resolutions. If the settling time error band is described as ± 1/2 LSB, a DAC with 10 V full scale range and 8 bit resolution has an allowable error band of ± 20 mV. Considering other two DACs with same full scale range but 10 bit and 12 bit resolution, the first has a ± 5 mV error band, the latter has a ± 1.22 mV error band [16]. This doesn't mean that the 12 bit DAC is slower than the 8 bit DAC, it is simply required to settle to a more tightly specified error band [16].

D. Manufacturers' approaches

Concerning the manufacturers' documentation several different settling time definitions are provided, too. It is a time interval measured starting from the beginning of the output transition [17,18] or "*the 50% point of the full scale*" [19] or more generally once the DAC has accepted a command to change its output value [20] until the output is stable within a defined error band. The error band could be expressed in LSB or in percent of "*full scale voltage*" [19] and could be defined between ± 1⁄2 LSB or some other specified tolerance of the final value [21]. Reference [22] adds that the settling time is usually specified "*for a full-scale 10 V transition*".
Manufacturers' documentation definitions are quite similar to those reported in the standards. However, also in this case an agreement concerning the starting instant from which to compute the settling time is missing. Often information about the error band amplitude or the DAC transition considered is provided, but the problem of the final value determination is not taken into account and the reference voltage variations in multiplying DACs as well.

E. Proposed definitions

From the presented state of art of the settling time definitions some comments can be drawn. Starting from the two parameter definitions with respect to the input and to the output, in the former case the settling time measurement is clearly more complete since includes all its components (dead time, slew time, recovery time and linear settling). However, this kind of definition involves considering two different signals (at the input and at the output of the DAC) requiring a more complex test bench, (an instrument with at least two channels is needed). On the contrary, defining the settling time with respect to the output, involves the analysis of only the DAC output signal and consequently a more immediate measurement. However, since it is often difficult to identify the transition starting instant, setting an output amplitude threshold is necessary. The 50% point stated in [8] and [14] as triggering threshold is fairly unambiguous, and is not affected by noise, such as clock or trigger transients, which can mislead the observer into believing that the transition has started. Another problem addressed by definitions reported in [8] is the determination of the final value to be considered in the settling time computation. Because of the presence of noise, and specifically 1/f noise, the final value is not really determined in many cases. IEEE Std. 1241 suggests the 1s time interval as a good compromise as after this time the transition can be measured statically with instruments like digital voltmeters.
As quoted above, when waiting for 1s is not allowable, another settling time definition (the short term settling time in [8]) has to be considered.
The problem concerning the name of the parameter introduced by the IEEE Std. 181, related to the ambiguity of the word time both to refer to an instant and an interval, could be addressed with the simple addition of the word "interval" after settling time. In this way it would be possible to preserve the traditional parameter name taking into account its currently wide use.
All these considerations led to the following proposed definitions.
In the case of settling time with respect to the input two different definitions are suggested:
The settling time interval is the time interval measured from the instant when the digital input changes and the instant at which the step response enters and subsequently remains within a specified error band around the final value. The final value (unless otherwise specified) is defined to occur 1s after the beginning of the step. Unless otherwise specified the worst-case transition has to be considered.
The short-term settling time interval is the time interval measured from the instant when the digital input changes and the instant at which the step response enters and subsequently remains within a specified error band around the final value. The final value is defined to occur at a specified time less than

1s after the beginning of the step. Unless otherwise specified the worst-case transition has to be considered.

In the case of settling time, with respect to the output, two definitions are proposed, too:

The output settling time interval is the time at which the step response enters and subsequently remains within a specified error band around the final value, measured from 50% point of the response. The final value (unless otherwise specified) is defined to occur 1s after the beginning of the step.

The output short-term settling time interval is the time at which the step response enters and subsequently remains within a specified error band around the final value, measured from 50% point of the response. The final value is defined to occur at a specified time less than 1s after the beginning of the step. Unless otherwise specified the worst-case transition has to be considered.

These definitions require the specification of the error band, the time at which the final value is defined to occur and the transitions considered as the worst case. Information about the error band considered is essential considering that some 14 and 16-bit DACs specify settling time to the 12-bit level, because of measuring the settling time with an error band of 1 LSB at the 16-bit resolution is a real instrumentation challenge [11]. Four is the minimum number of definitions to take into account the settling time measurements including all its components (*settling time interval)* and those don't (*output settling time interval)* as well as applications for which is not allowable waiting for 1s to determine the final value (*short-term settling time interval* and *short-term output settling time interval*).

In case of multiplying DACs other two definitions are needed: the *reference settling time interval* and the *settling time to stead-state ramp* as suggested by IEC 607478.

The former is "*the time interval between the time when a specified step change of the reference voltage occurs and the instant when the analog output enters and subsequently remains within a specified error band around the final value*". The latter is "*the time interval between the instant a ramp in the reference voltage starts and the instant when the analog output value and subsequently remains within a specified error band about the final ramp in the output*".

III. RISE TIME AND FALL TIME

These parameters give information about the slew time component of the settling time. For this reason IEC 60748 associates their definition to the slope time, that is "*for a step-function change of the input signal level, the time interval between the end of the delay time and the instant at which the magnitude of the output signal first passes through a specified value close to its final value*". The delay time quoted in the previous definition is "*the time interval between a step-function change of the input signal level and the instant at which the magnitude of the output signal passes through a specified value close to its initial value*".

IEC 60748 adds in a note that the amplitude threshold normally specified for the end of the delay time (the beginning of the slope time) is 10% of the final value, while the ending level is 90%.

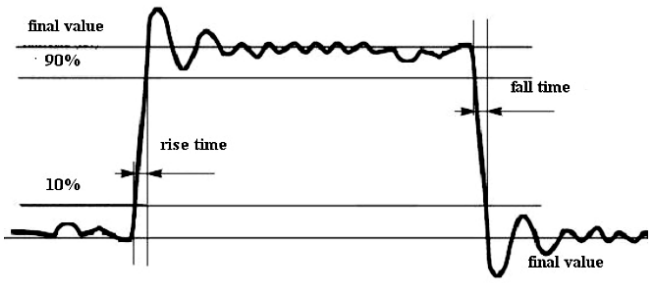

Fig. 4. DAC rise and fall time.

IEEE Std. 1241 rise time definition states it is "*the time for the signal to go from 10% to 90% of the transition range*", while the fall time is "*the time for the desired signal to go from 90% to 10% of the transition range*", (Fig.4). In this case the two definitions don't depend on that provided for the delay time or on the kind of change in the applied input signal. However, understanding what is the transition range is essential. IEEE Std. 1241 deals with the transition range in the section entitled "Digital logic signals" as "*the range between the lower (base) and the higher signal level (top)*".

In the place of the transition range, the full scale step is considered in [19] to define the rise time.

Concerning the amplitude percent levels between whose the rise and fall times have to be computed, they can be 10/90% or 20/80% [23] as well as 30/70% [15].

Rise and fall time are deprecated terms in IEEE Std. 181, first for the use of the word time to represent an interval, and then because "*if the first transition of a waveform happens to be a negative transition, some users may refer to its transition duration as its rise time, and some others may refer to its transition duration as its fall time*". The two parameters are, therefore, replaced with the *transition duration* defined as "*the difference between the two reference level instants of the same transition. Unless otherwise specified, the two reference levels are the 10% and 90% reference levels*".

It is clear that the transition duration of a positive-going transition corresponds to the rise time and to the fall time in case of transition duration of a negative-going transition.

As quoted in the case of the settling time the problem highlighted by the IEEE Std. 181, can be solved adding the word interval after rise and fall time.

Rise and fall time obviously assume different values depending on the code transition applied to the DAC. Moreover, they have to be coherent with the settling time interval definition, since they represent a part of this parameter, measuring them in a different way doesn't make sense. Therefore, all the quoted above comments led to the following proposed definitions.

The rise time interval is the time for the signal to go from 10% to 90% points (unless otherwise specified) of the output response corresponding to the specified worst case output signal change.

The fall time interval is the time for the signal to go from 90% to 10% points (unless otherwise specified) of the output response corresponding to the specified worst case output signal change.

The wordings "*output response*" and "*specified worst case output signal change*" make these definition suitable also in the case of the *reference settling time interval* and the *settling time to stead-state ramp*, since they are not strictly related to a code transition or a step response.

IV. GLITCH

A *glitch* is generated when during a code transition the new code signal value appears before or after the signal value of the former code disappears [24].

DAC glitch can arise from two mechanisms: capacitive coupling of digital transitions to the analog output, and the effects of some switches in the DAC producing temporary spurious outputs since they operate more quickly than others [11]. Capacitive coupling frequently produces roughly equal positive and negative spikes which more or less disappear in the longer term. The glitch produced by switch timing differences is generally unipolar, much larger, and of greater concern [11].

IEC 60748-4 defines glitch as "a *short, undesirable transient in the analog output following a code change at the digital input*".

The *glitch area* is "*the time integral of the analog value of the glitch transient*", specifying that usually, the maximum specified glitch area refers to a specified worst-case code change.

Finally, the *glitch energy* is "*the time integral of the electrical power of the glitch transient*". In this case, usually, the maximum specified glitch energy refers to a specified worst-case code change.

IEEE Std. 181 provides a more general definition stating the glitch is "*a transient that leaves an initial state, enters the boundaries of another state for a duration less than duration for state occurrence, and then returns to the initial state*".

Reference [15] defines the *glitch energy or glitch impulse* as "*the total area of the glitches in a DAC's output as it switches across the largest major transition (i.e. 01111111 to 10000000 in an 8-bit DAC) and back again*". The parameter is expressed in picosecond-volts (psV) or equivalently picovolt-seconds (pVs).

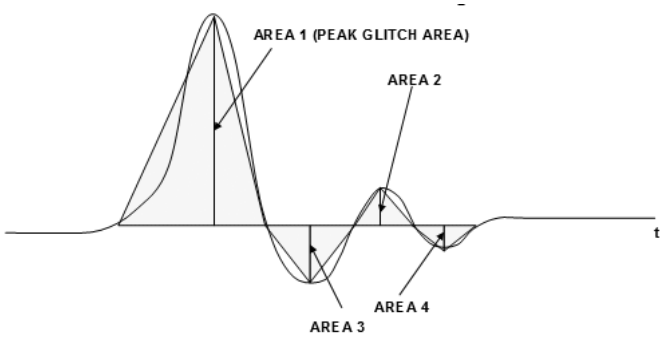

Fig. 5. DAC glitch impulse area [11].

This definition is different respect to the reported one in the IEC standard because it is theoretically incorrect since it refers to an energy a quantity that is not an energy.

The glitch area is defined as "*the area that falls outside the rated error band*". Moreover, the authors of [15] add that "*the area under the negative glitches is considered positive area and should be added to the area under positive glitches"* and "*both the rising-edge glitch energy and the falling edge glitch energy should be tested*".

Glitch impulse area in [11] is estimated from the mid-scale settling time waveform as a sum of triangle areas built as shown in Fig.5. If the total positive area equals the total negative glitch area, then the net area is zero. The specification given on most data sheets is the net glitch area, although in some cases, the peak area may be specified instead [11].

The glitch area is also assumed to be triangular in shape in [24], but in this case it is measured considering the area under the first peak only. The reported reason is that in this way a more realistic specification for board and system level designers is provided as they can more adequately evaluate the severity of the glitch [24].

The use of square impulses instead of the triangle ones for modelling glitches is considered in [25] as a worst case estimation of the glitch impulse area.

Most of the manufacturers' datasheets relate the glitch energy or impulse definition to the major carry transition [26,27,28] as done in [15], without citing the error band. This is determined to be ± ½ LSB in [23] and "*± 2% of full scale*" in [19].

Concerning the measurement unit of the glitch energy most of the definitions use volt-second (Vs) (pico or nano-volt), not actually units of energy, only [15] uses also joule (J). This can be explained by the widespread habit of using the term glitch energy or impulse to refer to the area under the curve on a voltage-versus-time plot. However, [11] clearly considers the term glitch energy a misleading name for indicating glich area.

Although the largest glitch is mostly generated by a major carry transition around the MSB level [25], it can be present at whatever code transition. An example is reported in [24], where for the Intersil HI5721 [29] the worst case glitch is the 0000011111 to 1111100000 transition. This is achieved by the split R/2R-segmented current source architecture, which decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range [24].

Another important consideration is that taking into account or not error bands as well as different error band width produce different glitch energy values.

Usually datasheets don't specify if the area under the negative-going spike is subtracted from the area under the positive spike, or if it is added to determine the glitch energy. It's clear that the glitch energy value obtained is different depending on these two cases. In the same way the glitch energy value changes if both the rising edge and the falling edge glitch energy are considered or not.

Therefore, a good glitch definition should include all the above information to avoid confusion and ambiguity.
The definitions proposed by IEC 60748-4 are theoretically proper. The glitch area and energy, in fact, don't express the same quantity and are defined as time integrals, without using any approximation. Moreover, there is no ambiguity between energy and area. However, as quoted above the glitch area is often estimated as a sum of areas computed by an approximated waveform (triangular or square shape). The glitch area and energy definitions should take into account this diffused normalcy.
The code transition considered has to refer to the worst case and the error band has to be specified. Another question concerns if only the first transient of the DAC output has to be considered in computing the glitch area and energy or not.
When considering the glitches due to data input changes, the secondary spikes are due to settlement effects that can compensate each other and are not the preeminent contributes, being the first spike much bigger than the others.
All these comments led to the following proposed definitions.
Glitch is the first transient peak in the analog output falling outside the specified error band subsequently a code change at the digital input.
The glitch area is the time integral of the analog value of the glitch transient that falls outside a specified error band following a specified worst-case code change. This parameter can be computed by using integral approximations that have to be always specified. The glitch area is expressed in volt per second (Vs).
The glitch energy is the time integral of the electrical power of the glitch transient that falls outside a specified error band following a specified worst-case code change. This parameter can be computed by using integral approximations that have to be always specified. The glitch energy is expressed in watt per second (Ws) or joule (J).

V. CONCLUSIONS

Finding common characteristics in the DAC parameter definitions cannot be taken for granted, as well to come to an agreement among all the references.
In the paper the need for a unique set of DAC specifications including both the end-user and the manufacturers point of view has been highlighted. Several definitions for the main DAC dynamic time domain parameters coming from different sources have been collected, compared and discussed in order to achieve a unique set of definitions.
The proposed definitions have been written considering that each parameter has to be unambiguously defined and practically measurable.

AKNOWLEDGMENT

The author wishes to thank Sergio Rapuano, Jerome Blair and Solomon Max for their technical support.

REFERENCES

[1] E. Balestrieri, P. Daponte, S. Rapuano, "Digital to analog converters: a metrological overview", Proc. of the 9th Workshop on ADC Modelling and Testing, Athens, Greece, September 29th - October 1st 2004, vol. 2, pp.875-880.
[2] P. Kiss, J. Arias, D. Li, V. Boccuzzi, "Stable high-order delta–sigma digital-to-analog converters", IEEE Trans. on Circuits and Systems I, vol.51, No.1, pp.200-205, Jan. 2004.
[3] M. Albiol, J. L. González, E. Alarcón, "Mismatch and dynamic modeling of current sources in current-steering CMOS D/A converters: an extended design procedure", IEEE Trans. on Circuits and Systems, vol.51, No.1, pp.159-169, January 2004.
[4] P. Crippa, C. Turchetti, M. Conti, "A statistical methodology for the design of high-performance CMOS current-steering digital-to-analog converters", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol.21, No.4, pp.377-394, April 2002.
[5] K. L. Parthasarathy, R. L. Geiger, "Unambiguous characterization and specification of D/A converter performance", Proc. of 2000 Midwest Symposium on Circuits and Systems, pp. 890-894, August 2000.
[6] IEEE Std. 1658 Draft, "IEEE Standard for terminology and test methods for digital-to-analog converters", 2005.
[7] E. Balestrieri, S. Moisa, S. Rapuano, "DAC static parameter specifications - some critical notes", Proc. of 10th IMEKO TC4 Workshop on ADC Modelling and Testing, Gdynia and Jurata, Poland, 12-15 September 2005, vol. I, pp.81-86.
[8] IEEE Std. 1241, "IEEE Standard for terminology an test methods for analog-to-digital converters", 2000.
[9] Intersil, AN 002, "Principles of data acquisition and conversion", Oct. 1986, available at www.intersil.com.
[10] J. Williams, "Component and measurement advances ensure 16-bit DAC settling time", Linear Technology Corp, AN 74, July 1998.
[11] W. Kester, "Evaluating high speed DAC performance", Analog Device, MT-013, January 2006, available at www.analog.com.
[12] IEC 60748-4, Semiconductor Devices – Integrated Circuits – Part 4: Interface integrated circuits – Sec. 2: Blank detail specification for linear analogue-to-digital converters, Second edition, 1997.
[13] JESD99A.01, "Terms, Definitions, and Letter Symbols for Microelectronic Devices", May 2003.
[14] IEEE Std. 181, "IEEE Standard on transitions, pulses, and related waveforms", 2003.
[15] M. Burns, G. W. Roberts, "An introduction to mixed-signal IC test and measurement", Oxford University Press, 2001.
[16] Analog Device, "Analog-digital conversion handbook", Prentice Hall, 1986.
[17] Analog Device, "Data converters: high speed digital-to-analog converters glossary", available at www.analog.com.
[18] Atmel, "Data converter terminology", Application Note, available at www.atmel.com.
[19] Philips, "Mixed signal testing cookbook", Nat. Lab. Report 7103, ver. 2.1 - October 1999.
[20] Maxim, "ADC and DAC glossary", Application Note 641, December 2000, available at www.maxim-ic.com.
[21] National Semiconductor, "D/A converters - definition of terms", May 1999, available at www.national.com.
[22] Linear Technology, "Component and measurement advances ensure 16-Bit DAC settling time", Application Note 74, July 1998.
[23] B. Jasper, "Practical telecom DAC testing", available at www.testedgeinc.com
[24] J. Garcia, S. G. LaJeunesse, "Understanding glitch in a high speed D/A converter", Intersil Corporation, TB 325.1, January 1995, available at www.intersil.com.
[25] R. J. Van de Plassche, "CMOS integrated analog-to-digital and digital-to-analog converters", Kluwer Academic Publishers, Boston, 2003.
[26] Analog Device, AD5602/AD5612/AD5622 datasheet, available at www.analog.com.
[27] Maxim, MAX5290-MAX5295 datasheet, available at www.maxim-ic.com.
[28] Texas Instruments, DAC8554 datasheet, available at www.ti.com.
[29] Intersil, HI5721 datasheet, available at www.intersil.com.