Jerry Twomey
Effective Electrons
Phone: 760-522-5090
Email: jerry@effectiveelectrons.com

www.effectiveelectrons.com
www.ieeeconsultants.com/members/Twomey.HTM
3144 Cabrillo Bay Lane,
San Diego, CA 92110, USA

IC's: Analog, Mixed Signal, & RF
Semiconductor/Foundry/SPICE Models

Interference Noise Solutions
Design/Training/Review/Troubleshooting

- **Integrated Circuit product development and staff training**
- **Technical Oversight of custom IC's for OEM's.**
- **Experienced in high frequency design, analog circuits, interference & inherent noise, ESD & I/O design, ADC's, DAC's, PLL's, Filters, and micro-power methods.**
- **IC's designed in CMOS, BiCMOS, CMOS-SOI, Silicon-Germanium (SiGe) BiCMOS, and Bipolar foundry processes. Conversant in foundry, semiconductor modeling, process technology and radiation hardening issues. Expertise in "not seen in simulation" issues.**

Experience:
November 2003 - Present: **Effective Electrons,** San Diego California – IC Design, Technical Consulting, Training Seminars, and OEM support services. Client activity:

- June-August 2008 –PCIE transmitter, Low Power Oscillators, 45nm CMOS (Qualcomm, San Diego, CA)
- May-April 2008 –Configuration of Cadence Mixed Signal EDA (Tektronix, Beaverton Oregon)
- October 2006 – December 2007 – 90nm SOI design PLL Frequency synthesizers, ESD, I/O Cells, LVDS Receiver/Transmitter, Verilog-AMS PLL models (ATK Mission Research, Albuquerque NM)
- August 2006 – March 2007 – Medical, muscle motion stimulus system (Breg-Orthofix, Vista CA)
- July 2006 – EDN Magazine – Technical writer covering 43rd Design Automation Conference
- June – July 2006 – Technical training seminars (Kriptic Devices, Kuala Lumpur Malaysia)
- March 2005 – May 2006 - 65nm CMOS IC for 20 GB/sec data over MPP super-computer backplane transmitter/receiver. (Cray Inc. – Chippewa Falls Wisconsin, Seattle Washington)
- January – March 2005 – Control system for optical data systems. (Ceyx Technologies, San Diego)
- September – December 2004 – EM simulation for RF signal paths at 6-18GHz. (IBM, San Jose CA)
- April – September 2004 – RF front end - gmC filters for UWB receiver. (Alereon, Austin Texas)
- January 2004 – February 2005 – Custom IC for satellite communication. (Shin Satellite – Thailand & Codespace – Hood Oregon)

October 2002 – October 2003: **Axiom Microdevices**, Orange/Anaheim, California
CMOS RF Power Amplifiers for GSM cell phones. Series A start-up included IC design, layout, technical infrastructure, and staffing activities. This included:

- RF Front end driver circuits for PA
- PSS - linearity, phase noise
- ESD I/O design
- PA Power management and control
- Design team staffing
- IT and EDA support
- Foundry/Process Qualification

September 2000 – August 2002: **IBM - RF Design Center,** Encinitas, California
Wireless IC Design: Development of direct conversion receivers for 3G cellular phones, WCDMA, GSM, UMTS, CDMA 2000 cellular standards. This included:

- Spur reduced PLL charge pump
- GSM gain, noise & linearity analysis
- Enhanced linearity LNA biasing
- Active RC filters and gmC filters
- WCDMA analog base-band
- Sigma-Delta ADC for CDMA 2000
- Auto-compensated process circuits
- New foundry processes: RF-CMOS & SiGe

July 1998 – September 2000: **Fairchild Semiconductor,** San Diego, California
Mixed signal IC design: designer and technical mentor for the department.
Designs included:

- ADC,14 bit, VCO/counter
- ADC, 8 bit, 50 MHZ, pipeline
- DAC, 10 bit, 300 MHz, I-steering
- Li-ion battery protection IC for cellular
- Thermal monitor IC for Intel-uP
- LDO micro-power, 35 uA, for cellular
- PLL, 300MHz, for clock recovery

February 1996 - June 1998: **LSI Logic - Mixed Signal Design Group,** Milpitas, California
CMOS Mixed Signal IC Design: Done for a standard product cell library.
Designs included:

- PLL, 1GHz, data timing recovery
- PLL, 300 MHz freq. synthesizer
- PLL, 27 MHz, DVD timing recovery
- DAC, 10 bit, 200MHz, I-steering
- ADC, 10 bit, 3MHz, successive approx.
- ADC, 6 bit, 300MHz, flash
- ADC, 10 bit, 50 MHz, sub-ranging

Also: op-amps, comparators, band-gap references, variable gain amplifiers, offset alignment, process calibration circuits, network analysis for RF packaging above 1GHz, foundry development for new CMOS technology.

November 1995 - January 1996: **SVI Corporation**, Los Gatos, California
Design for an instrumentation system used to characterize 250MHz PRML channels.
June 1994 - November 1995: **Quantum Corporation**, Milpitas, California
Power Drive IC's use for disk drives. Bipolar and DMOS processes.
October 1990 - March 1994: **EXAR Corporation**, San Jose, California
BiCMOS and Bipolar IC's: Disk drive read channels; including pre-amplifiers, LNA's, programmable gmC filters, frequency synthesizers, and timing recovery PLL's. Products widely used in Seagate's disk drives.
May 1990 - August 1990: **IMP Corporation**, San Jose, California
Development of Read Channel IC: Architecture of a BiCMOS read channel IC for laptop computers.
August 1988 - May 1990: **Maxtor Corporation**, San Jose, California
Advanced Technology Research: R+D of new storage system read-back data detection.
November 1984 - July 1988: **Digital Equipment Corporation**, Shrewsbury, Massachusetts
Servo-writer System and Read Channel IC design
July 1983 - November 1984: **Data General Corporation**, Westboro, Massachusetts
Mixed signal IC design and creation of bipolar SPICE model transistors.
January 1980 - June 1981: **LTX Corporation**, Westwood, Massachusetts
Start-up in automated test equipment.

Academic & Professional:

- Chairman 2005 - 2008 IEEE San Diego – Solid State Circuits, Microwave Theory and Techniques
- IEEE Microwave Theory and Techniques, Reviewer for submitted publications, 2005 thru 2008
- IEEE Journal of Solid State Circuits, Reviewer for submitted publications, 2003 thru 2008
- Instructor, UCSD Extension "CMOS Analog and Mixed Signal IC Design" 1999 thru 2002
- Senior Member of IEEE, San Diego IEEE Executive Committee Member

Publications:

- "Efficient Simulation and Validation for Mixed-Signal SOCs" EDN Magazine, March 29, 2007
- "Determine Foundry-Model Problems Without Touching a Wafer" Chip Design Magazine April-May 2006
- "Simulation Vs. Silicon – Avoid Costly Mistakes With Accurate Models" Electronic Design Magazine, October 28, 2004
- "Signal Integrity Effects in Custom IC and ASIC Designs"
  IEEE Press, Wiley Interscience, contributing author, published 2002, ISBN 0-471-15042-8
- "Designing Analog and Mixed Signal Circuits on Digital CMOS Processes"
  EDN Magazine, August 3, 2000
- "Noise Reduction Is Crucial to Mixed-Signal ASIC Design Success (Part 1)"
  Electronic Design Magazine, October 30, 2000
- "Noise Reduction Is Crucial to Mixed-Signal ASIC Design Success (Part 2)"
  Electronic Design Magazine, December 4, 2000
- "BiCMOS 5HPE A New Silicon Germanium Technology for High Frequency RF Applications" IBM Micro News, Volume 7, Number 4, 2001

Management & Technical Lead: Digital, Exar, IMP, LSI Logic, Fairchild, IBM, Effective Electrons

Design Tools: Cadence, Analog Artist, Spectre, Spectre-RF, Virtuosso-XL, Dracula, Mentor Graphics, Design Architect, Accusim, Calibre, Viewlogic, Verilog-AMS, Verilog-A, HSPICE, SPICE, Matlab, ASITIC, Sonnet, PCAD

Education: MSEE-1983, BSEE-1979 - Worcester Polytechnic Institute