Jerry Twomey

Phone: 760-522-5090
Email: jerry@effectiveelectrons.com
3144 Cabrillo Bay Lane, San Diego, CA 92110, USA
US Citizen

Position Desired: Electronic product design. I am an Analog, Mixed Signal and RF designer experienced in IC/PCB/Systems product development. I have done communications, medical systems, micro-power applications, high speed data, power management, control systems, video, electro-mechanical servo/motion, and others. Have been a "hands on" designer, a technical lead, and managed product development teams.

Experience:

November 2003 – Present **Effective Electrons,** San Diego California – Contract circuit design and OEM support services. Client activity includes:

- August 2009 – Present – Medical system for therapeutic hypothermia induction, including all IEC-60601 compliance issues, analog sensors, pressure monitor/control, feedback control circuits, power/battery system, digital controller interfaces, and Verilog design for controller. (Benechill, San Diego CA)
- March 2009 – February 2010 - Blood Glucose Monitoring Systems, both hospital and personal monitor devices. Hospital system including power isolation, patient safety isolation circuitry, RFI, EFT, RF common mode, Magnetic fields, ESD, sensor and control system circuitry. Personal glucose monitor included antennas, polar plot analysis and RF network design. (Dexcom, San Diego CA)
- November 2008- January 2009 – Receiver architecture specification for optical fiber data transport at 100GB/s (LumiQ, Boston MA & San Diego CA)
- June-August 2008 –Designs of PCIE SerDes & Low Power Crystal Oscillator, 45nm CMOS (Qualcomm, San Diego, CA)
- April-May 2008 –Configuration of Cadence Mixed Signal EDA (Tektronix, Beaverton Oregon)
- October 2006 – December 2007 – 90nm SOI Radiation Hardened PLL Frequency Synthesizers, ESD, I/O Cells, LVDS Receiver/Transmitter, Verilog-AMS PLL models, PCB test benches for PLL and LVDS test chips. (ATK Mission Research, Albuquerque NM)
- August 2006 – March 2007 – Medical, muscle motion stimulus system, PCB circuits, motor power drivers, controls system, safety redundancy circuits, IEC-60601 compliance, and embedded controller code. (Breg-Orthofix, Vista CA)
- July 2006 – EDN Magazine – Technical writer covering 43rd Design Automation Conference
- June – July 2006 – Technical training seminars (Kriptic Devices, Kuala Lumpur Malaysia)
- March 2005 – May 2006 - 65nm CMOS IC for 20 GB/sec data over MPP super-computer backplane SerDes transmitter/receiver. (Cray Inc. – Chippewa Falls Wisconsin, Seattle Washington)
- January – March 2005 – Control system for optical data systems. (Ceyx Technologies, San Diego)
- September – December 2004 – EM simulation for RF signal paths at 6-18GHz. (IBM, San Jose CA)
- April – September 2004 – RF front end - gmC filters for UWB receiver. (Alereon, Austin Texas)
- January 2004 – February 2005 – Custom IC for satellite communication. (Shin Satellite – Thailand & Codespace – Hood Oregon)

October 2002 – October 2003: **Axiom Microdevices**, Orange/Anaheim, California
CMOS RF Power Amplifiers for GSM cell phones. Series A start-up included IC design, layout, technical infrastructure, and staffing activities. This included:

- RF Front end driver circuits for PA
- PA linearity, phase noise analysis
- ESD I/O design
- PA Power management and control system
- Design team staffing, IT and EDA support
- Foundry/Process Qualification

September 2000 – August 2002: **IBM - RF Design Center,** Encinitas, California
Wireless IC Design: Development of direct conversion receivers for 3G cellular phones, WCDMA, GSM, UMTS, CDMA 2000 cellular standards. This included:

- Spur reduced PLL charge pump
- GSM gain, noise & linearity analysis
- Enhanced linearity LNA biasing
- Active RC filters and gmC filters
- WCDMA analog base-band
- Delta-Sigma ADC for CDMA 2000
- Auto-compensated process circuits
- New foundry processes: RF-CMOS & SiGe

July 1998 – September 2000: **Fairchild Semiconductor,** San Diego, California
Mixed signal IC design: designer and technical mentor for the department. Designs included:

- ADC's,14, 8 bit, VCO/counter & pipeline
- DAC, 10 bit, 300 MHz, I-steering
- Thermal cooling monitor/control IC
- LDO micro-power, 35 uA, for cellular
- PLL, 300MHz, for clock recovery
- Product demonstration/test PCB design
- Li-ion battery protection & charger IC
- Power systems, batteries & chargers

February 1996 - June 1998: **LSI Logic - Mixed Signal Design Group,** Milpitas, California
CMOS Mixed Signal IC Design: Done for a standard product cell library.
Designs included:

- PLL, 300MHz & 1GHz CDR & Freq. Synth.
- DVD timing recovery & controller
- DAC, 10 bit, current steering
- ADC's, 6 bit flash & 10 bit, sub-ranging
- CMOS foundry/process development
- Band-gap & Process calibration circuits

June 1994 - November 1995: **Quantum Corporation**, Milpitas, California

- Power Drive IC's and PCB design used for hard disk drives spindle and servo motors
- Component & PCB optimization for cost and high volume automated assembly.

October 1990 - March 1994: **EXAR Corporation**, San Jose, California

- HDD read channels, pre-amplifiers & LNA's
- Programmable gmC filters
- Clock and Data Recovery
- Frequency synthesizer PLL's

Academic & Professional:

- Lecturer, winter quarter, 2010, UCSD ECE graduate studies, ECE-264C, ADC and DAC IC Design
- Rethinking Analog Design - Simulation vs. Silicon, May 2010, invited speaker, Stanford University
- Chairman 2005 - 2010 IEEE San Diego – Solid State Circuits, Microwave Theory and Techniques
- IEEE Microwave Theory and Techniques, Reviewer for submitted publications, 2005 thru 2010
- IEEE Journal of Solid State Circuits, Reviewer for submitted publications, 2003 thru 2010
- Instructor, UCSD Extension "CMOS Analog and Mixed Signal IC Design" 1999 thru 2002
- Senior Member of IEEE, San Diego IEEE Executive Committee, Silicon Valley Consultants Group

Publications:

- "Efficient Simulation and Validation for Mixed-Signal SOCs" EDN Magazine, 3/29/2007
- "Determine Foundry-Model Problems Without Touching a Wafer" Chip Design Magazine April-May 2006
- "Simulation Vs. Silicon – Avoid Costly Mistakes With Accurate Models" Electronic Design, 10/28/2004
- "Signal Integrity Effects in Custom IC and ASIC Designs, multi-author, 2002, ISBN 0-471-15042-8
- "Designing Analog and Mixed Signal Circuits on Digital CMOS Processes" EDN, 8/3/2000
- "Noise Reduction Is Crucial to Mixed-Signal ASIC Design Success (Part 1)" Electronic Design, 10/30/2000
- "Noise Reduction Is Crucial to Mixed-Signal ASIC Design Success (Part 2)" Electronic Design, 12/4/2000
- "BiCMOS 5HPE A New Silicon Germanium Technology for High Frequency RF Applications" IBM Micro News, Volume 7, Number 4, 2001

Patents:

- USPTO – 6,657,494: Variable Gain Mixer Amplifier With Fixed DC Operating Voltage Level
- USPTO – 7,256,573: Distributed Active Transformer Power Control Techniques
- USPTO – 7,043,206: Fully Integrated Offset Compensation Feedback Circuit
- USPTO – 7,027,791: Analog Baseband Signal Processing and Method

Design Tools:

Semiconductor – Cadence, Analog Artist, Spectre, Spectre-RF, Virtuosso-XL, OCEAN Scripts, SPICE, HSPICE Mentor Graphics, Design Architect, Accusim, Calibre, Viewlogic, Verilog-AMS, Verilog-A
PCB – Orcad, PSPICE, PCAD-2004, Mentor-PADS **Electromagnetic -** ASITIC, Sonnet
System & Lab Analysis – Matlab, Simulink, Agilent ADS, LabView, Mathmatica, MathCAD
Digital – Verilog, Xilinx ISE design suite for FPGA and CPLD devices.
Other: Microsoft Office (Word, Excel, Project, PowerPoint, Visio) Latex, Framemaker, Unix, Linux

Education: MSEE & BSEE - Worcester Polytechnic Institute, Worcester MA