the connectivity description of the cells and the custom library to produce the superblock layout. Wiring parasitics were extracted and circuit speed was analyzed using ADVICE and MOTIS on the superblock level. Verification tools were then used to validate the layout. Finally, symbolic representation of the entire superblock was generated and stored into a large ASCII file. Changes due to speed problems or logic updates could then be conveniently accommodated by editing this file.

As described above, GMCC is a hierarchical standard-cell approach. It provides flexibility in cell layouts, priority clock signal routings, and ease in circuit updates. These properties, which are very useful in performance enhancement, are lacking in the rigid standard-cell systems. GMCC has produced high-speed superblocks with a layout effort five times less than that obtained for hand-packing techniques. However, a 10–20-percent penalty may incur in terms of silicon area.

IV. Chip Assembly and Silicon Results

The frame modules and power/ground bus routings were continuously updated throughout the chip implementation process. A number of attempts at positioning these modules and superblocks were made. This allowed optimum intermodular wiring parasitics to satisfy the speed requirement. Inter-superblock signals and I/O signals (through the frame modules) were connected automatically by LTX2. The entire chip was evaluated using the multiple-delay mode in MOTIS ensuring that the required speed was attained. Design-rule violations and layout errors were also checked by LARC and GOALIE [14] in the chip level.

The DRC chip was successfully implemented. Devices obtained from the first processed wafers were proven to be error free after extensive testing. Fully functional chips were packaged and tested again in the WE®32100 microsystem environment. With the nominal processing parameters, the DRC chips operate with an internal clock rate of 36 MHz. Maximum clock skew measured from a large number of silicon samples was below 1 ns, as compared to the value of 3 ns provided by the worst-case simulation analysis.

V. Conclusion

A high-performance DRAM controller was implemented with a new layout methodology. Short turnaround time in the layout cycle enhanced the efficiency in attaining global optimization in architectural, logical, and physical design. High-speed VLSI circuits were realized through careful clock handling techniques and the GMCC approach. At the same time, low-cost IC design was achieved due to a greatly reduced staff requirements.

Acknowledgment

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Linearization of Voltage-Controlled Oscillators Using Switched-Capacitor Feedback

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***Abstract*—The voltage–frequency characteristics of any voltage-controlled oscillator (VCO) can be linearized using a simple circuit containing a switched capacitor. The oscillation frequency becomes insensitive to power supply or temperature variations, and is determined only by the values of a capacitor, resistor, and the control voltage with respect to a reference voltage.**

I. Introduction

There are many reasons for requiring the voltage-to-frequency characteristic of a voltage-controlled oscillator (VCO) to be linear, the most important one being that the VCO may be used to demodulate FM signals with low distortion in a phase-locked loop configuration. Instrumentation applications often require an analog voltage to be transmitted as a proportional frequency. The usual approach to linearization is to design an intrinsically linear voltage-to-current converter, that is then used to charge and discharge a timing capacitor between reference levels [1]. This may be characterized as an *open-loop* approach, where deviations from linearity at high frequencies of oscillation, or from power supply variations, go uncompensated. This letter describes a *closed-loop* technique, where a switched capacitor is used as a frequency-to-current converter in a linearizing feedback loop [2].

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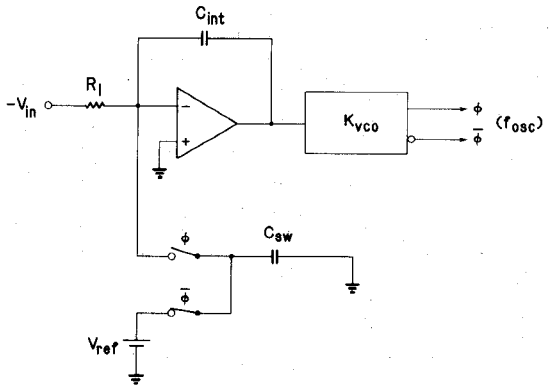

Fig. 1. Linearizing feedback loop for a VCO.

II. The Circuit

The VCO with the linearizing feedback loop (Fig. 1) is driven by a control voltage produced by the integration of the difference between an input current and another current proportional to frequency. The latter is derived by switching the capacitor C_{sw} between a reference voltage V_{ref} and ground at the oscillation frequency f_{osc} of the VCO. Thus, the average current through C_{sw} is

$$i_{av} = C_{sw} V_{\text{ref}} f_{osc} \tag{1}$$

and is of opposite polarity to the reference current V_{in}/R_1. This polarity is determined by the sequence in which the switches are operated. By connecting an inverting amplifier to the output of the integrator, a negative feedback loop results, which samples the output frequency in the form of a current and compares it with the input current. The loop reaches a steady-state equilibrium when the average current flowing into the integrator capacitor C_{int} is zero, that is, when

$$f_{osc} = \frac{V_{\text{in}}}{C_{sw} R_1 V_{\text{ref}}} \tag{2}$$

which is a linear dependence of frequency on input voltage, independent of the nonlinearities inherent in the VCO, and of fluctuations in temperature, power supply, and amplitude of the oscillation.

The loop is self-starting because of the negative feedback and the presence of the continuous current through R_1. This is an important consideration for a switched-capacitor circuit, which relies on an oscillation to already exist to initiate the capacitor switching action.

The range of f_{osc} that may be obtained by this technique is dependent on the oscillation range of the VCO. The timing elements of the VCO must be chosen such that this oscillation frequency range corresponds with the requirements imposed by (2) over the complete range of V_{in}.

The discrete pulses of current through C_{sw} will produce spikes about the average voltage at the integrator output. These spikes can be filtered out at the following inverting amplifier. However, their only effect on the VCO action is to modify the duty cycle of the oscillation, while keeping the period of oscillation locked to the value specified by (2). For many applications, such filtering is thus unnecessary.

This technique is appropriate for implementation on monolithic IC VCO's where the timing capacitor is on-chip. This is often the case where the VCO may be part of a large system on a chip, and where relatively high frequencies of oscillation are desired. An example is an FM demodulator on a single-chip radio.

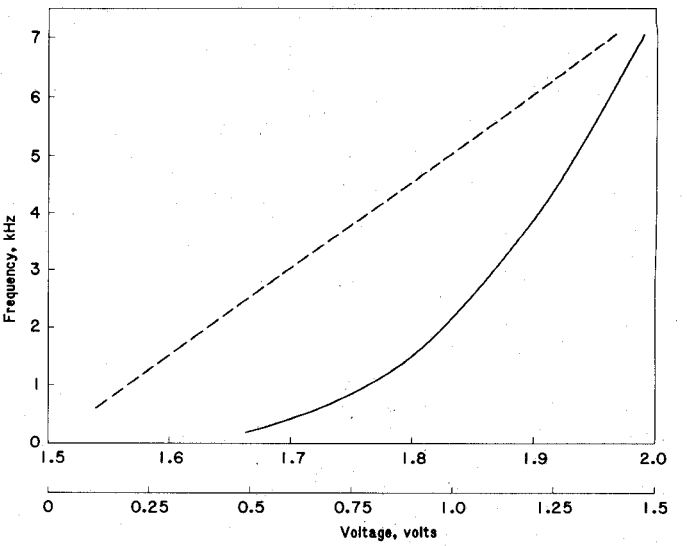

Fig. 2. Measured voltage–frequency characteristics before (solid line, lower scale) and after (dashed line, upper scale) the application of feedback.

III. Dynamics of Linearization Loop

An important consideration in making this scheme practical is the speed of response and the stability of the linearization loop. The equation governing the dynamics of the loop is

$$\left(\frac{V_{\text{in}}}{R} - f_{osc} C_{sw} V_{\text{ref}}\right) \times \frac{1}{sC_{int}} = \frac{f_{osc}}{K_{\text{VCO}}}$$

where K_{VCO} is the voltage-to-frequency transfer of the unlinearized VCO alone. The loop transfer function then is

$$\frac{f_{osc}}{V_{\text{in}}} = \frac{1}{R\left(C_{sw} V_{\text{ref}} + \dfrac{sC_{int}}{K_{\text{VCO}}}\right)}. \tag{3}$$

Thus the loop has a single time constant τ of magnitude

$$\tau = \frac{C_{int}}{C_{sw} V_{\text{ref}} K_{VCO}}. \tag{4}$$

If the linearized VCO is required to follow rapid changes in V_{in}, the magnitude of τ must be made small by choosing a small ratio of C_{int} to C_{sw}, as the other two quantities that determine τ are usually fixed. For this small capacitance ratio, the integrator is unable to "smooth" the charge pulses injected by the switched capacitor effectively, and the duty cycle of the oscillation may be affected. The oscillation frequency, however, displays the desired linear dependence on V_{in}.

IV. Experimental Results

To verify this concept, measurements were made on a readily available VCO with poor intrinsic linearity, the RCA 4046 CMOS phase-lock loop. A CMOS 4066 quad bilateral switch and an LM 324 dual operational amplifier constituted the feedback loop. The measured frequency–voltage characteristics correspond very well to the expected values (Fig. 2) from dc to 7.5 kHz. This frequency range was chosen to remain well below the unity gain frequency of the op amp. A marked improvement in linearity and removal of the offset in the inherent frequency–voltage characteristics of

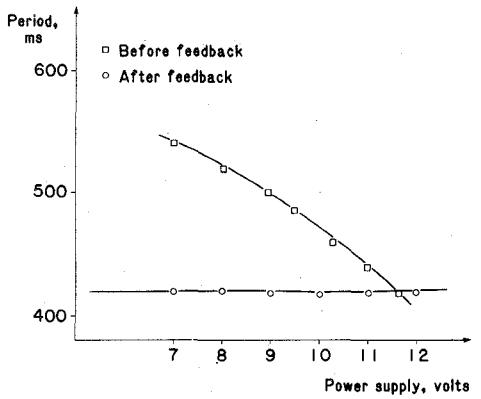

Fig. 3. Measure power supply dependence of frequency before and after application of feedback.

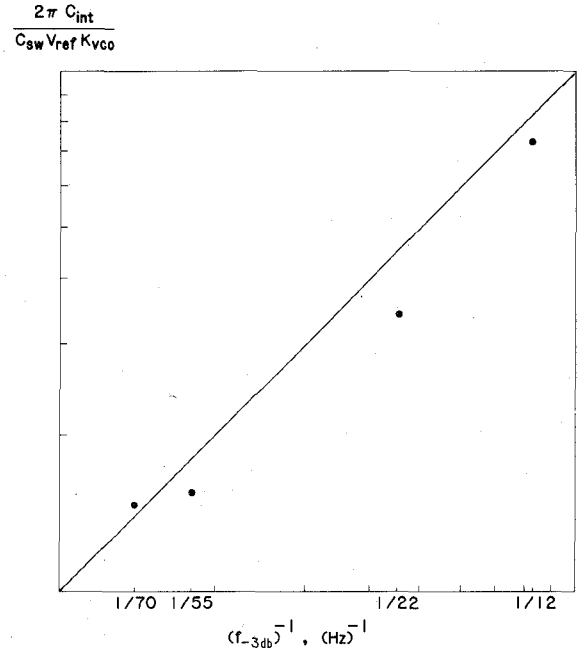

Fig. 4. Measured loop time constants compared with calculated line.

the VCO are observed. The power supply dependence of the oscillation frequency is also reduced to an immeasurably small level (Fig. 3). Clearly, if R_1 and C_{sw} have a low-temperature coefficient, then the loop will compensate for the temperature dependence of the 4046 as well.

The loop dynamics were measured by applying a sinusoidal input f_{in} of increasing frequency, and observing the VCO control voltage produced in the linearization loop. A 20-dB/decade rolloff in the loop sinusoid is obtained for $f_{in} > 1/(2\pi\tau)$. The measured values of the corner frequency correspond very well with the predictions from (4) (Fig. 4).

Although the test circuit oscillated at low frequencies, the technique may be used for any f_{osc}, limited only by the charging time of C_{sw} through the switch resistance, and parasitic feedthrough charges through the switch capacitances at very small values of C_{sw}. Naturally, at high frequencies the switch sizes will scale down with C_{sw}, keeping the proportional feedthrough relatively constant.

V. Conclusions

A simple linearizing feedback loop for VCO's using a switched capacitor and two op amps has been described. It provides a closed-loop means of making the oscillation frequency of VCO circuits proportional to the control voltage, when it might not otherwise be so. The power supply dependence of the oscillation frequency is reduced to almost zero. The variation of oscillation frequency with temperature is determined by the temperature coefficients of a resistor, capacitor, and reference voltage, which are normally much smaller than that of the VCO itself.

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Errata to "Analysis and Design Optimization of Domino CMOS Logic with Application to Standard Cells"

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The following corrections should be made to the above paper.[1] Equation (9) should read

$$I_r = \frac{\beta_n}{2}\left[V_{DD} - V_2(t) - aV_{Tn}^*\right]^2$$

$$= C_2\frac{dV_2}{dt} + \frac{V_2(t)}{R} = -C_1\frac{dV_1}{dt}.$$

Equation (15) is valid only if $V_2(0) < V_{2st}$. If $V_2(0) > V_{2st}$, the denominator of (15) should read

$$\frac{V_h}{RC_1} + \frac{C_2}{C_1}V_f \cdot D.$$

In (A7) and (A12), the n above the summation sign should be replaced by k.

After (A10), the paragraph should read "If M_i to M_k are not all of equal size $\cdots$."

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