MOM capacitor simulation challenges and solutions

Maxim Ershov

Silicon Frontline Technology, 595 Millich Dr., Campbell, CA 95008, USA
Phone: 1-408-963-6916, Fax: 1-408-963-6906, E-mail: maxim@siliconfrontline.com

Abstract

This application note describes characteristics and design challenges of metal-oxide-metal (MOM) interdigitated capacitors and circuits containing MOMs. It also explains how the MOM capacitor design can be facilitated using F3D – a parasitic extraction tool based on a random walk method.

I. MOM capacitor characteristics and design challenges

1. What is a MOM capacitor?

Analog integrated circuits (ICs) use various types of integrated capacitors utilizing MOS, p-n junction, MIM (metal-insulator-metal), poly-to-poly, MOM (metal-oxide-metal), and other structures. MOM capacitor, also known as VPP (vertical parallel plate), NVCAP (natural vertical capacitor), lateral flux capacitor, comb capacitors, interdigitated finger capacitor, etc. – is one of the most widely used, due to its good characteristics:

- high capacitance density (up to ~2 fF/μm^2)
- low parasitic capacitance
- symmetric plate design
- superior RF characteristics
- good matching characteristics
- no additional masks or process steps, and thus low cost

MOM capacitors exploit the effect of lateral (intralayer) capacitive coupling between the plates formed by standard metallization wiring lines and, optionally, vias (see Figure 1). Lateral capacitive coupling provides better matching characteristics than vertical coupling due to a better process control of lateral dimensions than that of metal and dielectric layer thicknesses. To increase the capacitance density (capacitance per unit area of silicon chip), several metal layers are connected in parallel by vias, forming a vertical metal wall or mesh. Normally, lowest metal layers (e.g, M1 – M5) with minimum metal line width and spacing are used for MOMs to maximize the capacitance density.

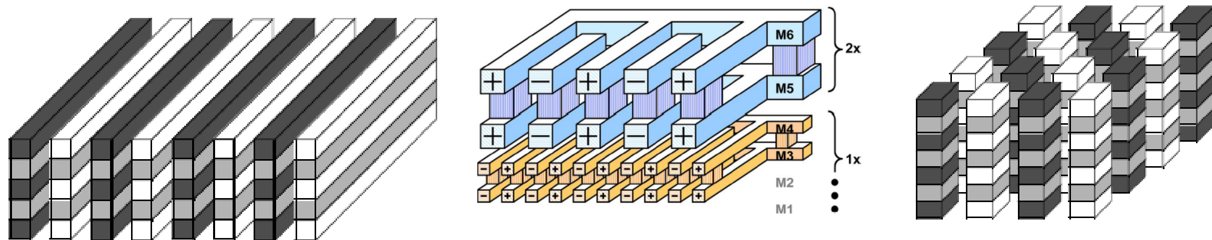

Fig.1. Vertical parallel-plate and vertical bar MOM capacitor structures.

2. Problems with existing capacitance extraction tools

Existing capacitance extraction tools are based on a pattern-matching algorithm that is incapable of providing the accuracy required for analog and mixed-signal circuits. Errors in calculated capacitance can reach up to 30-40%, or even higher. Parasitic extraction tools do not extract frequency-dependent models that can be used for MOM capacitor frequency characterization and calculation of quality factor and resonant frequency.

Capacitance and frequency-dependent characteristics of MOMs can be calculated using electromagnetic field solvers (such as HFSS). However, the problem is in size and complexity of the geometry ─ MOM capacitors have a very large area and a huge number of small features (vias, lines, etc.). The requirement of having a detailed three-dimensional mesh to achieve accurate results limits the size of the design that can be simulated, and simulation time can exceed several tens of hours. A very long simulation time precludes electromagnetic field solvers from being used as a design tool and restricts their application to verification purposes only.

3. MOM Capacitance value

Designing the layout for a MOM capacitor that has a required capacitance value is a challenge. Foundries and fabs offering MOM capacitor options in their process technologies do not provide design kits or tools allowing accurate capacitance calculation. As a result, the values of MOM capacitors have to be determined experimentally after fabrication. This complicates and delays the design of chips utilizing MOM capacitors.

4. Parasitic capacitance to ground and to neighboring nets

Parasitic coupling between MOM capacitor plates and neighboring nets and/or the ground can not be extracted accurately enough using existing extraction tools, which introduces an additional uncertainty that can lead to chip failures. Even if MOM capacitors are characterized through measurements and described by compact (SPICE) models, selective blocking (exclusion) of intrinsic MOM capacitance from parasitic extraction and calculating only parasitic coupling to ground and neighboring nets are beyond the capabilities of existing parasitic extraction tools. Parasitic capacitances of MOMs are especially important when exact matching or weighting of capacitors is required ─ in SAR ADCs (successive approximation register analog-to-digital converters), sample-and-hold circuits, switched capacitor circuits, and other precision analog designs.

5. Series resistance and inductance (quality factor, resonant frequency)

Finite resistance of the metal wires introduces a parasitic series resistance in MOM capacitor, which leads to power loss and reduces the quality factor $Q=1/(\omega RC)$. Parasitic series inductance of the wires of MOM capacitor leads to frequency dispersion of capacitance and resonance effect. At frequencies higher than the resonant frequency $\omega = 1/\sqrt{LC}$, the capacitor behaves as an inductor (inductive impedance dominates over capacitive impedance). Thus, for high-frequency applications, MOM capacitors should be designed in such a way that their resonant frequency is higher than the operating frequency, and the quality factor meets the design target. Design tools for MOM capacitors should provide accurate and efficient calculation of quality factor and resonant frequency.

6. Capacitor matching and statistical modeling

Variation of MOM capacitor parameter occurs due to process variability: metal and dielectric layer thickness, metal widths, and other variations of process parameters over the wafer, wafer-

to-wafer, and lot-to-lot. Design kits should provide models describing statistical properties of MOM capacitors to optimize matching characteristics, for centering process targets, and to improve yield.

7. Capacitor linearity, reliability, and dielectric leakage

Capacitor linearity (its independence on applied voltage and measurement frequency), dielectric reliability (time-dependent dielectric breakdown), and leakage are determined mainly by technological, process, and material properties. These parameters can not be predicted or improved using software tools, and thus they are beyond the scope of this application note.

8. Requirements for extraction tools for MOM capacitor design

A software tool that would be useful for design of MOM capacitor devices and circuit should be able to calculate all the necessary electrical characteristics, including parasitics, with sufficiently high accuracy (1% or better), and do so within a short period of time. So far, there has been no extraction tool available on the market satisfying all of these criteria.

II. F3D — software tool facilitating MOM capacitor simulation

F3D is a capacitance and distributed RC extractor based on a random walk method developed by Silicon Frontline Technology. This software tool is intended for accurate capacitance and RC extraction of small and medium size analog and mixed-mode circuits. F3D is also ideally suited for extraction and calculation of characteristics of MOM capacitors. A very fast extraction time and modest memory requirements of F3D are enabled by the intrinsic properties of the floating random walk technique. This method does not require a three-dimensional mesh or rigorous capacitance calculations, and its performance is optimal in the case of dense metal layouts, which is the case for MOMs. F3D can read layout information from GDSII files, or from industry standard extraction flow formats (CCI, DFII, Hercules). Technology information (metal and dielectric layer thicknesses, dielectric constants, resistivities, etc.) can be provided from various industry-standard formats (ITF, PROCFILE, ICT, iRCX). F3D takes into account all manufacturing effects described by these file formats (CMP, metal etch, metal trapezoidal shapes, planar and conformal dielectrics, etc.). F3D has been qualified by the major semiconductor foundries.

F3D calculates all significant coupling capacitance components with a user-specified accuracy, and generates a netlist (e.g., in a DSPF format) with distributed RC network accurately representing MOM capacitor. The following characteristics can be efficiently calculated using F3D:

- Plate-to-plate capacitance
- Parasitic capacitance from plates to ground and to neighboring nets
- Quality factor
- Resonant frequency
- Statistical properties

F3D can also generate a compact device model for MOM capacitors that can be used for efficient circuit simulation. These models have a limited number of elements and allow describing frequency-dependent characteristics of MOM capacitors.

III. Application examples

F3D has been successfully used to extract characteristics of MOM capacitors fabricated by different foundries and IDMs with technology nodes ranging from 180nm to 40nm. Excellent agreement with experimental data has been obtained for all cases without any data fitting. The extraction time did not exceed several minutes for the most complicated designs with extraction accuracy of 0.5% or better.

The figure below illustrates a good agreement between measured and F3D-extracted frequency-dependent characteristics of MOM capacitor fabricated with a 40nm CMOS process technology.

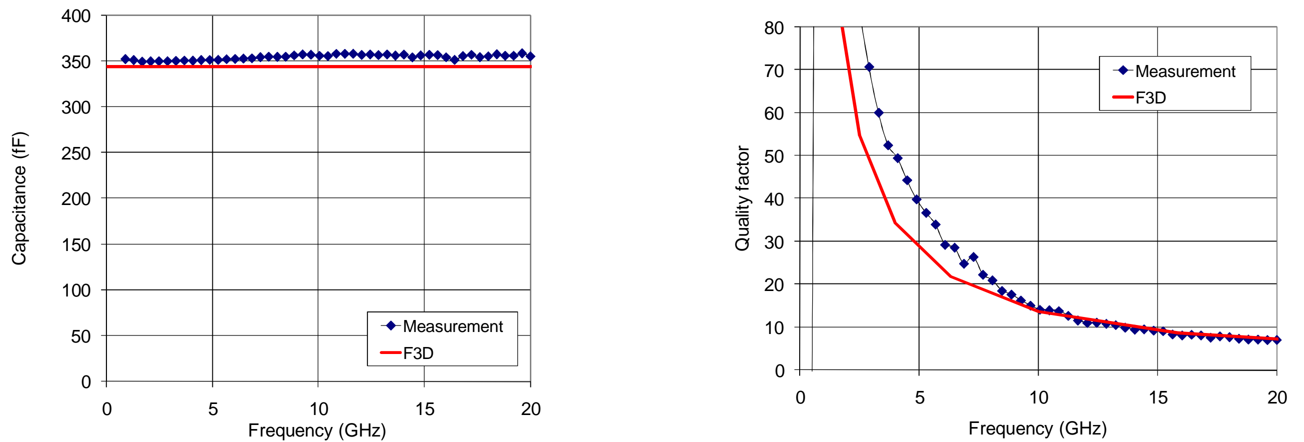

Fig. 2. Measured and simulation capacitance and quality factor of MOM capacitor (40nm technology).

Comparison of F3D-simulated capacitances for MOM capacitors with different sizes with experimental data are shown in Fig.3. These results were obtained without any fitting of the simulations, and the observed difference of ~3.5% can be attributed to manufacturing/process variations.

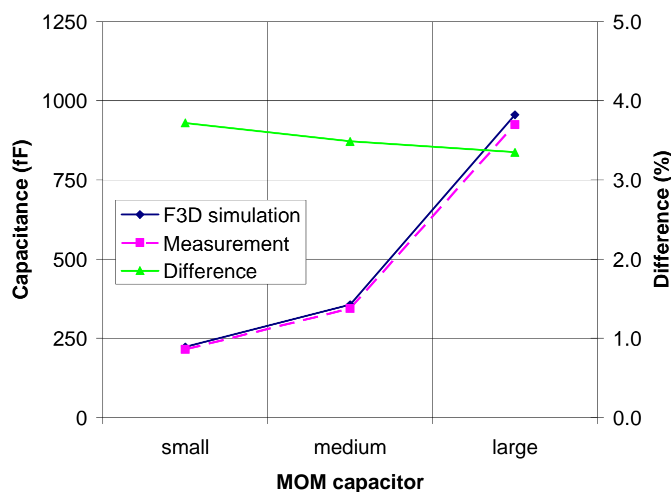

Fig. 3. Comparison of simulated and measured capacitance values (65nm technology).