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Technical Support Package

Stripline/Microstrip Transition in Multilayer Circuit Board

NASA Tech Briefs
NPO-41061



National Aeronautics and
Space Administration

Technical Support Package

for

STRIPLINE/MICROSTRIP TRANSITION IN MULTILAYER CIRCUIT BOARD

NPO-41061

NASA Tech Briefs

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NTR 41061 Title: A Cavity Backed Stripline to Microstrip Transition for High-Frequency, High-Speed Multilayer Circuit Boards with V-Shaped Extension

JPL Contributors – Section(s)

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Novelty: A stripline to microstrip transition has been developed that is suitable for multi-layered, high-frequency circuit boards. This transition is cavity backed, which eliminates coupling to neighbors. A novel V shape elongation to a rectangle cutout in the ground plane below the stripline (signal line) sits above a rectangular cavity and focuses the energy up the transition, minimizing reflection. The cavity eliminates coupling to neighbors and additionally reinforces the transmission up through the board to the top layer. The via connection is novel, in that it goes through the entire board, eliminating blind vias as the interconnecting vias. This allows the interconnecting via to be manufactured with a through-all approach that leads to more reliable connections. This via goes down to the bottom layer, but the radiation effects of this dead-end connection are compensated for by the V-shaped elongated cut-out in the ground plane, the cavity, and matching steps in the transition. The cavity is a simple-to-machine rectangular cavity, and does not need to be machined to meet the V-shaped elongated cut: this simplifies fabrication. This transition makes multilayer stripline to microstrip transitions possible with broadband operation.

How Work Relates to Current or Future NASA Activities: This work is in support of a Solid State Power Amplifier (SSPA) program developing next generation technologies for Spacecraft applications. The goal of this work is to develop microwave transmit power that competes with Traveling Wave Tube Amplifiers (TWTAs) using Solid State devices. This new technology is a step in providing an alternative to TWTAs that: do not use a high voltage power supply, are reliable, and use low-cost parts. This work has been funded by the JPL R&TD program.

Problem: In the process of designing a circuit board for a distributed solid state power amplifier, a way of getting buried stripline signals up to the top layer was needed. The requirements for the application were that the transition must traverse multiple layers, with intermediate layers containing dc circuitry, to the top layer where a patch antenna array was located. The transition must work at 32 GHz with low loss and low reflection. The transition must feed the top layer with an equal division power split on the microstrip line of the top layer. It was also required that the signal line via go all the way through the circuit board, and not be a 'blind' via.

Solution: A transition was developed that uses a via that translates through all layers of a high-frequency circuit board. The via connects to a circular pad on the bottom, or ground layer, which is a dead-end or no-connection point. This pad is surrounded by a cutout in the ground layer that has a V-shaped input. This V-shaped input focuses the fields to travel up the via, and works with a standard rectangular cavity below the transition. This makes the cavity easy to build by conventional machining techniques. The V-shaped focusing cut-out is also easy to fabricate based on printed circuit techniques. To compensate for reflections of the transition, step matching sections are used in the area of the V-shaped cutout.

Description: The developed transition is shown in the attached figures. Page 1 of the attached figures shows the transition, and that the power is equally split between ports 2 and ports 3 when the signal is input into Port 1. This insertion loss, S_{21} or S_{31} that is shown on page 1 and over a broader frequency band on page 2, is less than 0.2 dB of loss from 15 - 35.5 GHz. This shows that the transition is broadband in transmitting the signal up to the top layer. Pages 3 and 4 show that the input match is better than 19 dB over 15 - 35.5 GHz. This broad band input match is not expected from a circuit containing a cavity. But, the V-shaped elongated slot and input matching sections compensate for the narrowband nature of the cavity.

The connecting via (Via 1) traverses all the layers of the circuit board, which for this application where three ceramic substrate layers and two adhesive layers. Including the ground plane layer on bottom, this represents a 6 layer board as shown on page 5. A more detailed description of the layering can be found on page 5, which shows test boards being built. We note that this transition has already been demonstrated as part of a larger board, which includes the antenna array, as shown on pages 7, 8, and 9. The measurement represented on these pages supports the proper operation of the transition, but the test pieces will isolate the transition for a measurement of only the transition in a back-to-back

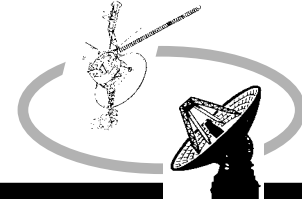
configuration. This test board is under fabrication and is intended as a measurement focused only on the transition for potential publication.

Mode strapping vias were used on this transition, as depicted by "Via2" on page 6. As shown, these vias are "blind" in that they connect up to an intermediate layer. These vias can be blind because they do not carry the signal and can be closely spaced as shown, this compensates for un-reliable connections caused by the blind via process.

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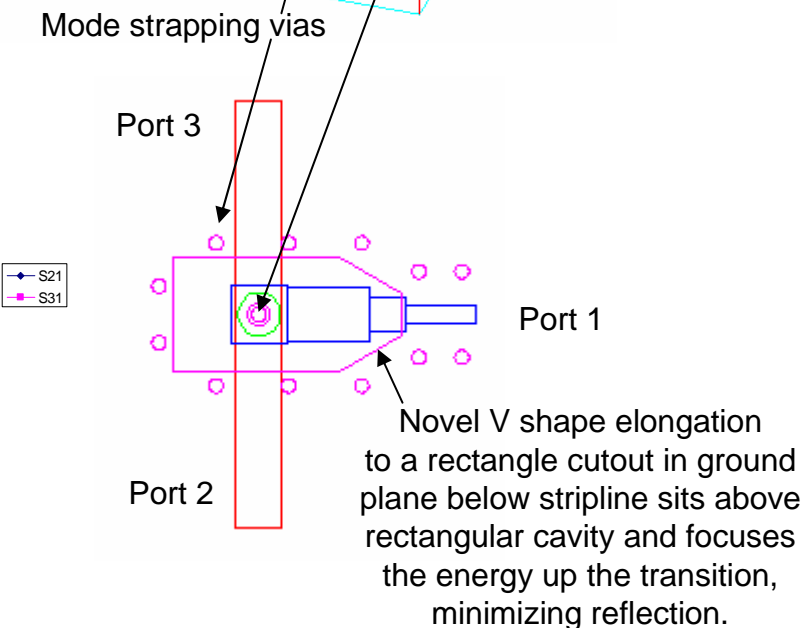
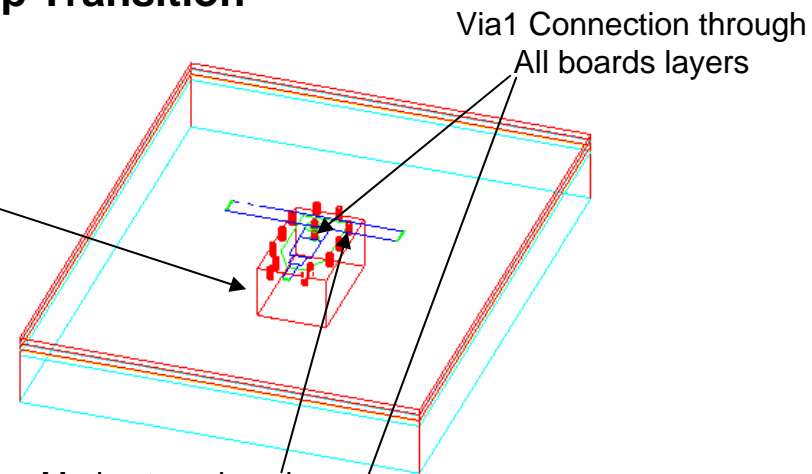
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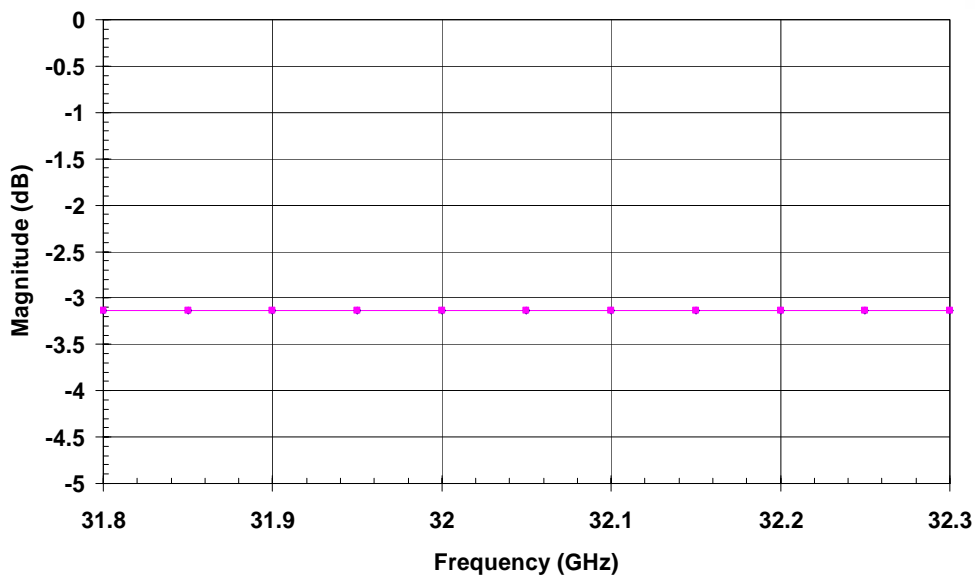


Stripline to Microstrip Transition

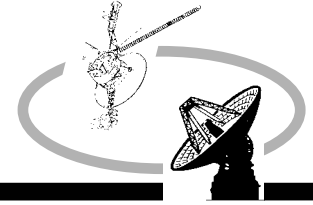
- **Stripline to Microstrip transition advantages**
 - Cavity backed, eliminates coupling to neighbors
 - Via connection through entire board, eliminates blind vias
 - Makes multilayer Stripline to microstrip transitions possible
 - High frequency operation: high speed



Magnitude of Scattering Matrix in dB, Power incident at Port 1

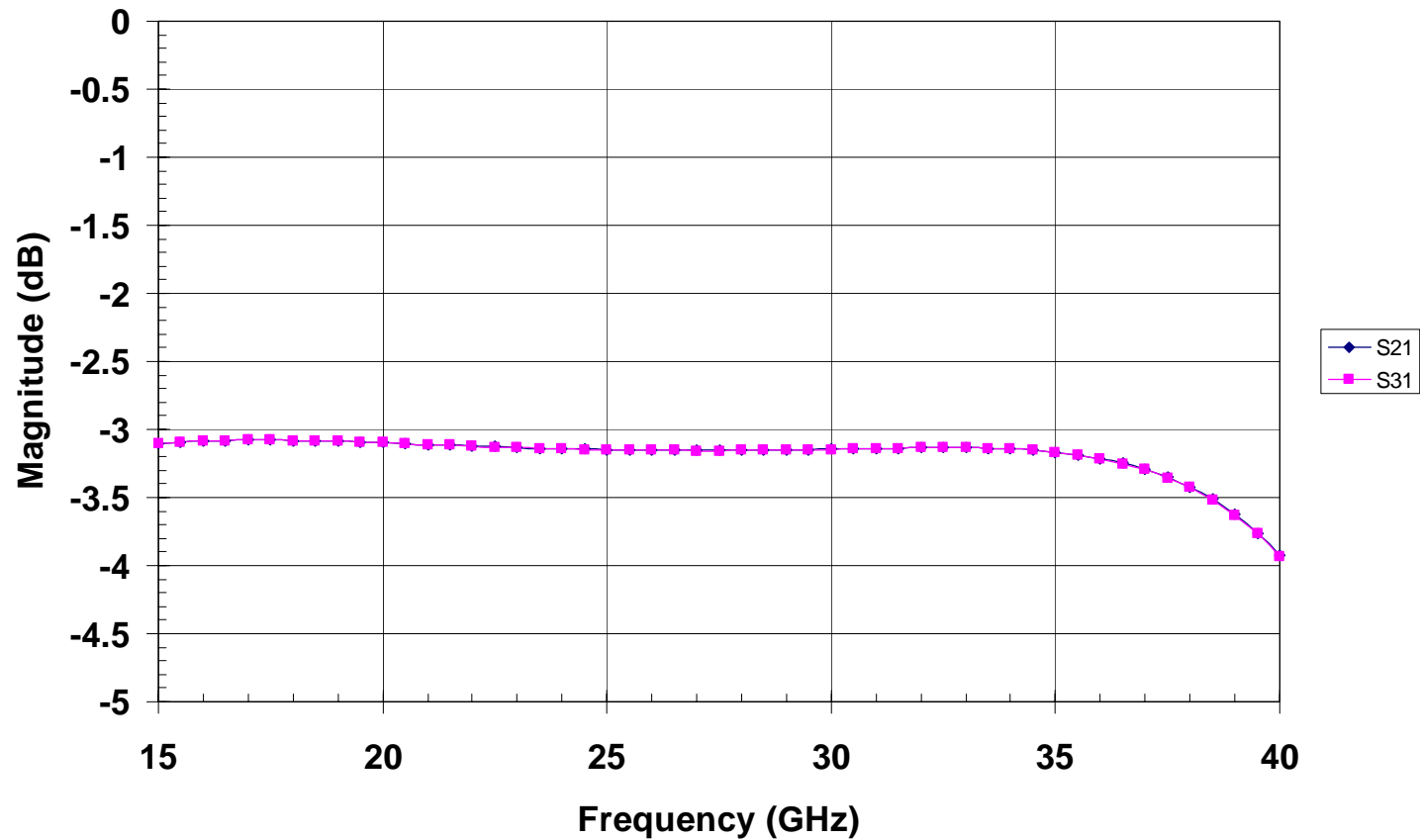


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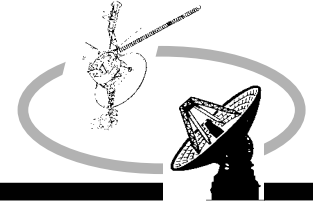


Microstrip to Stripline Transition: Wideband performance from 15-40 GHz

Magnitude of Scattering Matrix in dB, Power incident at Port 1

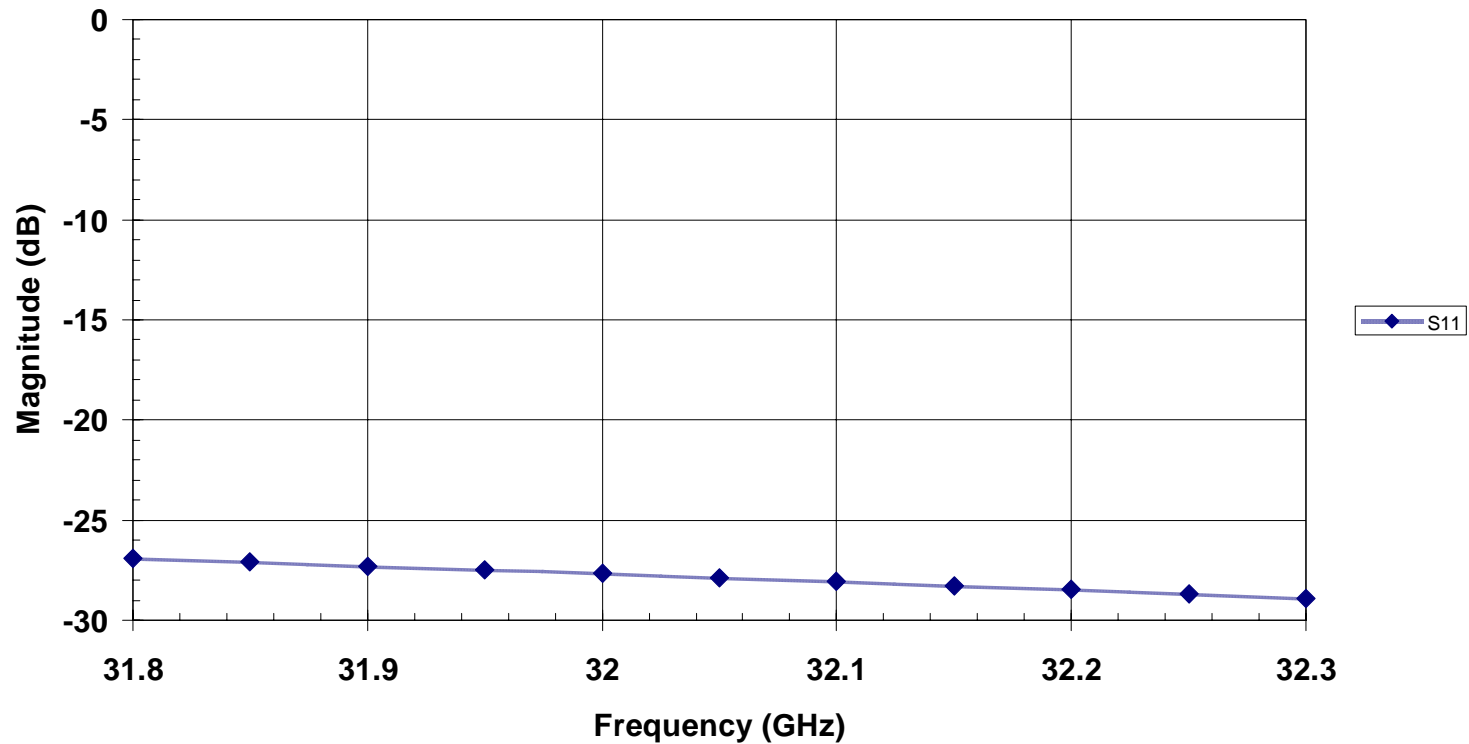


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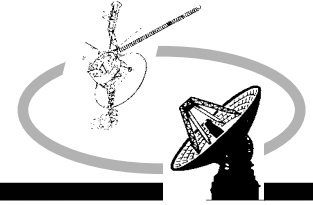


Microstrip to Stripline Transition

Magnitude of Scattering Matrix in dB, Input Match at Port 1

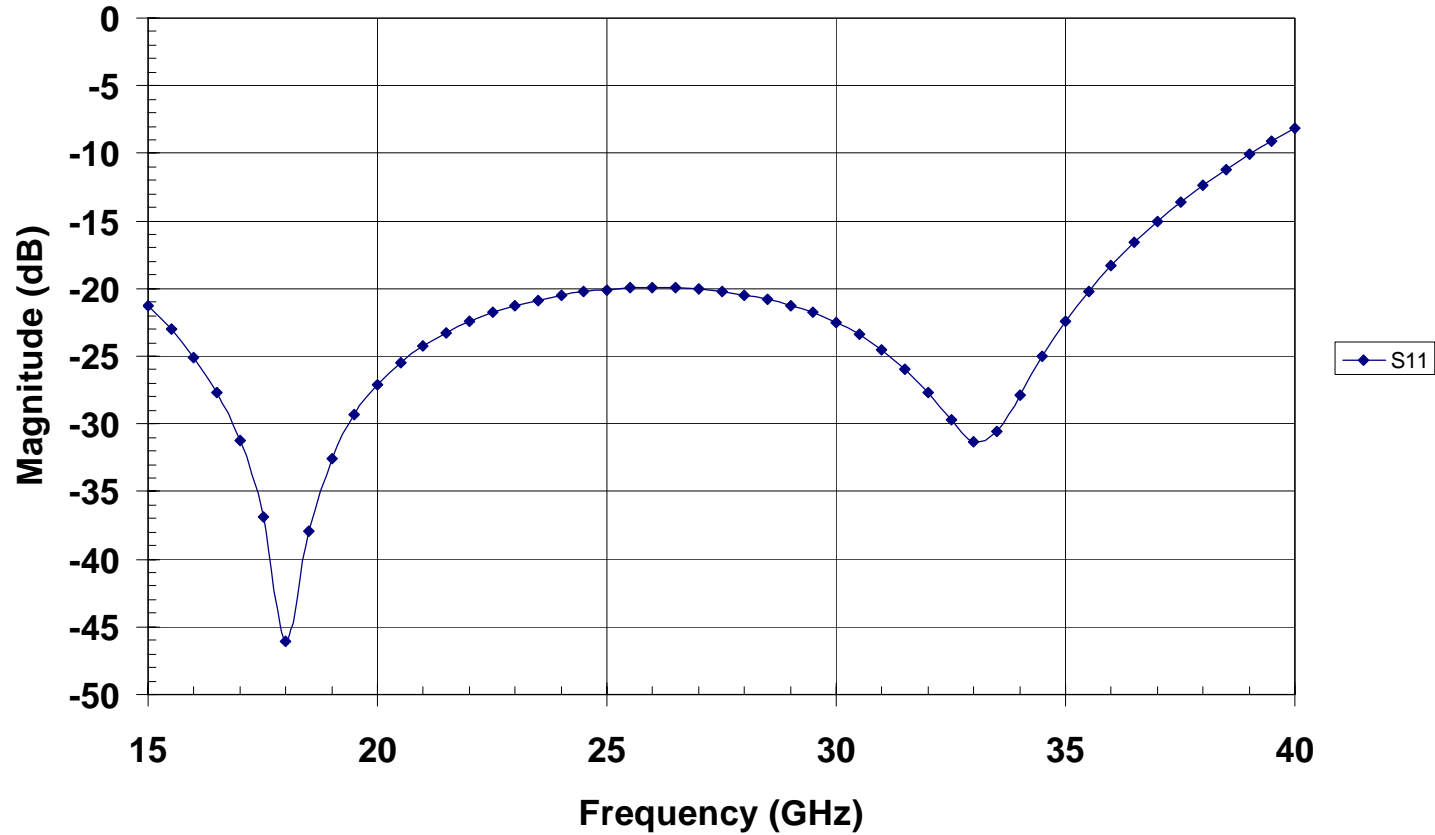


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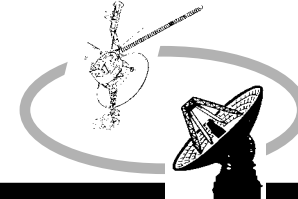


Microstrip to Stripline Transition: Wideband performance from 15-40 GHz

Magnitude of Scattering Matrix in dB, Input Match at Port 1



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Microstrip to Stripline Transition

Element Construction: the layers

Rogers R6002 (Ceramic):

0.254 mm (10 mils)

$\epsilon_r = 2.94$ nominal @ 10 GHz,

as supplied $\epsilon_r = 2.916 - 2.927$

loss tangent = 0.0012 @ 10 GHz,

as supplied loss tangent = 0.0013 – 0.0014

Gore SPEEDBOARD™ C Prepreg:

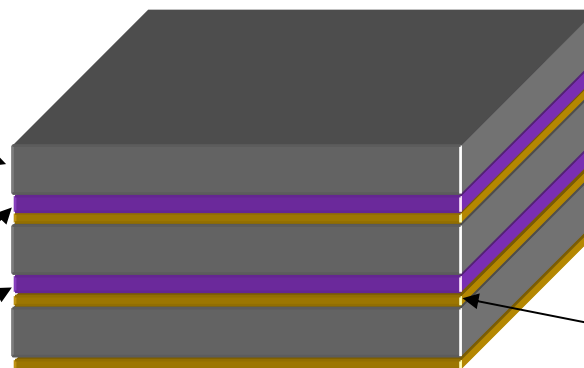
38 μm (1.5 mils) pressed thickness

$\epsilon_r = 2.67$

loss tangent = 0.0053

Std. Resin (~68%)

Other Prepregs such as Dupont FEP
are suitable.



RF ground plane:

17.5 μm (1/2 oz.) rolled copper

Stripline/Microstrip Feed:

17.5 μm copper (1/2 oz.)

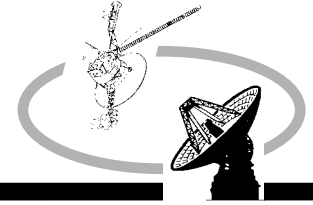
Ground (location of cutout with V shaped extension):

17.5 μm (1/2 oz.) rolled copper,

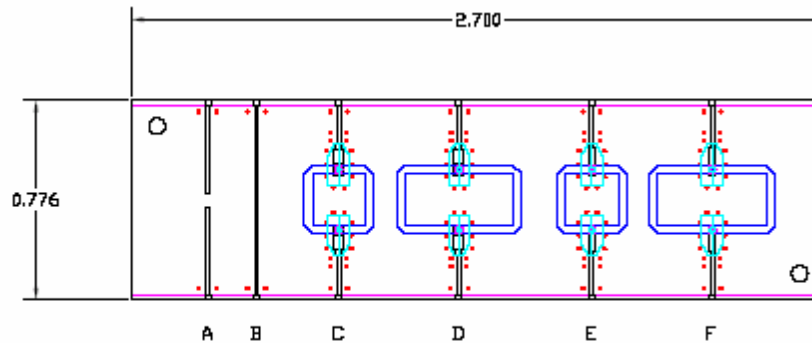
plated to 35 μm (1 oz.)

2.54 – 3.81 μm (100 – 150 $\mu\text{-inches}$) nickel,

3.048 – 4.572 μm (120 – 180 $\mu\text{-inches}$) gold



Microstrip to Stripline Transition: Test Board



Artifacts A, B
Reflect and Line standards.
Thru std in part 1022579, stripline coupling test board.
Artifacts C, D
Optimized for 50 Ohm
Artifacts E, F
FEP Patch-notched r58fepr2_tycoadv

BOARD_OUTLINE1		BOARD_OUTLINE2		LAYER STACKUP		
	LAYER_1_DC1_PATCH		LAYER_3_SIGNAL		VIA1	.010 RT6002
	LAYER_2		LAYER_3_GND_TOP		VIA2	.0015 Speedboard
	LAYER_3_GND_TOP	DRILL1	LAYER_4			.010 RT6002
	LAYER_4		LAYER_5_SIGNAL			.001 FEP
	LAYER_5_SIGNAL		LAYER_6_GND_BOTTOM			.010 RT6002
	LAYER_6_GND_BOTTOM					

LAYER_1_DC1_PATCH	.0007 Cu (1/2 oz)	TRACE
LAYER_2 (empty)	NO COPPER	
LAYER_3_GND_TOP	.0007 Cu (1/2 oz)	SLOT
LAYER_4 (empty)	NO COPPER	
LAYER_5_SIGNAL	.0007 Cu (1/2 oz)	TRACE
LAYER_6_GND_BOTTOM	.0007 Cu (1/2 oz)	SLOT

VIA1 .010 DIA FILLED
VIA2 .010 DIA FILLED

PLATING

LAYERS 1, 6: Gold per specification below

LAYER 5: Gold per specification below on exposed RF pads only.
DO NOT PLATE BURIED COPPER

Gold finish per MIL-G45204 Type 3
Ni 100 to 150 u-inches
Au 120 to 180 u-inches

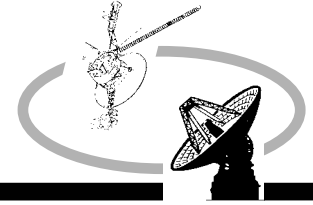
Materials
RT6002 1/2 oz rolled copper
Gore Speedboard standard resin

Dimensions in inches
Outside dimension tolerance +/- .002

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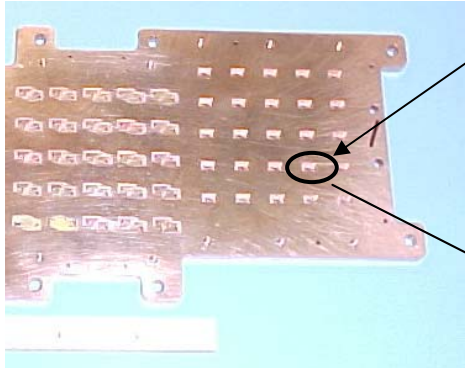
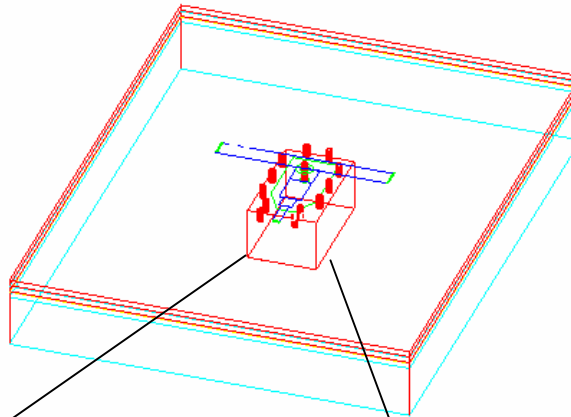
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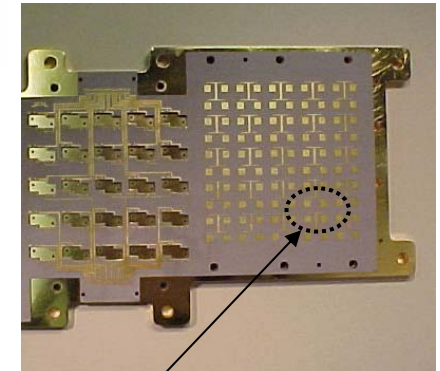


Ka-Array Patch Antenna Simulation vs. Measurement: includes Microstrip to Stripline Transition

Design fabricated with
1.5 mil Speedboard ($\epsilon_r=2.6$, $\tan\delta=0.004$)
10.7 mil 6002 ($\epsilon_r=3.005$, $\tan\delta=0.0012$)



Baseplate showing cavity: under transition



Antenna array on
Circuit Board
using the transition

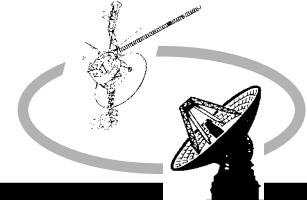


Buried line in circuit board: input to transition

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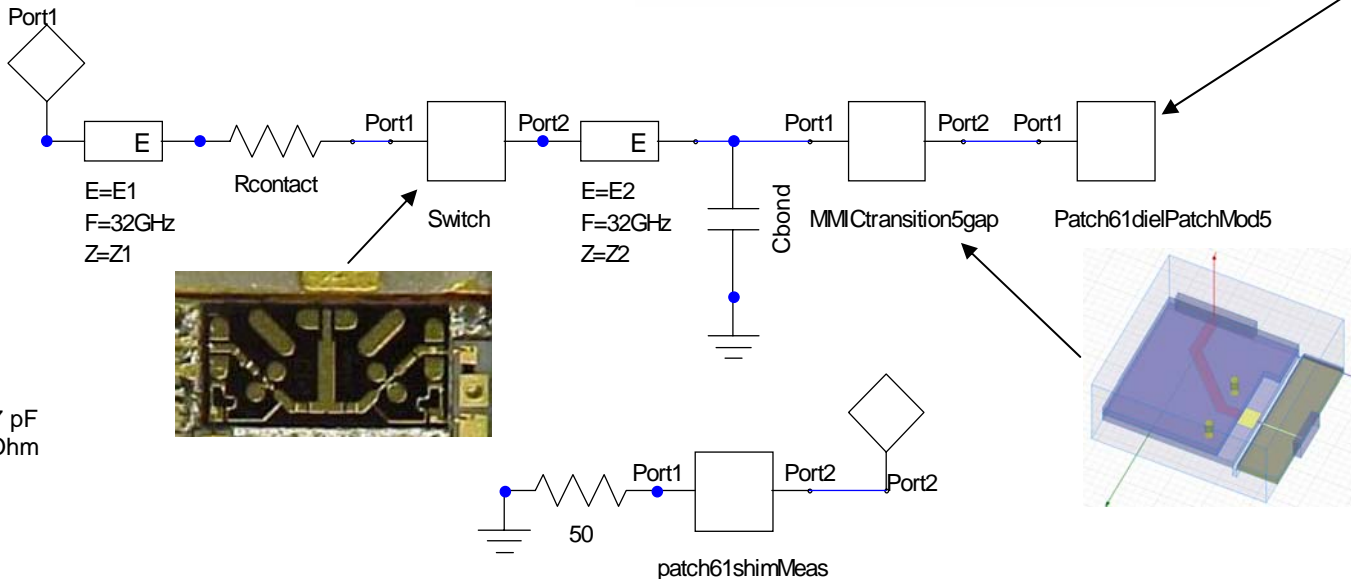
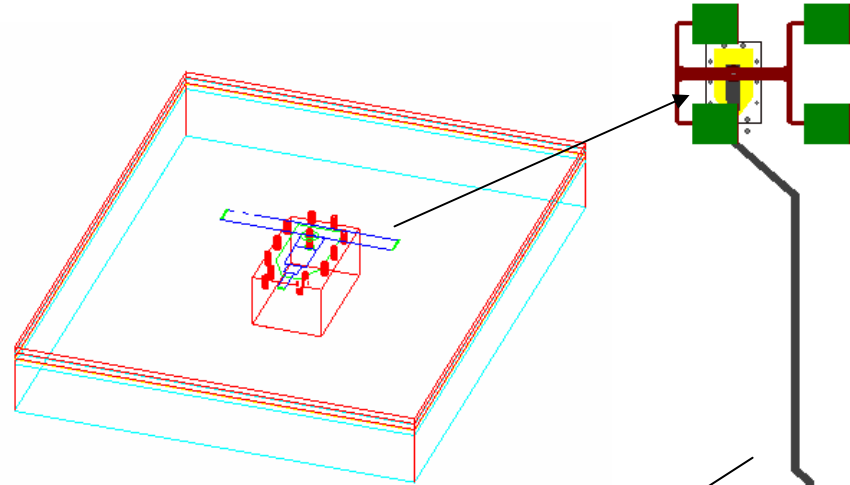
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Ka-Array Patch Antenna Simulation vs. Measurement: includes Microstrip to Stripline Transition

Speedy Design with
 1.5 mil Speedboard ($\epsilon_r=2.6$, $\tan\delta=0.004$)
 10.7 mil 6002 ($\epsilon_r=3.005$, $\tan\delta=0.0012$)
 4 mil GaAs ($\epsilon_r=12.9$, $\tan\delta=0.0$)
 5 mil MMIC to board gap
 14 mil well depth below board ground

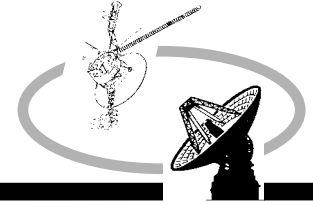


$E1=14$ deg
 $Z1=14$ Ohm
 $E2=42$ deg
 $Z2=56$ Ohm
 $C_{bond}=0.097$ pF
 $R_{contact}=5$ Ohm

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Ka-Array Patch Antenna Simulation vs. Measurement: includes Microstrip to Stripline Transition

