Offset-PLL based frequency up-conversion for low spurious transmission

Master's thesis
performed in **Electronics Systems**

by
Anders Nilsson

Reg nr: LiTH-ISY-EX-3450-2003

16th June 2003

Offset-PLL based frequency up-conversion for low spurious transmission

Master's thesis

performed in **Electronics Systems**,
Dept. of Electrical Engineering
at **Linköpings universitet**

by **Anders Nilsson**

Reg nr: LiTH-ISY-EX-3450-2003

Supervisor: **Ingvar Söderman**
Sectra Communications AB

Examiner: **Kent Palmkvist**
Linköpings Universitet

Linköping, 16th June 2003

Avdelning, Institution
Division, Department

Electronics Systems,
Dept. of Electrical Engineering
581 83 Linköping

Datum
Date

25 maj 2003

Språk
Language
☐ Svenska/Swedish
☒ Engelska/English
☐ _____

Rapporttyp
Report category
☐ Licentiatavhandling
☒ Examensarbete
☐ C-uppsats
☐ D-uppsats
☐ Övrig rapport
☐ _____

ISBN
—

ISRN
LITH-ISY-EX-3450-2003

Serietitel och serienummer
Title of series, numbering

ISSN
—

URL för elektronisk version
http://www.es.isy.liu.se
http://www.ep.liu.se/exjobb/isy/2003/3450/

Titel Offset-PLL-baserad modulator för högpresterande sändarsystem

Title Offset-PLL based frequency up-conversion for low spurious transmission

Författare
Author Anders Nilsson

Sammanfattning
Abstract

The goal of this final year project is to investigate various techniques to up-convert a baseband signal into radio frequency signals, and to investigate the practical problems encountered in an offset phase locked loop design by implementation.

Phase locked loops are commonly used in radio transmitters and receivers to generate accurate RF signals from a low-frequency reference. This thesis will highlight some of the problems and strengths of various up-conversion schemes, and suggest an offset-PLL architecture free from many of those problems.

An offset-PLL is often used in mobile communication systems where the required levels of out of band transmission are tough and the use of superheterodyne up-conversion cannot be used due to spectrum or bandwidth requirements.

However a drawback of an offset-PLL is the high locking time; this can render the offset-PLL useless in TDMA communication systems. This problem among others has been studied theoretically as well as practically on an actual implementation of an offset-PLL for mobile communications. The offset-PLL was designed and manufactured as part of this project.

Nyckelord
Keywords Offset-PLL, low spurious, up-conversion, radio, transmitter, modulator

Abstract

The goal of this final year project is to investigate various techniques to up-convert a baseband signal into radio frequency signals, and to investigate the practical problems encountered in an offset phase locked loop design by implementation.

Phase locked loops are commonly used in radio transmitters and receivers to generate accurate RF signals from a low-frequency reference. This thesis will highlight some of the problems and strengths of various up-conversion schemes, and suggest an offset-PLL architecture free from many of those problems.

An offset-PLL is often used in mobile communication systems where the required levels of out of band transmission are tough and the use of superheterodyne up-conversion cannot be used due to spectrum or bandwidth requirements.

However a drawback of an offset-PLL is the high locking time; this can render the offset-PLL useless in TDMA communication systems. This problem among others has been studied theoretically as well as practically on an actual implementation of an offset-PLL for mobile communications. The offset-PLL was designed and manufactured as part of this project.

Contents

List of Figures

Acknowledgements

This final year project has been carried out at Sectra Communications AB, a company in the Sectra group in Linköping.

I would like to thank my supervisor Ingvar Söderman and my colleagues, Magnus Fransson, Bengt Sjöström and Frithjof Qvigstad for their invaluable help and comments during the project.

I would also like to thank my supervisor at ISY, Kent Palmkvist.

1

Introduction

1.1 Preface

This report describes a final year project conducted during spring 2003 at Sectra Communications AB. The goal of the project was to investigate the problems encountered during design and implementation of an offset-PLL.

1.2 About Sectra

Sectra is one of Sweden's fastest growing high-tech companies in the IT area. Since the mid-1980s, Sectra has developed and sold cutting edge solutions in niche segments wherein Sweden is an early adopter and leads the technical development.

Sectra has more than 270 employees in eight countries and operations that reach out to customers all over the world. Sectra AB is a divided into three branches:

- Medical Systems.
- Secure Communication Systems.
- Wireless Information Systems.

The author has been a part time Sectra employee since 1997.

1.3 Method

The project was conducted in the following fashion:

- Literature study.
- Development and drawing of schematics.
- PCB Layout and component selection.
- PCB manufacturing.

- Software development.
- Test and evaluation.
- Analysis of results.
- Report writing.

About two months of the project time was used to study different up-conversion architectures and make simulations in Matlab. Another two months were devoted to hardware design, and printed circuit board layout. The last month was used to measure the performance of the offset-PLL and to write this report.

1.4 Report

1.4.1 Reading instructions

The purpose of this report is to highlight some of the benefits and problems of using an offset-PLL compared to other up-conversion schemes.

Some basic knowledge of radio systems, radio design and digital design is required to fully benefit from this report.

Throughout this thesis it is assumed that the selected modulation scheme has constant envelope, i.e. frequency or phase modulation.

1.4.2 Outline

First a short introduction to up-conversion will be given. Following the introduction, common up-conversion techniques will be presented. Their problems and strengths will also be discussed.

Further, the concept of an offset-PLL is presented and an architecture is proposed. The implementation and the results from the implementation is finally analyzed and concluded.

1.5 Tools

During this final year project the following tools have been used:

- *PC-Filter* for filter synthesis.
- *ARRL Radio designer* for filter analysis and design.
- *Mentor Graphics Expedition PCB* for schematic entry and PCB layout.
- *Spice* for analog simulation.
- *Emacs, XFig* and LaTeX for report writing.

2

Background

2.1 Introduction to up-conversion

Up-conversion is the process of converting a baseband signal to a passband signal at a higher frequency. This can be described as a shift of the signal in the frequency domain. See Fig 2.1.

In a digital transmission system, the binary information which the system is going to transmit must be converted to an analog representation. The resulting waveform is called a *baseband signal.* The baseband signal is usually created by a signal processor or similar digital circuit which also encodes the data and often adds error correction information.

In a typical modern radio system, the signal which is to be transmitted is usually created digitally in baseband form. A baseband signal is an signal carrying the desired information centered around zero in the frequency domain. As it is very inconvenient to transmit baseband signals over the air the baseband signal is converted to a higher frequency by up-conversion.

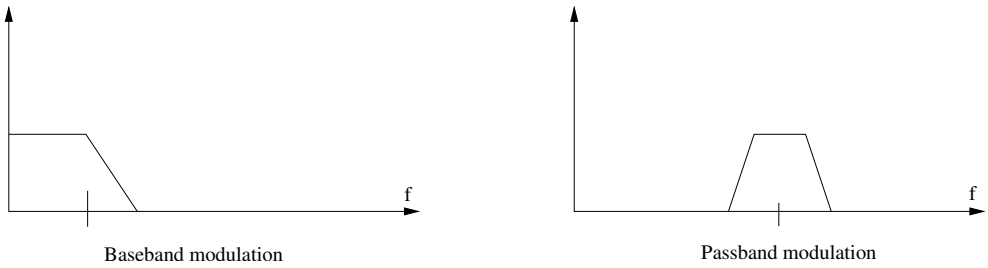

Figure 2.1: Baseband v.s. Passband signal

Mathematically, up-conversion can be considered a multiplication of the baseband signal by a carrier frequency, often referred to as local oscillator, *LO*.

2.2 Nonlinearities

The main problems in all up-conversion techniques using multiplication are nonlinearities in the component responsible for the multiplication.

If a sinusoidal signal is passed through a nonlinear component, harmonics will be created.

$$RF_{in} = \sin(\omega t)$$

$$RF_{out} = \alpha_1 \sin(\omega t) + \alpha_2 \sin(2\omega t) + \alpha_3 \sin(3\omega t) + ...$$

One common method is to use a double balanced mixer where all even harmonics almost cancel each other. The RF signal will then become:

$$RF_{out} = \alpha_1 \sin(\omega t) + \alpha_3 \sin(3\omega t) + ...$$

2.3 Up-conversion schemes

To achieve a clean transmission of baseband signals many different up-conversion methods can be used. For example:

- Homogenous up-conversion. This scheme converts the baseband signal directly to the desired frequency without any intermediate frequency.
- Heterogenous up-conversion. This class of up-converters uses one or many intermediate frequencies during the up-conversion process.
- Direct digital synthesis, *DDS*. Direct digital synthesis is a completely digital solution which creates the desired output signal without analog baseband signals or intermediate frequencies.

Even though every method's aim is to achieve perfect up-conversion the weaknesses of each different architecture cannot be ignored. In the following chapters, the different architectures will be described and analyzed.

3

Architecture description

3.1 Transmitter architectures

Selecting the right transmitter architecture is very important, and can be the difference between product success and failure. There are many different up-conversion methods available. However, the need to optimally utilize the available spectrum restricts the designers choice between different architectures. This chapter will highlight some of the features and the functions of the most common up-conversion methods.

3.1.1 Homodyne up-conversion

Homodyne up-conversion implies that the baseband signal is directly converted to the desired frequency. In order to avoid signal corruption by aliasing, the baseband signal must be represented as a complex valued signal.

The real value is referred to as the in-phase, I component whereas the imaginary value is referred to as the quadrature-phase, Q component.

The output signal is described by:

$$RF = I \cdot \cos \omega_{LO} + Q \cdot \sin \omega_{LO}$$

The baseband signal can either be directly converted to the desired frequency by a complex mixer (so called IQ-mixer), or by two separate mixers and a combiner, as seen in figure 3.1.

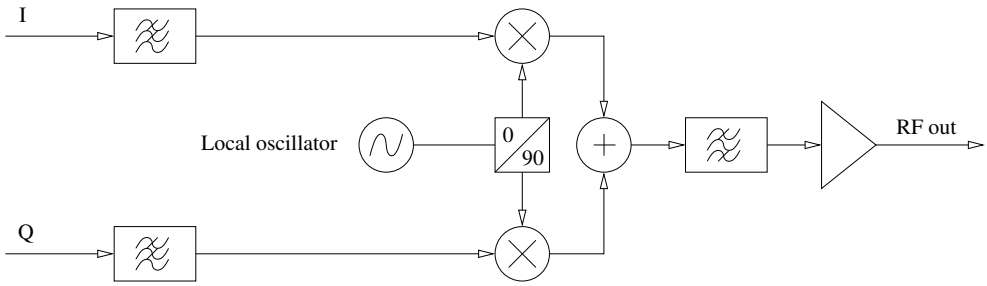

Figure 3.1: Homodyne transmitter

The baseband signals are often digitally low-pass filtered in the signal processor or in a DAC incorporating a digital noise shaping filter. This ensures that the spectrum of the baseband signal entering the mixer has a clean spectrum, free from unwanted harmonics.

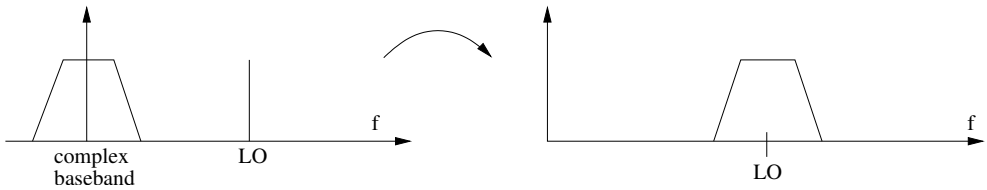

Figure 3.2: Homodyne up-conversion

3.1.2 Heterodyne up-conversion

Unlike homodyne up-conversion, heterodyne up-conversion uses an Intermediate Frequency during up-conversion. Either the baseband signal is first transformed to an intermediate frequency by modulating a tunable oscillator, or the intermediate signal is created directly by a digital signal processor.

The intermediate frequency is then filtered by a special band-pass IF-filter, often a very narrow crystal or ceramic filter. This procedure ensures that the intermediate frequency has a clean spectrum before it is fed into the mixer. Usually the intermediate frequency has a low frequency compared to the radio frequency.

The resulting RF signal is described by:

$$RF = \cos(\omega_{LO}) \cdot \cos(\omega_{IF}) = \underbrace{\frac{\cos(\omega_{LO} - \omega_{IF})}{2}}_{desired} + \underbrace{\frac{\cos(\omega_{LO} + \omega_{IF})}{2}}_{image}$$

Figure 3.3 illustrates the resulting spectrum from a ideal up-conversion.

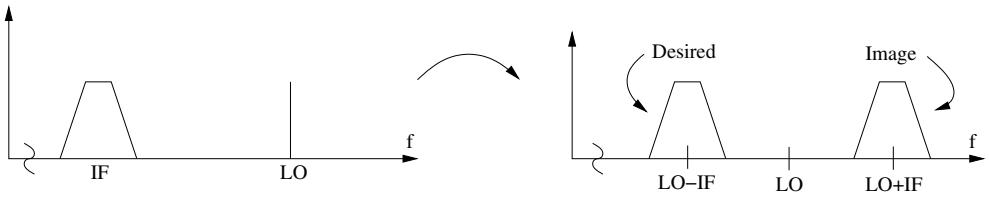

Figure 3.3: Heterodyne up-conversion

Due to signal modulation to the intermediate frequency, the intermediate frequency must be filtered by a narrow band pass filter before it is fed to the mixer. The resulting architecture is realized as follows:

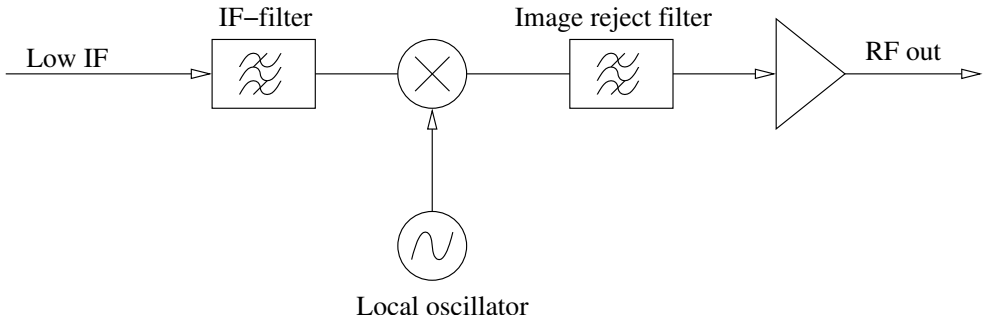

Figure 3.4: Heterodyne transmitter

The intermediate frequency and corresponding filter are often in the range from 10.7 MHz to 71 MHz depending on the current design. The selection of the intermediate frequency is crucial and it is discussed later in this chapter.

The intermediate frequency is real-valued, in contrast to the complex valued baseband signal used in homogenous up-conversion. This allows the use of a regular mixer instead of an IQ-mixer, and will thus reduce the unit cost and complexity.

Heterodyne up-conversion is the most used method of up-converting signals. The intermediate frequency is usually created by modulating a fixed frequency modulator, or by adding the desired baseband signal in the PLL feedback loop. Engineers have continued to improve the method and as a result a modified architecture has been developed.

This architecture is called *superheterodyne up-conversion* and is a sub class of heterodyne up-conversion and is even more popular than regular heterodyne up-conversion.

The main difference between superheterodyne up-conversion and heterodyne up-conversion is the use of two or more intermediate frequencies during the up-conversion process. The structure is presented in figure 3.5.

This allows the designer to use a higher frequency on the final intermediate frequency and thus position any image out of a large band.

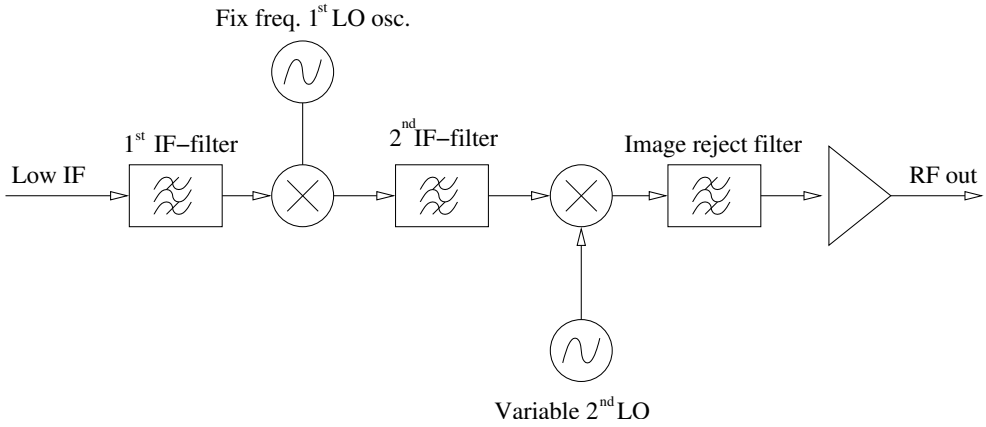

Figure 3.5: Superheterodyne transmitter

Although heterodyne and superheterodyne up-conversion are the most used up-conversion methods they have their drawbacks too.

A drawback of heterodyne up-conversion is that it is hard to know exactly the deviation of the transmitted signal, unless the low intermediate frequency is created by a signal processor or equivalent.

The frequency components in the different stages of up-conversion are presented in figure 3.6. The first intermediate frequency IF_1 is created by a signal processor and then multiplied by the carrier frequency of the first fix-frequency local oscillator LO_1. The result of the multiplication is the desired product consisting of the differance term $LO_1 - IF_1$ and the image at $LO_1 + IF_1$. Here the desired frequency component is selected by a narrow band pass filter. The procedure is then repeated and finally the desired frequency component is selected by an image reject band filter at the output of the modulator. This filter can both be of a band-pass or a low-pass type.

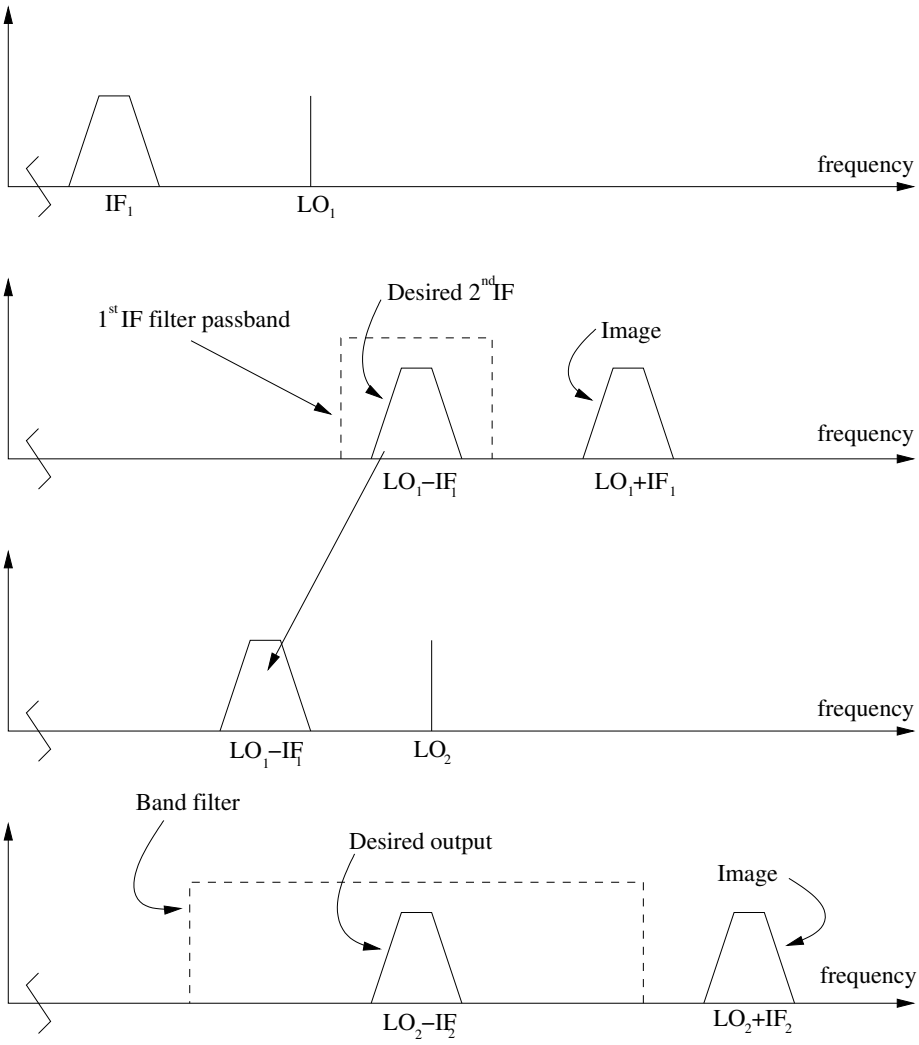

Figure 3.6: Spectrum in the different stages in superheterodyne up-conversion

3.1.3 Direct Digital Synthesis

Direct Digital Synthesis, *DDS*, is a completely different approach to create a modulated carrier at radio frequencies. Unlike both homodyne and heterodyne up-conversion methods, it creates the radio frequency directly from digital modulation information.

Besides a digital to analog converter and a reconstruction filter, the DDS is a completely digital component.

A typical direct digital synthesis system consists of:

- A phase accumulator.
- A frequency register.
- A modulation register.
- A cosine ROM.
- A digital to analog converter.
- A reconstruction filter.

The block diagram of a DDS is shown in figure 3.7.

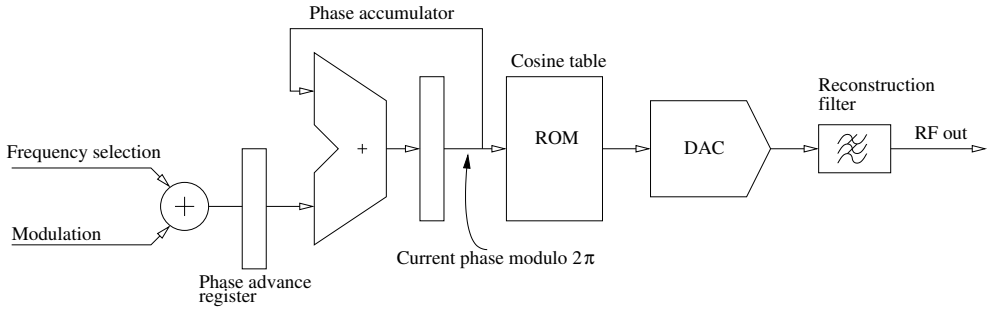

Figure 3.7: Schematic view of a DDS

The principle of direct digital synthesis is to use a phase accumulator to index a sine or cosine table stored in a memory. The memory content is then fed to a digital to analog converter and later to a reconstruction filter to smoothen the signal.

The sum of the contents of both the frequency register and the modulation register is called *phase advance*.

The desired output frequency is derived from the clock frequency and the phase advance every clock cycle.

$$RF = \cos\left(\frac{\phi_{advance} \cdot f_{clk}}{2\pi}\right)$$

Figure 3.8 illustrates the main waveforms in a direct digital synthesizer. The upper waveform illustrates a modulated output signal. The carrier frequency is selected by changing the stationary phase advance. In this example the stationary phase advance is $\frac{\pi}{4}$. Then modulation with a deviation of $\pm\frac{\pi}{10}$ is added to the stationary phase advance. This modulation is shown as the ripple of the line in the lower figure.

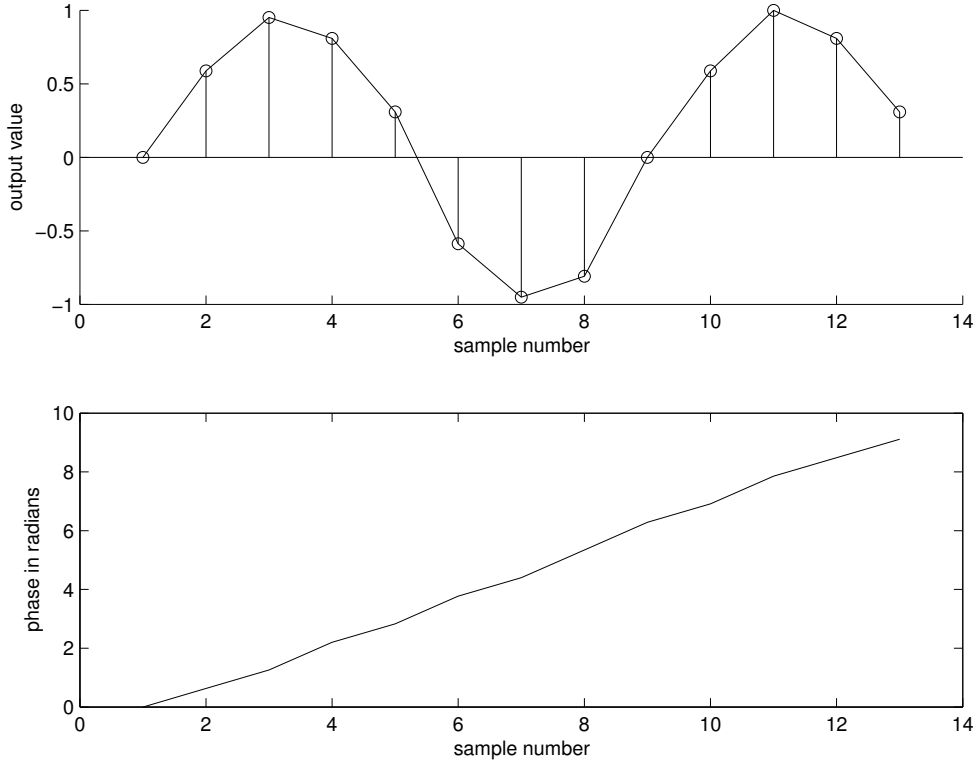

Figure 3.8: Waveforms in a DDS

As described earlier frequency selection is done by incrementing the phase by a constant value each clock cycle and then adding or subtracting the desired phase modulation. In this way, the output frequency can be tuned and modulated without changing the clock frequency of the DDS.

`Example`: The sample frequency is selected to 1 GHz, and the user want to create a carrier frequency of 100 MHz.

The DDS then needs to increase its phase accumulator by $\frac{f_{out}\cdot 360^\circ}{f_s}$ degrees every sample.

$f_{out} = 100MHz, f_s = 1GHz \rightarrow \phi_{advance} = \frac{100\cdot 10^6\cdot 360}{1\cdot 10^9} = 36^\circ$ per sample.

One drawback is that if the DDS is tuned to a high frequency, the number of sample points per output signal period will become low and thus require a very good reconstruction filter in order to maintain good spectral properties.

4

Architecture analysis

4.1 Architecture analysis

As mentioned before each architecture has its own drawbacks. In the following pages the most occurring drawbacks of the three up-conversion methods will be raised and discussed.

4.1.1 Homodyne up-conversion

Homodyne architectures will suffer from nonlinearities in the mixer. In the mixer, harmonics of both the local oscillator and the baseband signal will be produced by nonlinearities. This is illustrated in figure 4.1.

Harmonics of the local oscillator can easily be filtered out by an external low-pass filter because they have at least one octave higher frequency. On the other hand, baseband harmonics are a greater problem since they cannot easily be filtered out. They can however be reduced by careful mixer design or mixer selection. But generally it is hard to create a high performance mixer covering a large band, i.e., the avionics band[1] or a military VHF band.

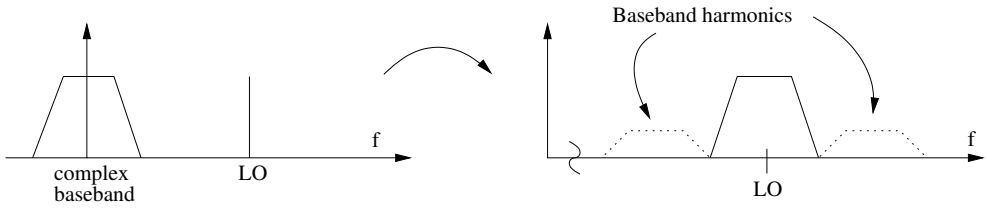

Figure 4.1: Nonlinearities in a homodyne up-converter

[1] 108 MHz to 137 MHz

In the following example, a 130 MHz carrier has been modulated by 12.5 kHz sinusoidal on both the in-phase and the quadrature channel. Figure 4.2 illustrates the result due to mixer nonlinearities.

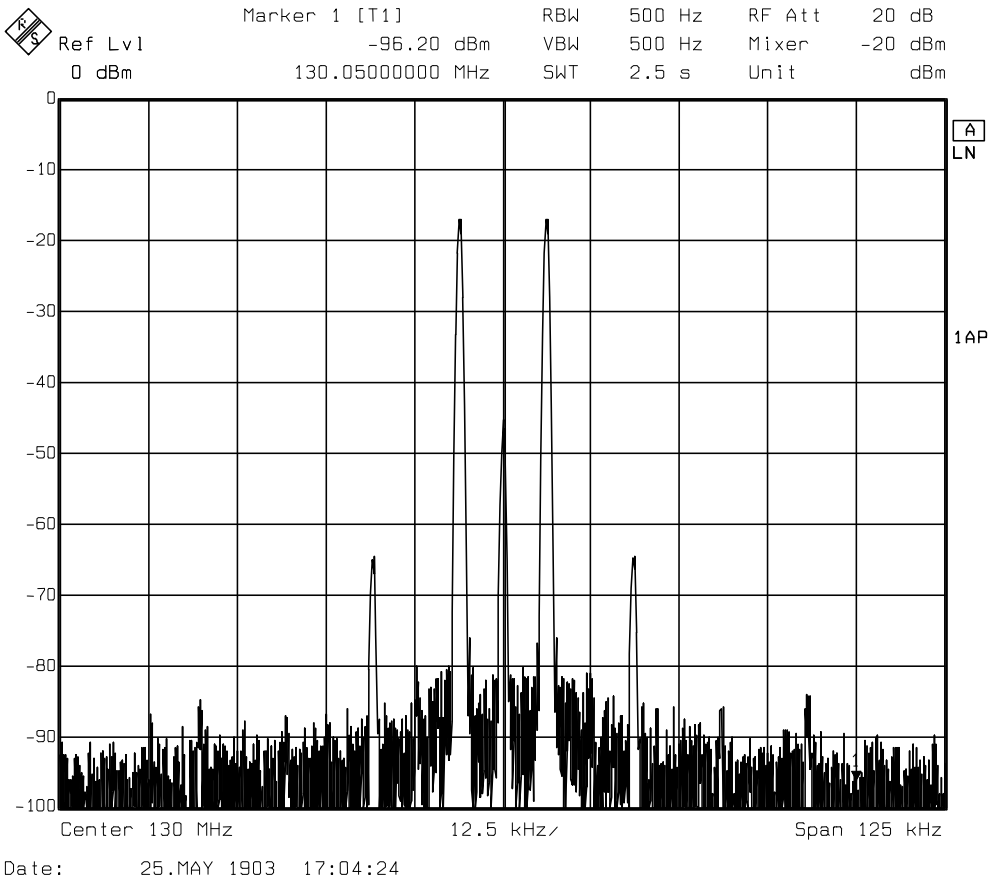

Figure 4.2: Mixer nonlinearities in homodyne up-conversion

Homodyne up-conversion require high amplitude and phase accuracy over a large frequency band. These mixer imperfections can almost be completely corrected by a digital correction filter in the DSP.

4.1.2 Heterodyne up-conversion

Due to the non-linear behavior of a real mixer, harmonics of both the intermediate frequency and the local oscillator will be created.

All of the intermediate frequencies will mix with the local oscillator harmonics and create a huge amount of mixing products called spurs.

Perfect mixing:

$$RF = \underbrace{\cos\left(\Omega_{IF} - \Omega_{LO}\right)}_{in\ band\ spurs} + \underbrace{\cos\left(\Omega_{IF} + \Omega_{LO}\right)}_{high\ frequency\ spurs}$$

Here $\Omega_{IF} = n \cdot \omega_{IF}$ and $\Omega_{LO} = m \cdot \omega_{LO}$ where $n, m = \pm 1, \pm 2...$

The resulting radio frequency signal will contain both sums and difference frequencies as shown above.

The frequency components which are a sum of a local oscillator harmonic and an intermediate frequency harmonic can easily be filtered out by a low-pass filter due to their high frequency. The frequency components which arise from difference products will however create signals which lie in the band of interest.

`Example:` Lets assume the up-converter is designed to work in the avionics band which covers 108-137 MHz. The designer has chosen the intermediate frequency to be 45 MHz.[2]

The desired output frequency is 135.1 MHz and the intermediate frequency is 45 MHz.

$f_{IF} = 45MHz, f_{LO} = 180.1$ MHz with the desired output frequency $180.1 - 45 = 135.1$ MHz, and the image at $180.1 + 45 = 225.1$ MHz.

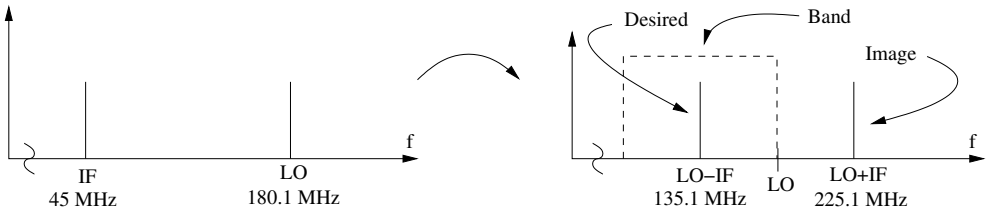

Figure 4.3: Example of ideal up-conversion

Theoretically, the only frequency component inside the desired band is the signal on 135.1 MHz.

[2]This is a common intermediate frequency in industry.

However in a real life measurement on the last example, the following output spectrum was measured.

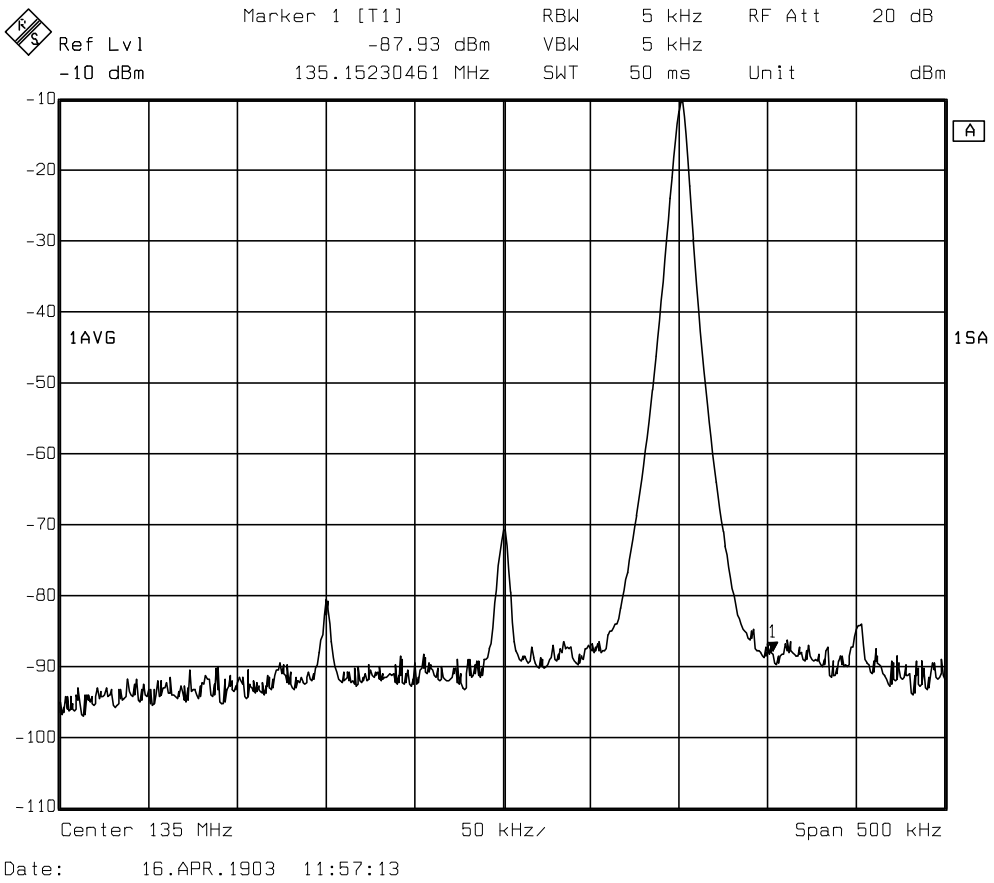

Figure 4.4: Measured output spectrum

In figure 4.4 unwanted frequency components are clearly visible. The unwanted frequency components that appear in the spectrum are referred to as *spurs* or *spurious frequency components*. The spurs arise from nonlinearities in the mixer as mentioned before.

A realistic model of any real mixer is shown in figure 4.5.

This is typical for heterodyne up-conversion and is hard to avoid if the system is designed to cover a large frequency band.

The following result was created by Matlab simulations of the previous example using the mixer model in figure 4.5. The exact amplitude of the spurs seen in figure 4.6 cannot be determined since they are dependent of the bandwidth of the mixer and the attenuation of high frequency harmonics in the mixer.

In figure 4.6 the amplitude of the harmonics is inversely proportional to their order.

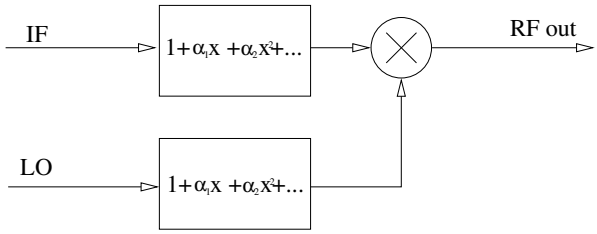

Figure 4.5: A realistic model of a mixer

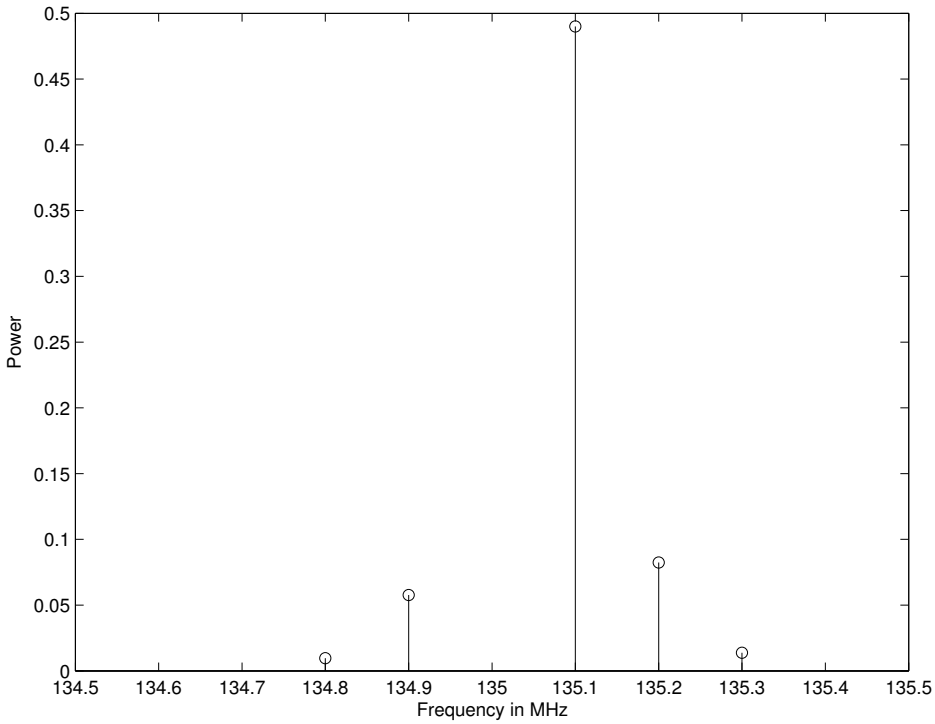

Figure 4.6: Calculated output spectrum

In order to determine in which frequency ranges the system is affected by spurs, every spur created by harmonics up to the 11:th order is calculated in Matlab.

The number of spurs within a certain frequency distance from the desired frequency can be estimated by calculating all harmonics of both the local oscillator and the intermediate frequency, and their sum and difference.

In the following example, the number of spurs within 10 MHz from the desired frequency is calculated for different local oscillator values between 100- and 200 MHz. In this example the intermediate frequency is set to 45 MHz.

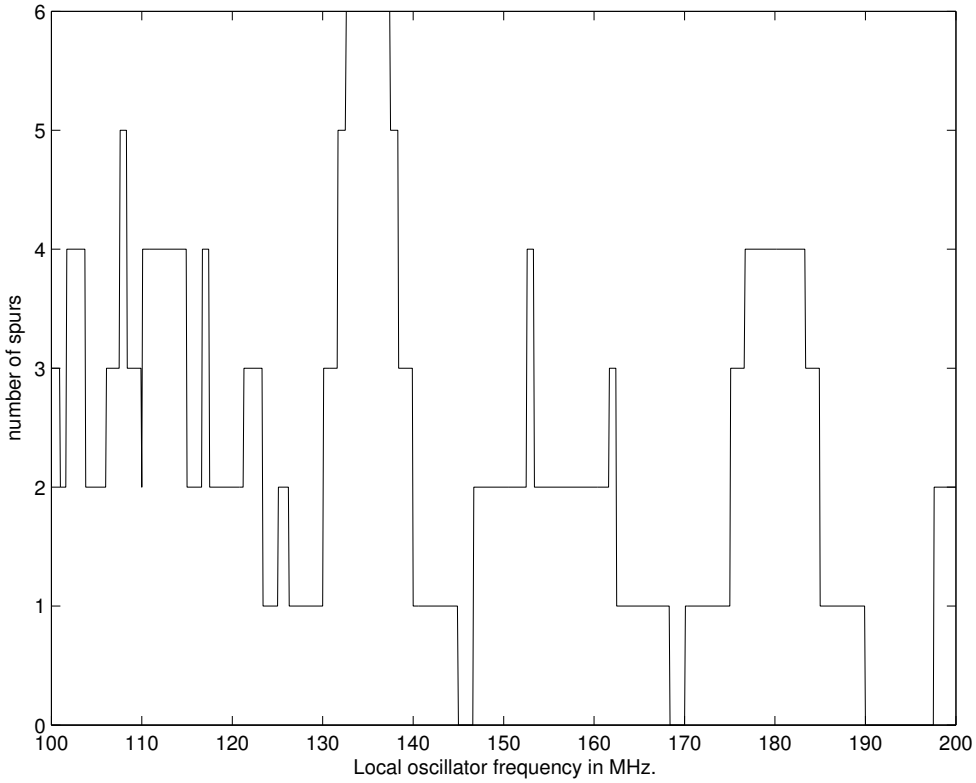

Figure 4.7: An estimation of the number of spurs within 10 MHz from the desired signal.

This example highlights the most important problem with heterodyne up-conversion. As seen in figure 4.7, it is almost impossible to avoid spurs even in a small fraction of a large band.

By choosing another intermediate frequency the designer can avoid spurious frequencies in a small fraction of a larger band. As a general rule the intermediate frequency must obey the following rule:

$$f_{if} > 2 \cdot BW$$

where BW is the width of the band. In this way the spurs with the highest energy are placed

out of band. However, this can still be problematic since the same or stricter spectrum rules are applied for out of band as in-band signals.

4.1.3 Direct Digital Synthesis

The main benefit of Direct Digital Synthesis is the ability of immediate frequency change. This property is essential in frequency hopping systems.

The drawbacks of DDS are the harmonics. Harmonics of the desired signal will suffer from folding around the sampling frequency. This folding will create non-desired signals in the band of interest, and thereby restrict the useful operating frequency range of the DDS. This increases the demand for linearity in the associated DAC.

The useful operating range is also limited by the clock-rate of the DDS and the increasing complexity of the reconstruction filter when the desired frequency approaches half the sample rate.

Other drawbacks of a DDS solution are high power consumption and price. A typical DDS capable of cover the avionics band costs about $\$50$ and consumes 2 Watt.[3]

In spite of its advantages, both the high price and the high power consumption prevent designers of using direct digital synthesis in mobile terminals.

4.2 Conclusions

As stated before, choosing the right transmitter architecture is very important. At the same time, architecture choice is one of the hardest choices to do in a transceiver design.

If the product is to operate within a small band, the heterodyne architecture is preferred since it can be implemented quite efficiently and cost effectively.

By selecting a suitable intermediate frequency the problem of spurs can be eased, if not eliminated. However, this is not possible if the band is broad. If a large band is to be covered, the homogenous architecture is preferred since it will not suffer from spurs in the same sense as a heterogenous architecture. Instead the homogenous architecture will require a highly linear complex-valued mixer in order to suppress baseband harmonics. Also, more processing power is required to facilitate a digital equalizer which can compensate for the imperfections in the mixer and baseband filters. This will make the product more complex and increase the unit price.

Another alternative is to use an offset PLL. This solution is free from many of the problems associated with up-conversion in the other discussed methods. The offset PLL is able to operate in a broad band without image or spur problems.

In the next chapter a proposed offset PLL architecture is presented and analyzed.

[3] Performance figures from Analog Devices AD9858 1 GSPS DDS, `www.analog.com`

5

Offset-PLL

5.1 Offset-PLL basics

5.1.1 Analog phase detector

The key component in every phase locked loop is the phase detector. This component compares the phase of two signals and provides a signal proportional to the phase difference.

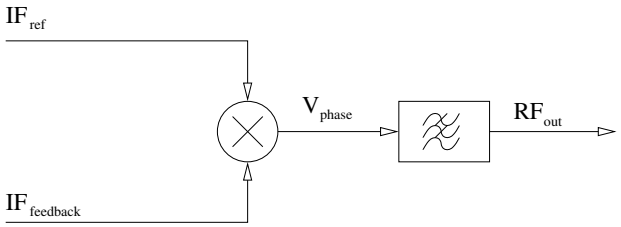

Figure 5.1: Analog phase detector

A mixer can be used as analog phase detector if the output is low-pass filtered.

$$IF_{ref} = \sin\left(\Omega_{ref} + \Phi_{ref}\right)$$

$$IF_{feedback} = \sin\left(\Omega_{fb} + \Phi_{fb}\right)$$

$$\Omega_{ref} \tilde{=} \Omega_{fb}$$

$$V_{phase} = \cos\left(\Phi_{ref} - \Phi_{fb}\right) + \underbrace{\cos\left(\Omega_{ref} + \Omega_{fb} + \Phi_{ref} + \Phi_{fb}\right)}_{removed\ by\ channel\ filter}$$

Using a mixer as phase detector will provide a 90 degree phase shift of the output signal. The purpose to use an analog phase detector is to lower the phase noise of the system. An analog phase detector has less noise than a digital phase detector.

5.1.2 Operation

Figure 5.2 illustrates the offset-PLL.

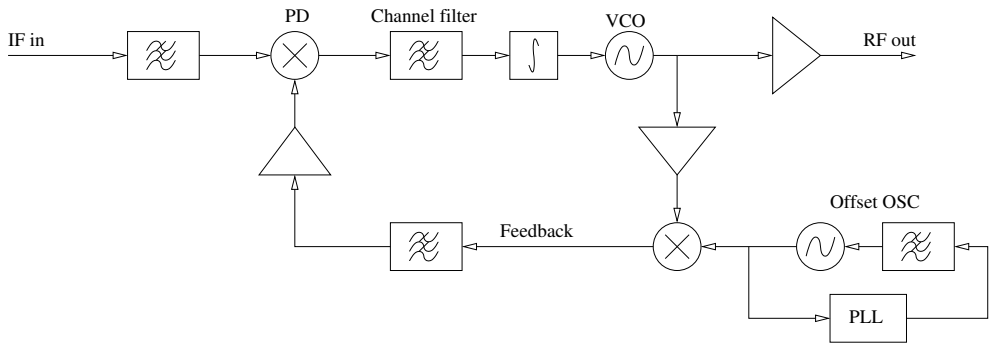

Figure 5.2: Offset-PLL

The intermediate frequency signal from the modulator is multiplied by the feedback signal. The resulting phase error is then low pass filtered and integrated to form the control voltage to the VCO.

The resulting baseband signal from the phase detector (mixer) can be described by:

$$V_{phase} = \underbrace{\cos\left(\Phi_{ref} - \Phi_{fb}\right)}_{baseband} + \underbrace{\cos\left(\Omega_{ref} + \Omega_{fb} + \Phi_{ref} + \Phi_{fb}\right)}_{removed\ by\ channel\ filter}$$

The baseband component is integrated in order to form a control voltage to a voltage controlled oscillator.

$$f = \int \Phi dt$$

The feedback signal is created by down-converting the output signal with the offset-frequency. The offset-frequency is provided by an offset-frequency oscillator and its respective PLL.

In this way, the structure forms a closed loop, which ensures that the output is an up-converted version of the intermediate frequency.

The performance of this loop is mainly determined by the bandwidth of the loop filter and the gain of the integrator. The ability to handle large frequency deviations as those created by channel switching is also a very important design issue which needs to be addressed. These issues are treated in a following chapter.

5.2 Offset-PLL characteristics

Because the output signal is not up-converted using mixers, the output spectrum will not contain images of the transmitted signal, and more important, it will not contain any spurs created by mixer nonlinearities.

This property is especially important when the transmitter is required to cover a large band. As stated earlier, a heterodyne architecture can successfully cover a small portion of a designated band, but will suffer from spurs when the band increases.

Another very important feature of the offset-PLL is that it allows the use of high power voltage controlled oscillators. In professional systems, the designer wants to use as high as possible power in the oscillator since this reduces the phase noise.

A drawback of the proposed architecture is that it can only be used in systems using constant envelope modulation since the RF signal created by the VCO is fed directly to the transmitter.

This restricts the choice of modulation schemes to those which have a constant envelope, for example GMSK, M-PSK, FSK and others. However, the architecture could be extended to support non-constant envelope by allowing amplitude modulation of the power amplifier, but this is not studied in this thesis. Such architecture is referred to as a polar loop.

6

Demonstrator design

This chapter describes the design of the offset-PLL demonstrator. The design and implementation of this offset-PLL based up-converter accounts for about 2 months of full time work.

The main purpose of the demonstrator was to find out what problems were encountered during the design of an offset-PLL.

This demonstrator of the proposed system is designed to be used as a part of a VHF aircraft transponder system. Aircraft radio equipment is governed by strict spectrum regulations and it is the purpose of this demonstrator to comply to these rules.

6.1 System environment

The transponder system has the following requirements on the modulator and the offset-PLL:

- The system operates in the frequency range of 108-137 MHz.
- The modulation scheme can be either GMSK or GFSK.
- The system data rate is 19.2 kbit/s.
- The channel spacing is 25 kHz.

These requirements can be transformed to form requirements on the offset-PLL. The offset-PLL must be able to operate with full performance within the whole specified band. It must also use an intermediate frequency which allows the modulator to fulfill the data rate and modulation scheme requirement.

6.2 Proposed architecture

I propose an architecture similar to the architecture seen in figure 5.2. The proposed architecture is presented in figure 6.1.

The proposed architecture consists of the basic offset-PLL from figure 5.2 and control and supervision units.

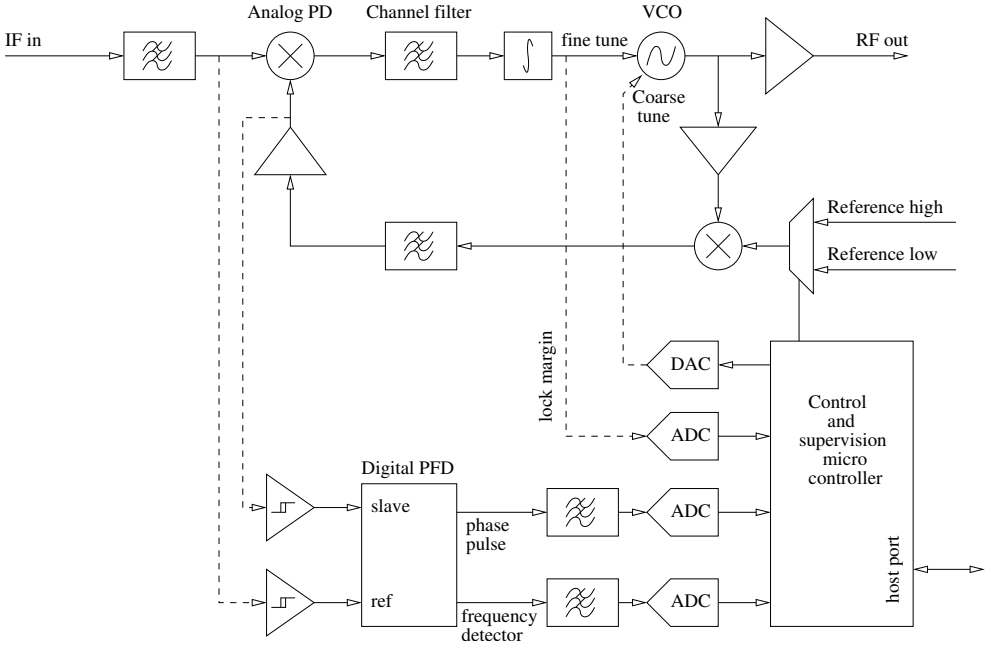

Figure 6.1: Proposed architecture

The control and supervision interface to the offset-PLL is illustrated by dashed lines in figure 6.1. It consists of:

- A digital phase and frequency detector.
- Analog to digital converters for supervision.
- Digital to analog converter for control.
- A microcontroller with a host interface.

6.3 Design

In order to fully understand the difficulties related to an offset-PLL design, a complete up-converter demonstration system was designed. In doing this, several blocks, such as a suitable modulator were needed to be studied and implemented in order to determine their interaction with the actual offset-PLL.

6.3.1 Modulator interface

As described earlier, the offset-PLL requires an intermediate frequency to lock to. The suggested design uses an intermediate frequency of 2.4 MHz, but any frequency in the range of approximately 0.5 MHz to 10 MHz can be used.

The choice of intermediate frequency is often heavily restricted by the architecture providing the signal, the chosen modulation scheme and by the data rate.

The intermediate frequency can be generated by:

- A digital signal processor.
- A ROM based modulator.
- An analog modulator.

The most common way to generate a low intermediate frequency is by a signal processor calculating the waveform in real time. This is a very flexible solution since the system is able to change modulation parameters while the system is online. A drawback of real time waveform generation is the heavy computational load and thereby an increased system cost and power consumption.

If however the system is to be used with fixed modulation parameters *(modulation scheme, data rate, et.c.)* a better solution is to use a ROM based modulator. This modulator relies on pre-calculated waveforms stored in a memory bank.

The waveforms stored in the memory are calculated so that the final modulated waveform is created by joining segments of the ROM content. This reduces the memory size and the implementation cost. The block diagram of such a modulator is presented in figure 6.2.

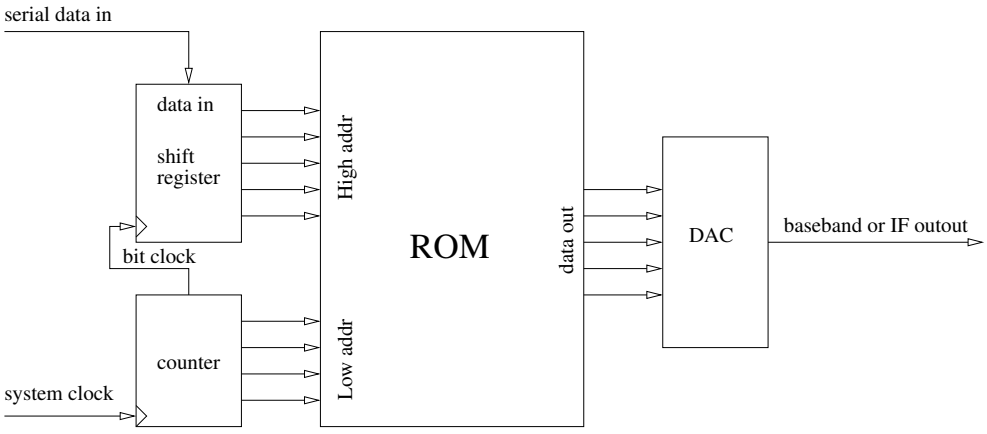

Figure 6.2: Proposed ROM based modulator for GMSK/GFSK

Gaussian modulation schemes such as GMSK and GFSK implies that one bit is spread in time by a gaussian function as shown in figure 6.3. In order to accommodate for this time-spread the modulator must keep track of what data has been sent and which bits are going to be sent in the near future.

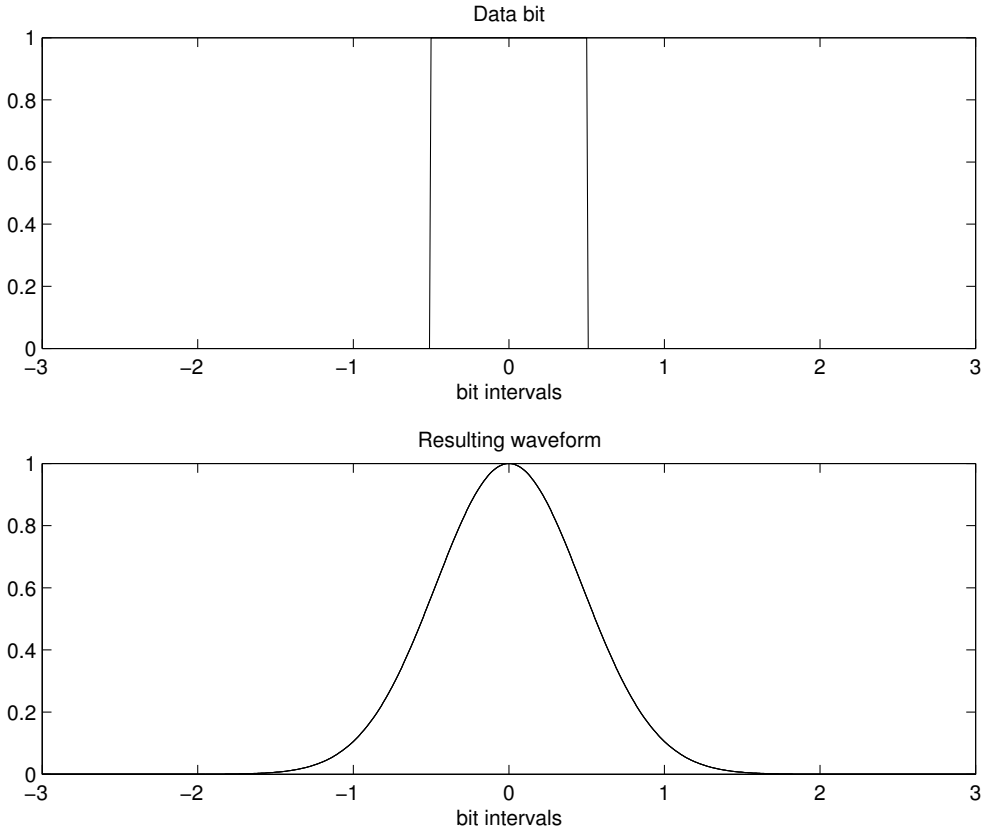

Figure 6.3: Waveforms in a gaussian modulator

The modulator consists of a large ROM containing a pre-filtered waveform and a shift register to accommodate the memory effect.

The modulator was implemented in Matlab and the ROM content was generated, but due to time constraints in this project, the modulator ROM and FPGA were unfortunately not included on the test board.

As stated before, the offset-PLL can use any intermediate frequency in the range of about 0.5 MHz to 10 MHz. However, the modulator imposes limits on the choice of intermediate frequency.

However the intermediate frequency must fulfill the following basic requirements:

- The intermediate frequency must be an integer multiple of the symbol rate.
- The intermediate frequency must be an integer multiple of the sample rate.

The requirements stated above ensures that there is an integer number of samples per data bit, and an integer number of samples per intermediate frequency period which is one requirement on the ROM based modulator.

In the next section the voltage controlled oscillator is studied among other macro blocks used in this demonstrator design.

6.4 Voltage controlled oscillator

The voltage controlled oscillator is the most important component of the offset-PLL since its performance will limit the whole system's performance.

One of the key parameters of the voltage controlled oscillator is the phase noise performance. Phase noise is defined as power/Hz at a certain offset from the carrier frequency. Figure 6.4 illustrates the phase noise.

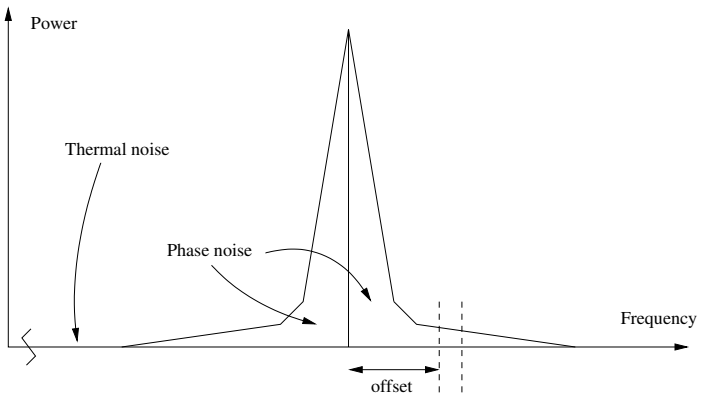

Figure 6.4: Phase noise in an oscillator

As stated before, one of the greatest benefits of the offset-PLL is the fact that the output signal is not up-converted by using mixers. Besides avoiding spurs in the system, this allows the use of high power local oscillators.

Additionally by using high power oscillators the phase noise can be reduced due to higher voltages in the oscillator. By raising the voltages in the oscillator, the signal-to-noise ratio can be improved.

When the demonstrator was designed, an oscillator with the following performance was required:

- Frequency range 108-137 MHz.

- Two different control voltages. One coarse tuning voltage, and one fine tuning voltage.
- Coarse tuning, K_{coarse}: 1.5 MHz/Volt.
- Fine tuning, K_{fine}: 200 kHz/Volt.
- Phase noise: 150 dBc/Hz at 100 kHz offset.

6.5 Loop filter

Another critical component of the offset-PLL is the loop filter. The loop filter consists of the channel filter and the low pass filter in Figure 6.1.

The magnitude and phase response of this filter is important to both prevent oscillations in the feedback loop and to prevent out of channel frequencies to modulate the voltage controlled oscillator.

As usual, good design practice must be undertaken in the loop filter design in order to achieve a good result. An improper feedback loop can potentially render the system unstable and prevent locking under certain conditions.

The loop filter will determine the usable modulation bandwidth of the offset-PLL, and ensure that the spectrum in adjacent channels is below required limits.

The filter must meet the following requirements.

- Modulation passband.
- Provide enough phase margin in the closed loop.

It is very important that the channel filter has a low group delay. Extensive group delay can make the feedback loop unstable.

The designed filter characteristics are presented in Figure 6.5.

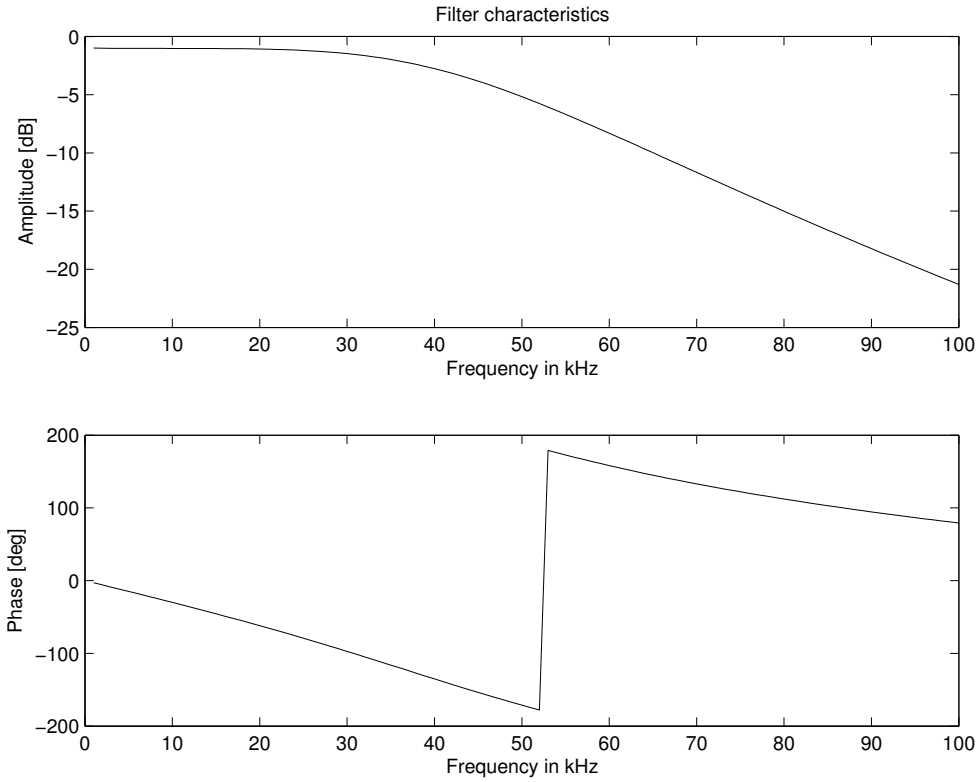

Figure 6.5: Loop filter characteristics

6.6 Integrator

Because the signal from the phase detector is proportional to the phase error, the phase error signal must be integrated in order to form a control voltage to the VCO since its output frequency is proportional to the control voltage. The integrator will cancel static or slow changing phase errors.

According to Section 5.1.1 the filtered baseband signal will be:

$$V_{phase} = \underbrace{\cos\left(\Phi_{ref} - \Phi_{fb}\right)}_{baseband}$$

The control voltage can be derived by recognizing the following relation. $\omega = \int \Phi dt$.

This yields:

$$V_{control} = \int V_{phase} dt$$

The implementation of the analog integrator is described by figure 6.6.

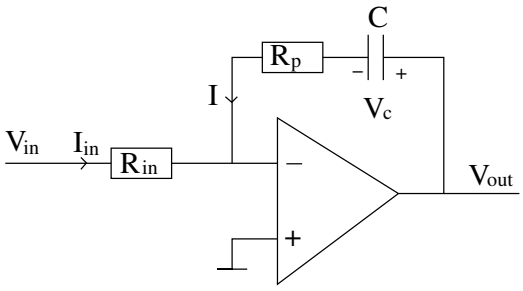

Figure 6.6: Integrator

The current through a capacitor is derived from:

$$Q = C \cdot V$$
$$I = \frac{dQ}{dt} = \frac{dC \cdot V}{dt}$$

Where Q is the charge in the capacitor, C the capacitance and V the voltage over the capacitor.

In order to be able to provide stability to the system the integrator also contain a proportional term, P in the expression below.

The output voltage is derived:

$$I_{in} = V_{in}/R_{in}$$
$$V_{out} = V_c + I \cdot R_p$$
$$I = \frac{d}{dt}(V_c \cdot C) \Rightarrow V_c \cdot C = \int I dt$$
$$V_{out} = \frac{1}{C}\int I dt + I \cdot R_p$$
$$I = -I_{in} = -V_{in}/R_{in}$$
$$V_{out} = \frac{1}{C}\int I dt + I \cdot R_p$$
$$V_{out} = \underbrace{-\frac{1}{C \cdot R_{in}}\int V_{in} dt}_{I} \underbrace{- V_{in}\frac{R_p}{R_{in}}}_{P}$$

The most important parameter in this block is the gain of the integrator which is determined by the following expression: $\frac{1}{C \cdot R_{in}}$.

The integrator gain changes the overall loop gain and can be adjusted by either changing R_{in} or C.

To determine the loop gain the following parameters must be known:

- The gain[1] of the voltage controlled oscillator.
- The conversion gain of the analog phase detector *(mixer)*.
- The passband attenuation of the loop filter.
- The integrator gain.

The value of these components can be determined by measuring the parameters listed above on the demonstrator board.

The output voltage from the analog phase detector is presented in Figure 6.7.

[1] [Hz/volt]

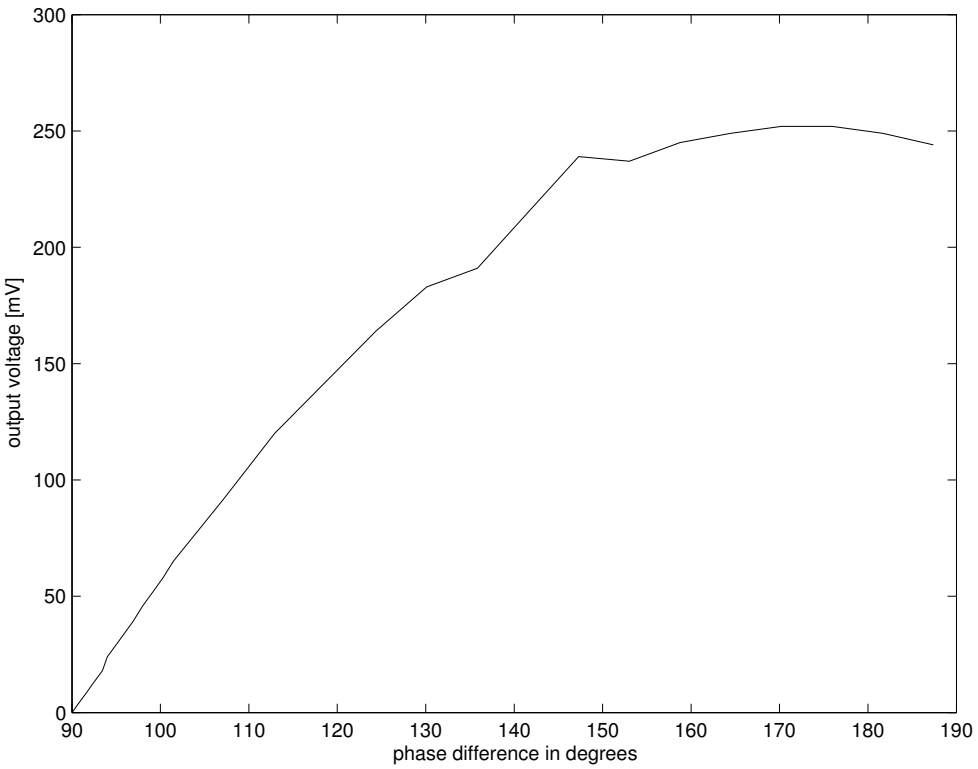

Figure 6.7: Measured output voltage from the analog phase detector

6.7 Supervision and control

Maintaining the function of the offset-PLL requires rigid control and supervision. To achieve this aim, the offset-PLL must continuously be monitored by a microcontroller to ensure that the integrator does not saturate and to ensure that the DC component of the integrator voltage is centered around zero.

The microcontroller is also responsible for handling the large frequency errors that will be the result of frequency hopping or channel selection. The main loop will not always be able to bring the offset-PLL to lock if the error frequency is larger than the bandwidth of the loop filter.

To be able to supervise the loop, the microcontroller has a conventional phase-frequency detector connected to one of its ports. This PFD is simultaneously used as a frequency detector and phase detector. By measuring the voltage from both the phase comparator, and the frequency detector the microcontroller can determine the lock state in the main loop.

6.8 Locking procedure

When the microcontroller receives a frequency change command from the host, the program uses a look-up table to find the value of the coarse tuning voltage. Before the microcontroller changes the DAC to reflect this new value, the table value is corrected for the actual fine tuning voltage measured at the integrator output. During normal operation the integrator is supposed to work around zero. If the integrator voltage is non-zero, the table value is corrected to reflect this change.

In this way the microcontroller can maintain a fresh frequency look-up table even if the hardware parameters change by temperature changes and ageing of oscillator components.

The microcontroller must continuously monitor the integrator and the digital phase and frequency detector in order to verify the lock status.

If the loop fails to lock within a specified time, the microcontroller must correct its coarse tuning value depending on the status of the digital phase detector.

However, one problem of analog phase detectors is that the microcontroller does not know in which direction it should change the coarse tuning voltage if the phase error is large.

7

Demonstrator hardware layout

This chapter describes the printed circuit board of the demonstrator. The printed circuit board was designed by the author using Mentor Graphics Expedition PCB tools.

7.1 PCB layout considerations

The layout of the printed circuit board is shown in figure 7.1.

Special care must be taken during layout of circuit boards used for RF circuits. Due to the strict output spectrum requirements it is very important to prevent noise from the digital circuits or the power supply to reach the modulator. This is accomplished in the following way:

- Use ground planes to isolate control and power supply traces on the circuit board.
- Cut the ground planes between analog and digital circuits to avoid circulating RF currents induced by bus activity or similar.
- Use separate power supplies or regulators to all separate blocks.
- Filter the control signals and power supply between sensitive blocks.
- Shield sensitive areas by shield boxes.

The demonstrator board has four layers where two of the layers are dedicated ground planes. The remaining layers are used to route power and control signals between the various blocks. During the lay out of the board, as short as possible sections on the remaining layers are routed in order to be able to use them as extra ground planes.

In order to isolate the RF section of the board, a cut was made trough all ground planes between the controller section and the offset-PLL. This cut is clearly visible in the photograph B.1.

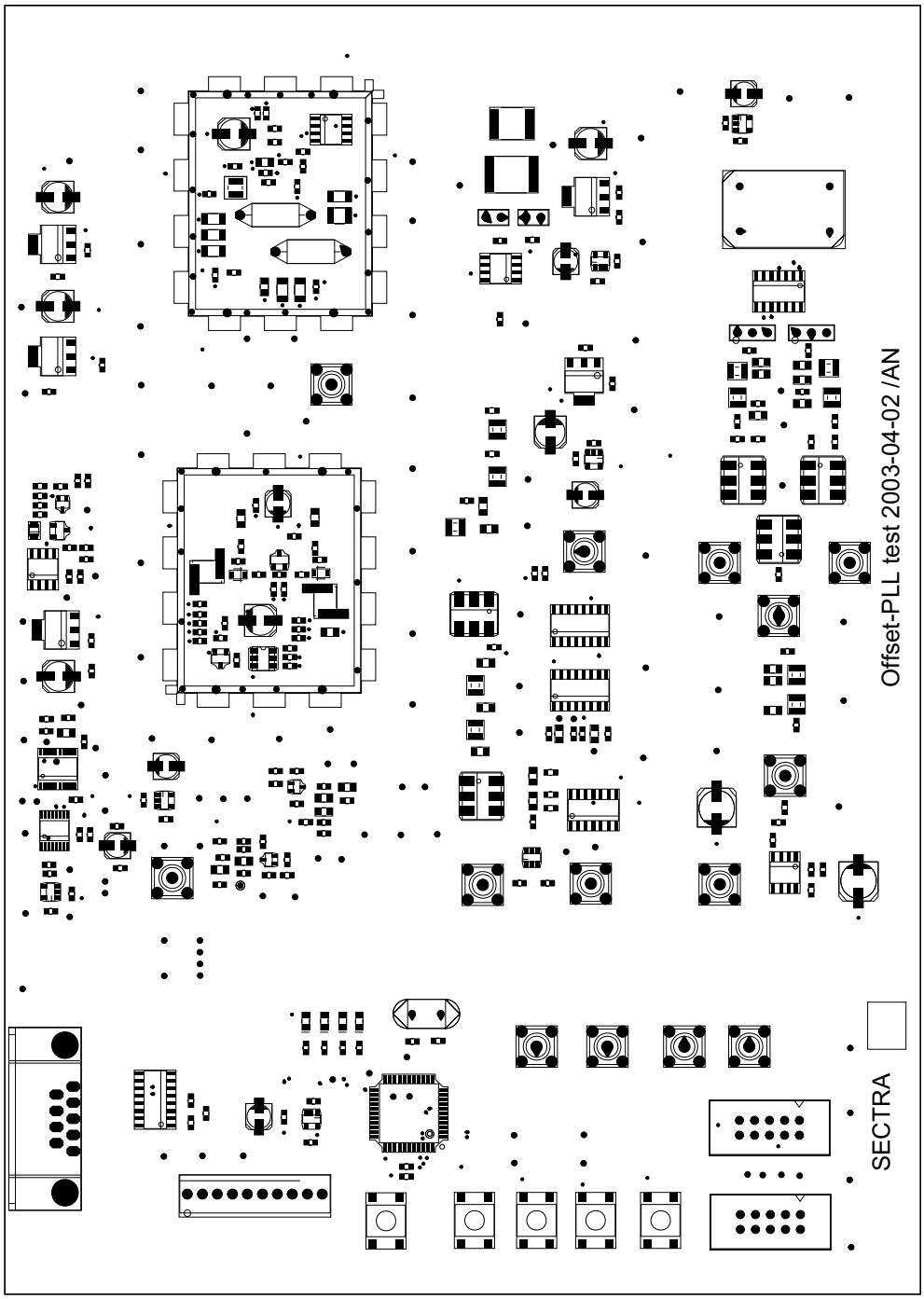

Figure 7.1: The demonstrator board

In photograph B.1, the ground plane voids in the oscillator and baseband filter cavity are visible. These voids are necessary in order to avoid parasitic oscillations in the oscillator and amplifier.

A common mistake in RF circuit board layout is the misuse of ground planes on component layer. If ground planes are mal-placed in for example an oscillator circuit or in amplifier circuits they can give rise to parasitic oscillations in active components.

These parasitic oscillations usually occur under transistors in oscillators and amplifiers. In unfortunate cases small wires of the ground plane form an inductor which provides feedback to the active element and then creates a parasitic oscillator. This design hazard is described by figure 7.2.

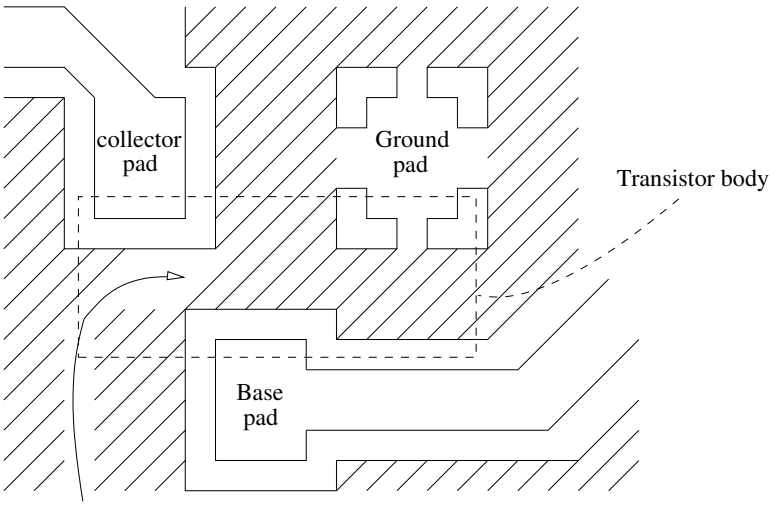

Figure 7.2: Parasitic oscillation design hazard

Usually these oscillations are hard to discover since they often occur at very high frequencies, about 4-10 GHz.

7.2 Measurement setup

The following test setup was used during the testing of the offset-PLL.

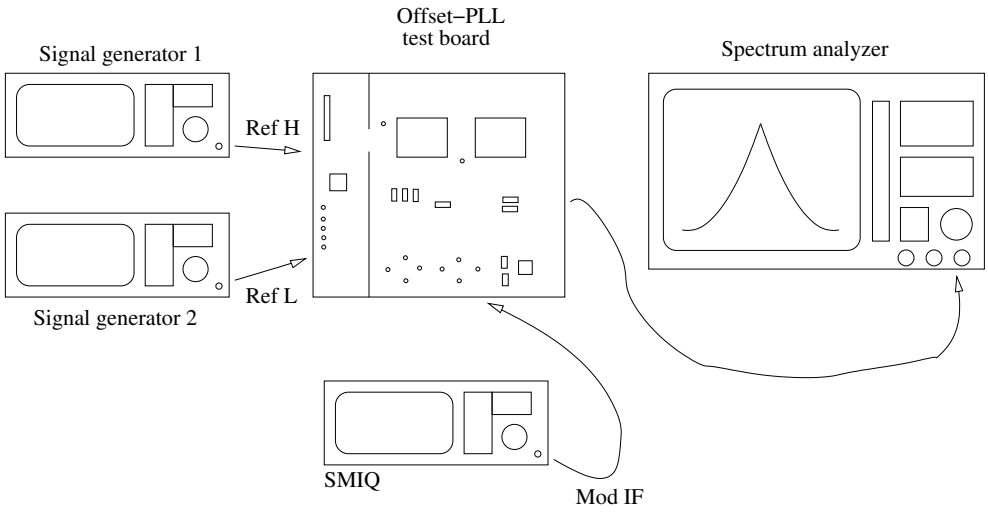

Figure 7.3: Measurement setup

The test setup seen in figure 7.3 uses:

- Two Hewlett & Packard RF signal generators for reference frequency generation.
- One SMIQ I/Q RF signal generator from Rhode & Schwarz. This signal generator has the capability to generate complete frames of data modulated by almost every modulation scheme.
- The FSEB spectrum and vector analyzer from Rhode & Schwarz.

A picture of the measurement setup is shown in figure B.2.

Signal generator 1 and 2 in figure 7.3 were used as reference frequency generators and the SMIQ signal generator was used as modulation source.

The output is analyzed by the spectrum analyzer. The normal analysis mode displays frequency on one axis and power on the other axis, whereas the demodulator mode displays frequency on one axis and time on the other axis. This feature is very useful in measuring and observing the lock procedure.

Due to time constraints, the full performance of the offset-PLL was not measured and included in this thesis. Only the lock behavior and output spectrum were studied.

It would be interesting to measure:

- The behavior of the feedback loop if the up-converter were modulated with a signal close to the pass-bandwidth of the channel filter.
- The lock time depending on which frequency steps were taken.
- The phase noise of the oscillator.

8

Results

8.1 Results

The goal of this final year project has been to develop an understanding of the different up-conversion techniques available today, and then investigate the practical problems encountered in an offset-PLL design by implementation.

In the following section several problems encountered during the implementation of an offset-PLL are presented. For the problems either a complete solution or an idea of how to solve them are given.

8.2 Problems encountered and their solutions

The following problems were encountered during the design and testing of the demonstrator offset-PLL.

8.2.1 Loop stability

One severe potential problem in all feedback systems is the problem of stability. In the case of an offset-PLL loop instability will create unwanted modulation as seen in figure 8.1. The instability of the control loop is creating a modulation of approximately 70 kHz, as seen in the previously referenced picture.

This instability is usually the result of improper loop filter design or by too much loop gain. However, the designer must also take appropriate actions in order to suppress oscillations induced by the software controlled compensation loop.

The solution to these problems is to make a complete control theory model of the system as early as possible in the design process.

Control theory analysis of the model can together with known design parameters provide designers a good start in order to make the system stable and optimize its performance.

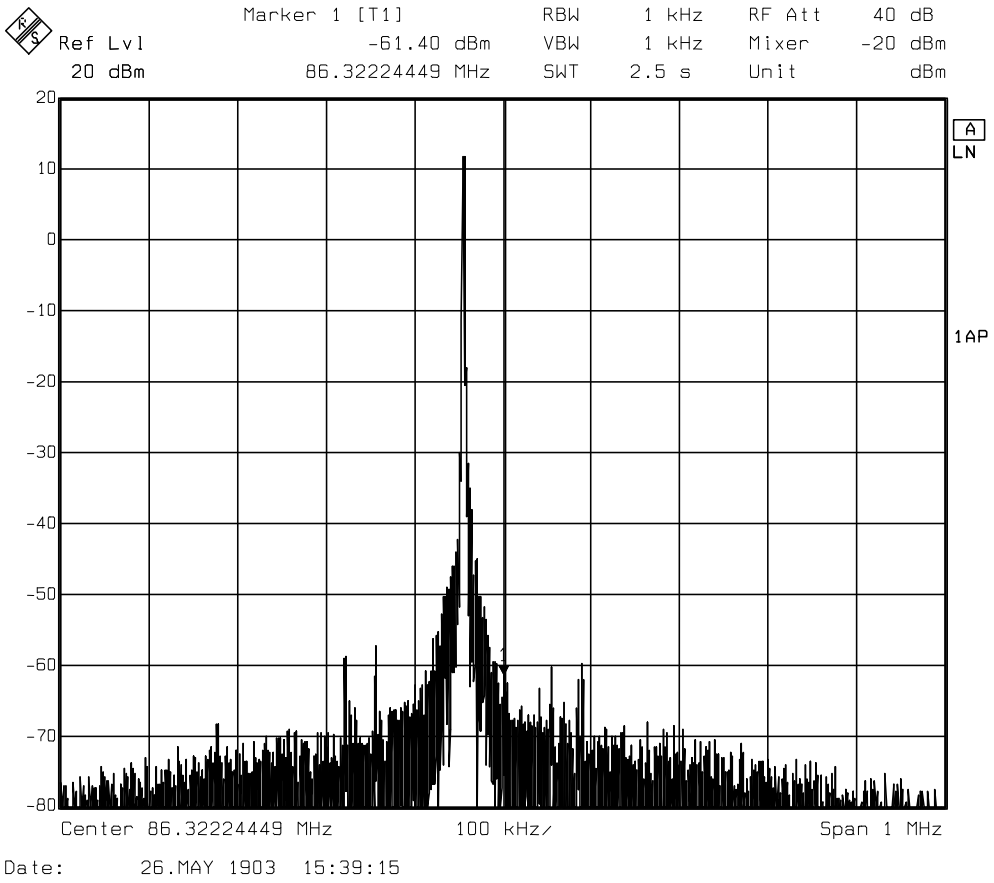

Figure 8.1: The result of loop instability

The optimum performance is achieved when the system is critically damped, and with a software controlled feedback loop, the design can be self-calibrating and thus achieve full performance during its service life regardless of component ageing.

8.2.2 Image frequency

The hardware must assure that the offset-PLL always locks to the right image of the reference frequency. This problem is illustrated by the example below.

`Example:` Let the offset oscillator run at 120 MHz. Then the phase detector cannot determine the difference between an VCO frequency of 122.4 MHz or 117.6 MHz.

This is due to $\Omega_{VCO} - \Omega_{offset}$ and $\Omega_{offset} - \Omega_{VCO}$ will both produce a 2.4 MHz intermediate feedback frequency.

The solution to this problem is to let the software control the coarse tuning in such a narrow band that the integrator cannot lock to the wrong image of the reference. This can also be accomplished by decreasing the tuning range of the fine-tune input on the voltage controlled oscillator.

This clearly indicates the need of a supervision frequency counter operating on the reference input and the created signal.

8.2.3 Locking time

The locking time of an offset-PLL is often longer than on a conventional PLL design. This is mainly because the offset-PLL must achieve lock on its reference oscillator and then achieve lock in the main loop. This can be avoided by using a DDS as a reference oscillator. This direct digital synthesizer can use fewer bits than a DDS replacing the complete up-converter since its output is down-converted and filtered by the channel filter.

Another solution is to change the software control algorithms to better control the VCO instead of instantaneously changing the frequency and coarse tuning setting.

8.2.4 Difficulties to calculate loop gain

The main problem during the offset-PLL design is to estimate or calculate the gain of all components in the control loop since many parameters are unknown or dependent on certain component choices. This problem is closely related to the problem of loop instability and long locking time.

Unfortunately there is no easy solution to this problem since each design must be analyzed individually. The straight forward approach is to do measurements on a prototype of the final up-converter and then change component values in the design.

8.2.5 Integrator reset

During the practical work the need of being able to reset the integrator was discovered. Without this possibility the system can be stuck in one of the extremes of the integrator. The microcontroller can however solve this by slowly change its coarse tuning value and thereby force the offset-PLL to lock and then slowly move the integrator back to its zero position. This can be useful during lab work, but loosing lock is devastating under normal conditions.

By being able to reset the integrator, the software can recover from a failure much quicker.

8.3 Modifications to the proposed design

In a future offset-PLL design the following issuses would be changed or needed to be included:

- Either a frequency counter or a phase and frequency detector on the reference input and VCO output.
- Means to reset the integrator.
- A variable gain amplifier in the feedback loop.
- A better supervision phase and frequency detector.

9

Conclusions

9.1 Conclusions

The offset-PLL is an excellent up-converter and its drawbacks of long locking time and complex architecture are more than enough compensated by its advantages such as spurious free up-conversion and the ability to allow the use of high power oscillators.

The offset-PLL is a complex architecture and requires a higher design effort than using a regular approach like superheterodyne up-conversion. If the designer takes the problems discovered during the creation of the demonstrator into account, the design will likely be successful and on time.

This final year work has proposed a design and proven the concept and validated the functionality of the proposed design.

9.2 Future architectures

In the future the use of offset-PLLs are expected to grow increasingly due to the higher spectrum requirements and the need to cover larger and larger bands. The trend is drifting towards software defined radio. A software defined radio must be able to cope with large operating bands while not violating any spectrum requirement.

Another future scenario is the replacement of analog architectures with DDS systems. This may be possible in a near future due the ever improving performance of the DDS chips available.

The greatest benefit of direct digital synthesis is the fact that the development can be expected to follow Moores Law, and thus will double the maximum frequency or reduce the noise by a factor of two every 18th month.

9.3 Future work

A natural continuation of this work would be to address the following issues:

- Develop a better control theory model of the offset-PLL.
- Improve locking time by changing software algorithms.
- Reduce phase noise by the use of a high power oscillator.
- Integrate a digital signal processor for loop control and intermediate frequency generation.
- Complete the measurements proposed earlier in the thesis.

A

Abbreviations

- ADC: Analog to Digital Converter.
- DAC: Digital to Analog Converter.
- FSK: Frequency shift keying.
- GMSK: Gaussian minimum shift keying.
- IF: Intermediate frequency.
- M-PSK: M-ary Phase shift keying.
- PA: Power amplifier.
- PCB: Printed circuit board.
- PD: Phase Detector
- PFD: Phase-Frequency Detector.
- PLL: Phase Locked Loop.
- RF: Radio frequency.
- TDMA: Time division multiple access.
- VCO: Voltage controlled oscillator.

B

Pictures

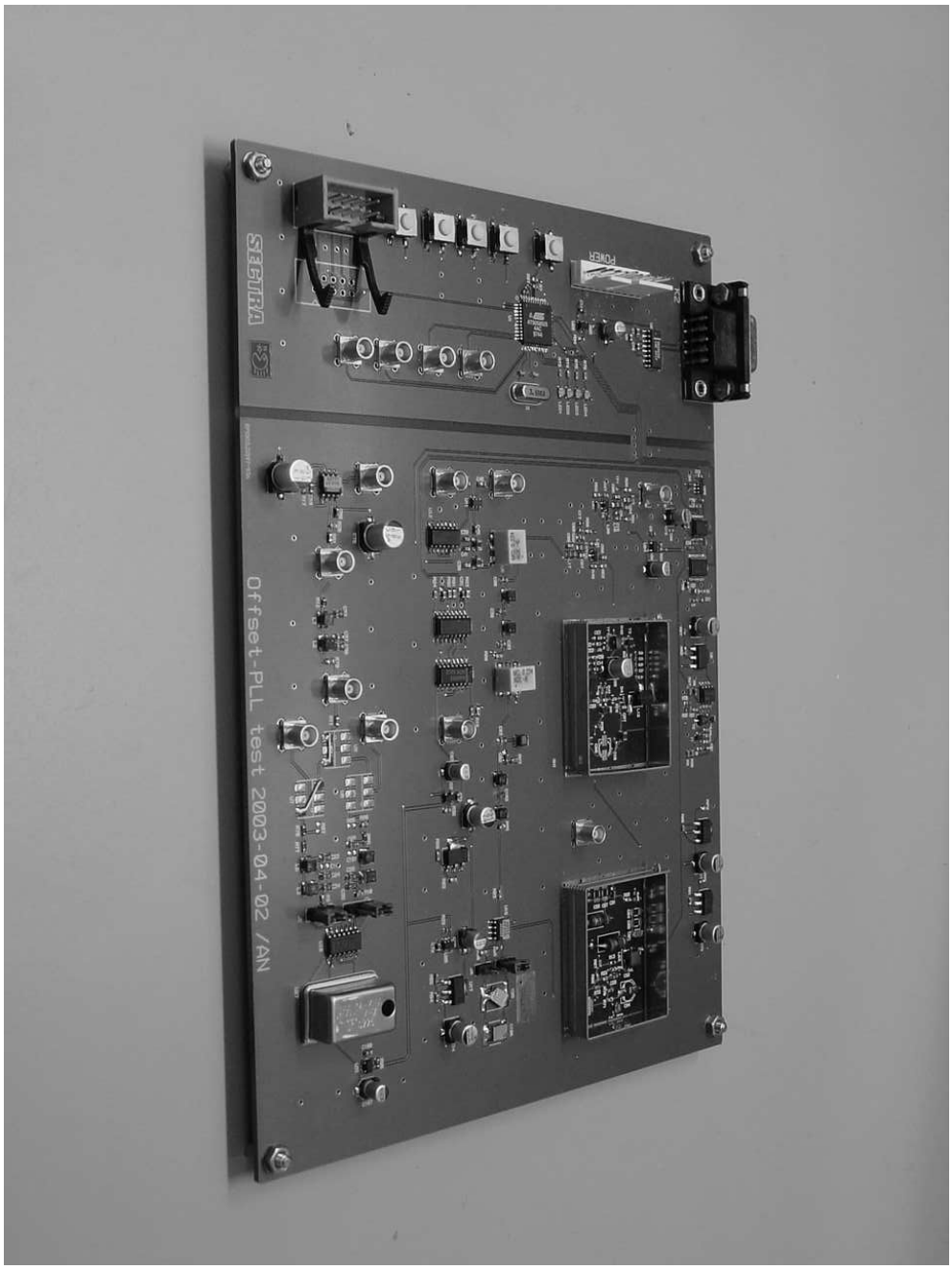

Figure B.1: The complete demonstrator board

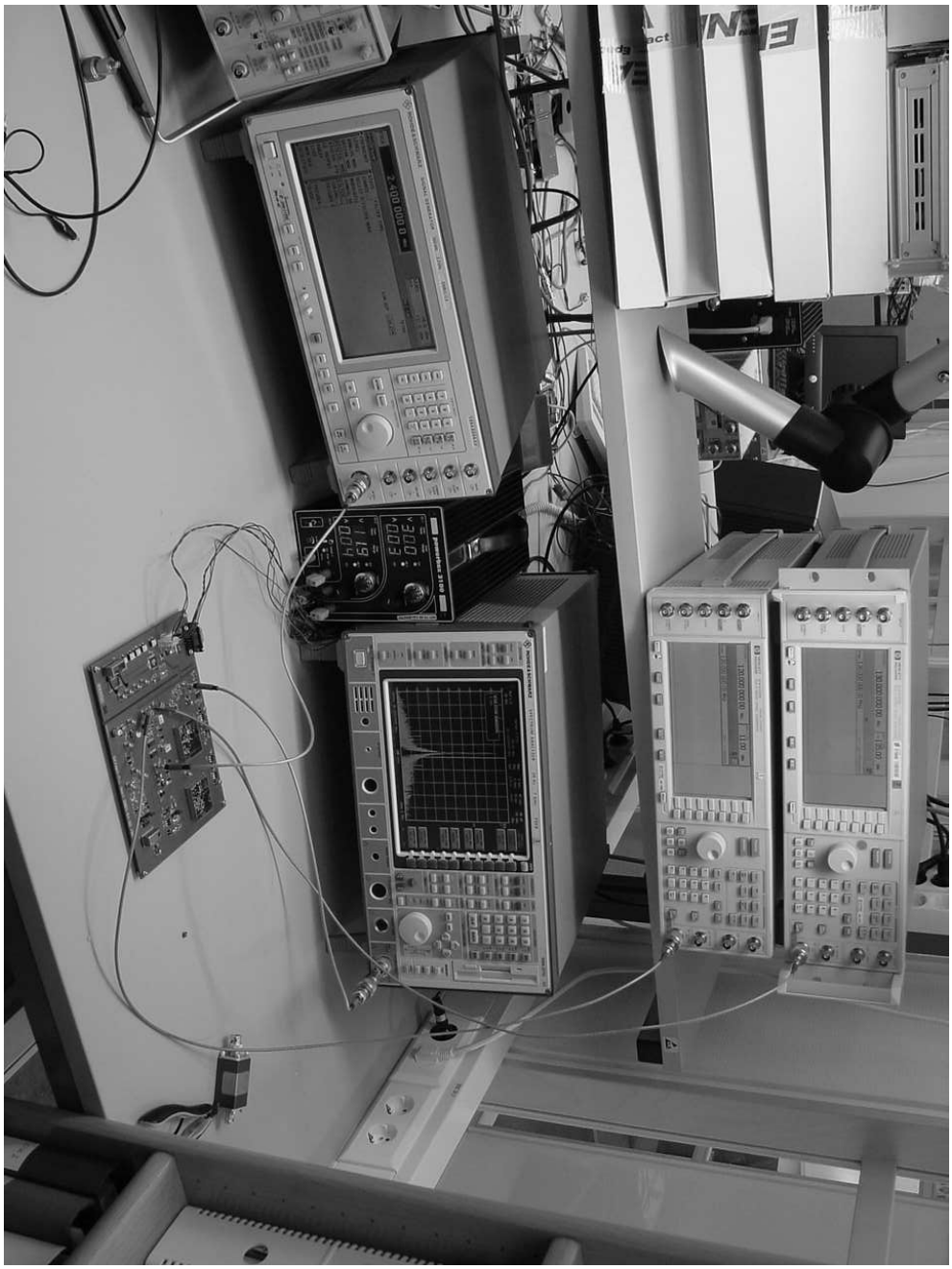

Figure B.2: The measurement setup

References

[1] Simon Haykin: Digital Communications, John Wiley & Sons; (February 1988)

[2] Bosco Leung: VLSI for Wireless Communication, Prentice Hall; 1st edition (August 15, 2002)

[3] Chris Bowick: RF Circuit Design, Newnes; Reprint edition (March 1997)

[4] Steve C. Cripps: RF Power Amplifiers for Wireless Communications; Artech House; (April 1999)

[5] Peter Vizmuller: RF Design Guide: Systems, Circuits, and Equations; Artech House; Book and Disk edition (April 1995)

Copyright

Svenska

English