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RF Synthesis without Inductors

A dissertation submitted in partial satisfaction

of the requirements for the degree

Doctor of Philosophy in Electrical Engineering

By

Long Kong

2016

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2016

ABSTRACT OF THE DISSERTATION

RF Synthesis without Inductors

by

Long Kong

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2016

Professor Behzad Razavi, Chair

Recent developments in RF receiver design have eliminated all on-chip inductors except for that used in the local oscillator. This dissertation addresses the "last inductor" problem and proposes both integer-N and fractional-N synthesizer architectures that achieve a phase noise and figure of merit (FOM) comparable to those of LC-VCO-based realizations.

A new wideband integer-N synthesizer is introduced to sufficiently suppress the ring's phase noise. It employs an exclusive-OR (XOR) phase detector and a master-slave sampling filter (MSSF) to achieve a lock range of 2-3 GHz, a loop bandwidth equal to one half of the reference frequency, and a locked phase noise of -114 dBc/Hz up to 10-MHz offset with a 3-stage ring oscillator. Realized in 45-nm CMOS technology, the design uses a harmonic trap to suppress reference sidebands to less than -65 dBc while consuming 4 mW.

The wideband architecture has been successfully extended to a fractional-N loop as well. A ring-oscillator-based cascaded synthesizer incorporates a digital synchronous delay line and an analog noise trap to suppress the quantization noise of the ΣΔ modulator. Realized in 45-nm CMOS technology, the synthesizer exhibits an in-band phase noise of -109 dBc/Hz and an integrated jitter of 1.68 ps_{rms} at 2.4 GHz with a power consumption of 6.4 mW.

The dissertation of Long Kong is approved.

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2016

DEDICATION

To my lovely parents

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ACKNOWLEDGEMENTS

I would like to thank my advisor, Professor Behzad Razavi, for his patience, encouragement and guidance. I had a hard time at the beginning of my Ph.D. research because I was in the analog-to-digital converter field in my Master's study. Professor helped me to build knowledge in this new field gradually and provided me very useful ideas when I came across a technical problem. I benefit a lot from his knee insight and understanding of circuits. Hardworking, passionate and creative as he is, he sets an excellent example for me in my future career.

I would also like to thank my friends and colleagues. When I first came to UCLA, Hao Wu helped me to set up tools from scratch. After joining Communication Circuits Lab, Hegong Wei, Joung Won Park, Joseph Mathew gave me very good suggestions on my research. My dear friend, Ming-Shuan Chen, helped me a lot on digital circuit design.

It is also my great pleasure to do summer intern at Broadcom, Irvine. As an analog modeling engineer, I spent a wonderful time at Jacob Rael's group. He recommended me to talk to a lot of experienced engineers in the company and resolved my concern of the career choice. He is knowledgeable and nice, making me feel like being in the family when I was in his group.

I was blessed to have these friends around me. Xiao Wang, Dihang Yang, Wenlong Jiang,

Yinan Dong, Abishek Manian and Xuan Dai helped me a lot throughout my study and life at UCLA. Together with them, I had a wonderful time.

Finally, I would like to give my greatest gratitude to my family and my girlfriend. Without their support, I cannot even move close to my goal. They are always with me at hard times and give me confidence to overcome all obstacles.

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PUBLICATIONS

Long Kong and Behzad Razavi, "A 2.4GHz 4mW Inductorless RF Synthesizer", *Digest of International Solid-State Circuits Conference*, pp. 450-451, Feb. 2015.

Joseph Palackal Mathew, Long Kong and Behzad Razavi, "A 12-Bit 200-MS/s 3.4-mW CMOS ADC with 0.85-V Supply", *IEEE Symposium on VLSI Circuits*, pp. 66-67, June 2015.

Long Kong and Behzad Razavi, "A 2.4 GHz 4 mW Integer-N Inductorless RF Synthesizer", *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 626-635, Mar. 2016.

CHAPTER 1

Introduction

Wireless devices use radio-frequency (RF) chipsets for connectivity. One critical part of these chips is the RF frontend, namely, transceivers. The transmitter has to deliver a large power so that it can reach the user at a long distance away. The receiver has to be sensitive enough to reconstruct the signal faithfully among various interferers form other users. Shown in Figure 1.1 is a simplified transceiver diagram.

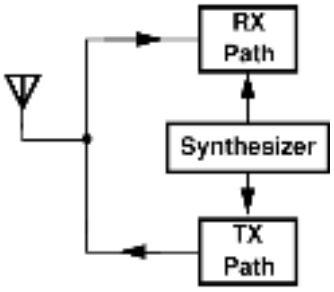

Fig. 1.1. RF transceiver diagram.

Besides the transceiver chain, a key component for both transmitter (TX) and receiver (RX) is the phase-locked frequency synthesizer. It provides an accurate carrier frequency for different channels with low phase noise and spurious tones. The carrier frequency must be extremely accurate to avoid the leakage from one user to other user's channel. The noise must be low enough to minimize signal corruption. In practice, since the undesired signal (blocker) can have a

much larger power than the desired one, the down-converted blocker can directly corrupt the desired signal when the carrier is not an ideal tone. This is called the "reciprocal mixing" and is illustrated in Figure 1.2.

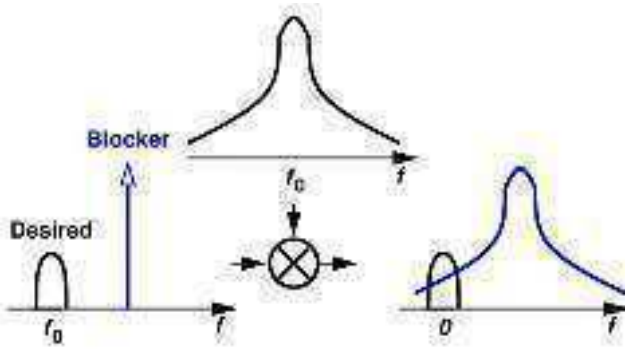

Fig. 1.2. Illustration of reciprocal mixing.

Considering all these issues, RF applications require a low-noise and low-spur frequency synthesizer. Of course, the power consumption must be acceptably low for a long battery life. This makes the RF synthesizer design a challenge task.

1.1 Motivation

With the scaling of semiconductor devices, the RF chip size has not shrunk as much as the digital baseband. This is primarily because RF circuits employ a number of spiral inductors. The situation is even worse in today's multi-band multi-mode RF transceivers. Since numerous inductors must be used, the die area of the RF front end becomes larger than that of the digital

baseband. Therefore, a great deal of focus has been placed on inductorless RF front-end design. In particular, circuits such as low-noise amplifiers and power amplifier drivers can now be realized without inductors. Unfortunately, the inductorless RF frequency synthesizer has not been invented yet in either industry or academic fields.

The need for LC oscillators in RF synthesis has been solidified by various studies revealing that the white-noise-induced phase noise of ring oscillators trades primarily with the power consumption [1], [2] and is relatively independent of the number of stages. However, ring oscillators do present compelling advantages: (1) they occupy a smaller area and can be readily placed within a transceiver layout with less serious concerns regarding proximity effects, (2) they entail much less coupling to and from other circuits, (3) they achieve a wider tuning range and can be multiplexed to cover decades of frequencies, and (4) they readily generate multiple phases.

That the phase noise of ring oscillators is difficult to improve at the circuit level forces us to higher levels of abstraction. Figure 1.3 shows an example of processing the signals in an RF receiver so as to suppress the phase noise in reciprocal mixing.

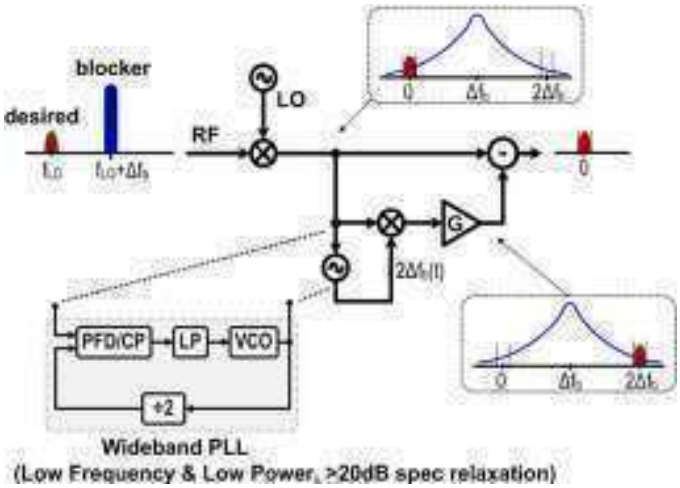

Fig. 1.3. Receiver architecture of reciprocal mixing cancellation [3].

This approach, however, does not correct for the effect of phase noise on the received signal constellation and the error vector magnitude (EVM) (e.g., in the absence of a blocker). Nor is it applicable to the transmitter. It is interesting to note that (a) applications entailing significant reciprocal mixing, e.g., GSM, actually place tighter requirements on the TX phase noise, and (b) applications specifying the phase noise by the EVM, e.g., IEEE 802.11 a/b/g, impose equally stringent phase noise constraints on RX and TX. In other words, the TX phase noise is at least as critical as the RX phase noise in most systems. It is therefore desirable to seek a solution that can be applied to both.

In this dissertation, I will propose a wideband integer-N synthesizer that allows the ring oscillator to meet the 2.4-GHz phase noise requirement. A spur reduction technique together with

a calibration scheme will also be introduced to reduce the reference spur levels [4], [5]. Thereafter, the wideband architecture will be extended to the fractional-N loop. A digital delay-line-based filter and an analog noise trap will be proposed to suppress the ΣΔ quantization noise.

1.2 Thesis Organization

This dissertation consists of seven chapters. Chapter 2 reviews the fundamentals of PLLs including bandwidth, noise transfer function and tradeoffs of type-I and type-II PLLs.

Chapter 3 presents an integer-N architecture that incorporates an MSSF to achieve a bandwidth close to $f_{REF}/2$. It starts with traditional PLLs and evolves gradually to the proposed architecture. In addition, a frequency domain analysis is carried out to mathematically predict the bandwidth and phase margin. The proposed spur reduction technique and the corresponding calibration are also discussed in this chapter.

Chapter 4 shows the challenge of the wideband fractional-N synthesizer, emphasizing the difficulty of the ΣΔ quantization noise reduction. Both digital and analog noise suppression techniques are introduced to enable low-noise, wideband operation.

Chapter 5 shows the measurement results and Chapter 6 summarizes this dissertation.

CHAPTER 2

Background

This chapter provides background for the PLL design. Section 2.1 shows the transfer function for the type-I PLL and studies its basic tradeoffs and limitations. Section 2.2 calculates the transfer function for the type-II PLL and focuses on its bandwidth and stability. Based on those functions, a range of the PLL bandwidth is derived for later comparison.

2.1 Type-I PLL Basics

This section studies the basics of the type-I PLL. The small signal model and transfer function are derived in 2.1.1. The tradeoffs are discussed in 2.1.2.

2.1.1 Transfer Functions

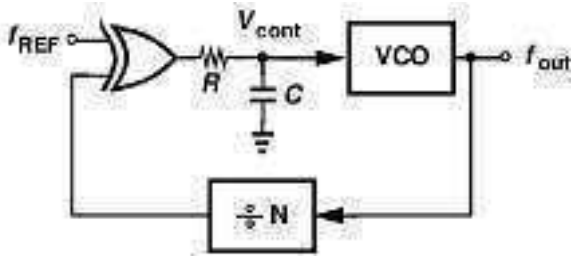

Fig. 2.1. Traditional type-I PLL.

A traditional type-I PLL is shown in Figure 2.1. It consists of an XOR gate as a phase detector (PD), a passive RC loop filter, a VCO and a feedback divider. With a phase detector gain of K_{PD} (= V_{DD}/π), a VCO gain of K_{VCO}, a low-pass corner frequency of ω_0 and a divider ratio of N, the input-output transfer function can be derived as

$$\frac{\emptyset_{out}}{\emptyset_{in}} = \frac{K_{PD}K_{VCO}\omega_0}{s^2 + \omega_0 s + \frac{K_{PD}K_{VCO}\omega_0}{N}}.$$

The VCO phase noise to output transfer function can be calculated as

$$\frac{\emptyset_{out}}{\emptyset_{VCO}} = \frac{s^2 + \omega_0 s}{s^2 + \omega_0 s + \frac{K_{PD}K_{VCO}\omega_0}{N}}.$$

To apply the damping theorem, the natural frequency ω_n and the damping factor ζ is shown below:

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}\omega_0}{N}}, \varsigma = \frac{1}{2}\sqrt{\frac{N\omega_0}{K_{PD}K_{VCO}}}. \tag{2.1}$$

2.1.2 Limitations

With the transfer functions in Section 2.1.1, we can study the tradeoff between the bandwidth and spur level. From Eq. (2.1), the bandwidth is proportional to K_{VCO} and ω_0. Since an increase on K_{VCO} results in a decrease in ζ, we have to enlarge the low-pass corner frequency to guarantee

a good settling behavior. As a result, the reference jump on V_{cont} will be large. This tradeoff limits the bandwidth of the type-I PLL.

Another disadvantage is the narrow acquisition range. Since the traditional type-I loop has only a phase detector without the frequency detection ability, the loop may fail to lock when the free-running VCO frequency is far away from the desired value. Typically, the type-I loop requires an additional frequency detection loop to help acquisition.

2.2 Type-II PLL Basics

This section studies basics of the type-II PLL and examines its limitations.

2.2.1 Transfer Functions

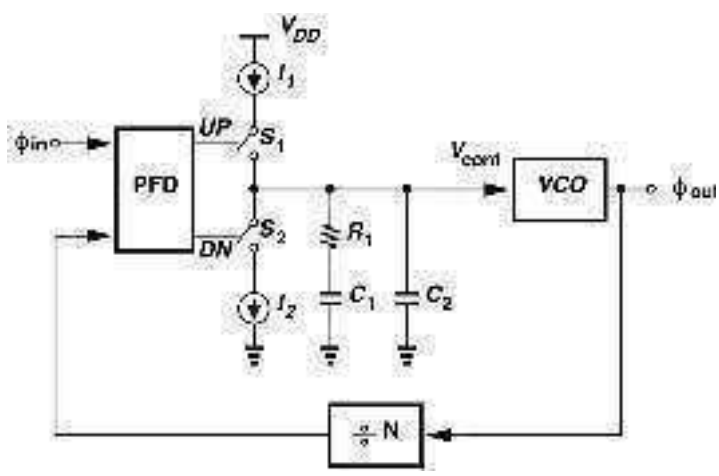

Fig. 2.2. Traditional charge-pump PLL (CPPLL) architecture.

Type-II PLL has one more integrator than type-I loop. Figure 2.2 shows the architecture of the

traditional CPPLL. The PFD generates up and down pulses to control the charge pump (CP). The CP dumps charge onto the loop filter to generate certain control voltage. If only the capacitor C_1 is used in the filter, the PLL contains two integrators and is prone to instability. The series resistor R_1 adds a left-plane zero, $-1/(R_1C_1)$, to the transfer function, thus stabilizing the loop. In practice, the mismatch in the up and down current sources causes reference jump on the control node. To reduce this jump, the capacitor C_2 is added to suppress the spur. Assume a nominal CP current of I_p and neglect the effect of capacitor C_2 at this moment, the input-output transfer function can be derived as

$$\frac{\emptyset_{out}}{\emptyset_{in}} = \frac{\frac{I_{CP}K_{VCO}}{2\pi C_1}(1 + R_1C_1s)}{s^2 + \frac{I_{CP}}{2\pi}\frac{K_{VCO}}{N}R_1s + \frac{I_{CP}K_{VCO}}{2\pi NC_1}}.$$

The VCO phase noise to output transfer function is

$$\frac{\emptyset_{out}}{\emptyset_{VCO}} = \frac{s^2}{s^2 + \frac{I_{CP}}{2\pi}\frac{K_{VCO}}{N}R_1s + \frac{I_{CP}K_{VCO}}{2\pi NC_1}}.$$

Now, the natural frequency ω_n and the damping factor ζ can be calculated as:

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi NC_1}}, \varsigma = \frac{R_1}{2}\sqrt{\frac{I_{CP}K_{VCO}C_1}{2\pi N}}.$$

2.2.2 Tradeoffs

The magnitude of the VCO phase noise transfer function is plotted in Figure 2.3. It starts with a second-order rise and becomes a first-order one when it encounters the first pole, then it remains flat after the second pole. It shows that the loop acts as a high-pass filter for the VCO noise. Hence, a wide loop bandwidth is desired.

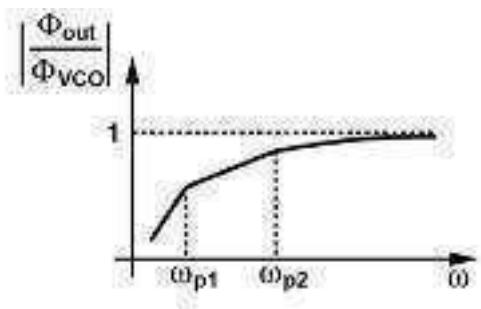

Fig. 2.3. Magnitude response of the VCO phase noise transfer function.

An increase in K_{VCO} results in a wider loop bandwidth and a better stability, this is contrary to the type-I loop. However, it does not mean the loop bandwidth can be much wider than the type-I loop. The previous calculation follows the continuous-time approximation, which is true when the loop time constant, roughly $1/(\zeta\omega_n)$, is much larger than the sampling period. If the loop bandwidth becomes larger, the voltage and current varies dramatically between two consecutive samples. Hence, the continuous-time approximation does not hold any more. At this condition, a z-domain model can be used to examine the stability. According to [6], a CPPLL typically has a loop bandwidth of less than $f_{REF}/10$. This is called the "Gardner's Limit". In the presence of CP

nonidealities, the loop bandwidth is reduced to typically $f_{REF}/20$ or less if spurs lower than -60 dBc are required [7] – [11].

2.2.3 Bandwidth Limitations

Unlike type-I PLL, which is unconditionally stable, the type-II loop does have a limited bandwidth. It is helpful to briefly review the different bandwidths encountered in PLL analysis: (a) the input-output transfer function has a certain 3-dB bandwidth, which we call the "PLL bandwidth," f_{BW}, in this paper; (b) the loop transmission has a unity-gain bandwidth, f_{UGB}, and (c) the VCO noise transfer function, a high-pass response, also has a 3-dB bandwidth, $f_{n,VCO}$. For example, a type-II PLL with a unity damping factor provides

$$2\pi f_{BW} \approx 2.5\omega_n = 2.5\sqrt{\frac{I_p K_{VCO}}{2\pi N C_1}},$$

$$2\pi f_{UGB} \approx 2.1\omega_n,$$

$$2\pi f_{n,VCO} \approx 1.55\omega_n.$$

For example, if f_{UGB} is chosen in the range of $f_{REF}/20$ to $f_{REF}/10$, then

$$0.037 f_{REF} < f_{n,VCO} < 0.074 f_{REF}. \tag{2.2}$$

As mentioned above, [7] – [11] choose a loop bandwidth less than $f_{REF}/20$, thus falling on the low

side of Eq. 2.2.

CHAPTER 3

A 2.4-GHz 4-mW Integer-N Inductorless RF Synthesizer

This chapter will propose the wideband integer-N synthesizer architecture and analyze the loop in both time domain and frequency domain.

3.1 Proposed Wideband PLL

The approach to suppressing the VCO phase noise is to develop a PLL topology that avoids Gardner's limit and, if necessary, deal with the ripple on the control voltage by additional techniques. We assume f_{REF} = 20 MHz. Let us consider a type-I PLL architecture as shown in Figure 2.1. Such a loop contains only one integrator and can, in principle, remain stable with a wide bandwidth. For example, Figure 3.1 depicts the circuit's transient behavior with $(RC)^{-1}$ = 2π(40 MHz), K_{VCO} = 1500 MHz/V, N = 120, and hence a loop bandwidth of 5.6 MHz.

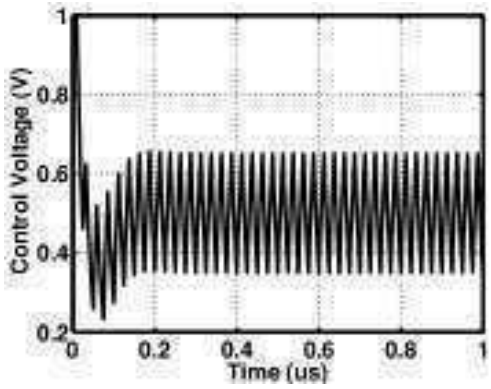

Fig. 3.1. Settling behavior of type-I PLL with bandwidth of 5.6 MHz.

Of course, since the XOR output swings from 0 to V_{DD}, the VCO experiences a large ripple. In fact, as RC is reduced, the theoretical loop bandwidth can even exceed $f_{REF}/2$, but, as plotted in Figure 3.2, the spurs eventually rise above the carrier, rendering the circuit meaningless. This PLL sustains a static phase error in proportion to the oscillator control voltage. For a V_{cont} ranging from 0 to V_{DD}, this error varies from 0 to about 180°.

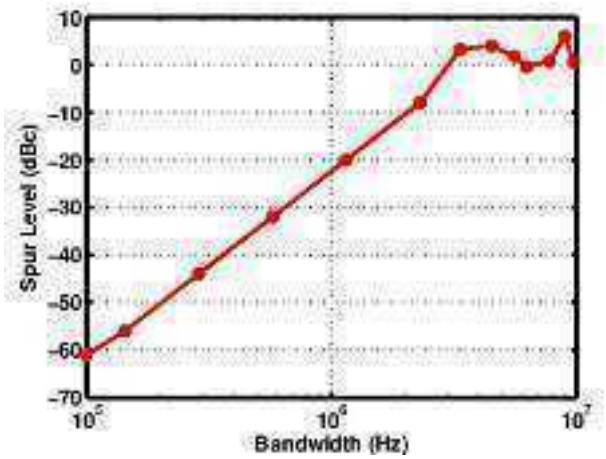

Fig. 3.2. Spur level versus bandwidth for type-I PLL.

The type-I PLL also suffers from a limited capture range. If the VCO begins with a frequency of f_1 and the XOR output at $|f_1/N-f_{REF}|$ is heavily attenuated by the filter, then the loop has no tendency to lock. In the foregoing example, $(RC)^{-1}$ must be lowered to $2\pi(0.47\ \text{MHz})$ for the output spurs to fall to -35.5 dBc, yielding a simulated capture range of about 7.4%.

3.1.1 Type-I PLL with Sampling Filter

In a manner similar to charge-pump PLLs [12], [13], we can replace the continuous-time filter in Figure 2.1 with a discrete-time implementation, aiming to isolate the VCO from the large XOR jumps. As depicted in Figure 3.3(a), we wish to select the timing between the main input and V_F such that S_0 turns on only during a "settled" level. Unfortunately, this is not possible because V_X still jumps between 0 and V_{DD}. Figure 3.3(b) shows the loop's waveforms in the locked condition, indicating that V_X varies at $2f_{REF}$ if the input has a 50% duty cycle. When V_F goes high, V_{cont} attempts to track V_X, reaching a certain level, V_1, that is necessary for the VCO to operate at Nf_{REF}.[1] That is, the loop adjusts the phase error, $\Delta\phi$, until the V_{cont} transient yields a value of V_1 at the end of one T_{REF}.

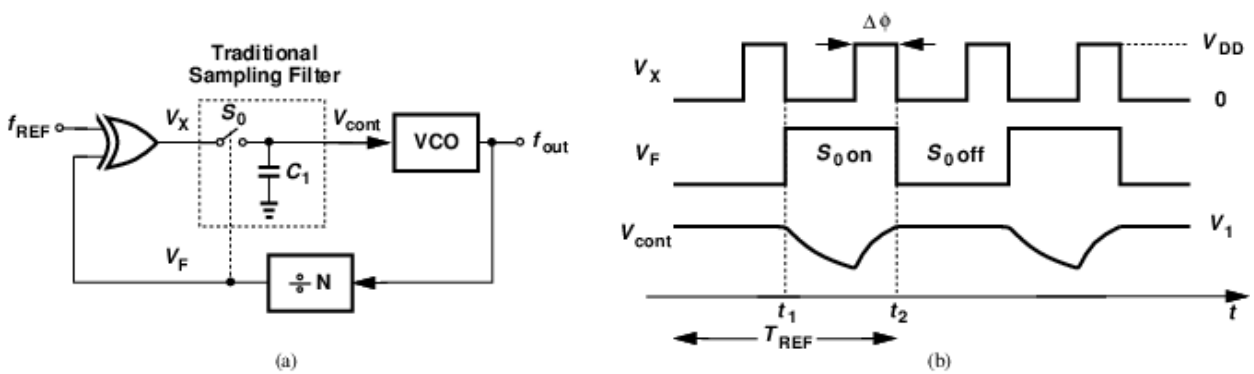

Fig. 3.3. (a) Type-I PLL with traditional sampling filter, and (b) time-domain operation.

[1] This is true only if the ripple is small.

The above technique does provide a constant voltage, V_1, for the VCO while S_0 is off. We therefore wish to modify the circuit so that the VCO does not sense the transient from t_1 to t_2. This is accomplished by inserting one more sampling network in the VCO control path [Figure 3.4(a)], with the two now operating in a master-slave manner. The divider output is converted to two nonoverlapping phases, preventing direct feedthrough from V_X to V_{cont}. We expect to observe a large ripple on C_1, similar to that in Figure 3.3(b), but a small ripple on C_2. As an example, Figure 3.4(b) shows the transient behavior with C_1 = 16 pF, C_2 = 1 pF, K_{VCO} = 280 MHz/V, and N = 120. The loop bandwidth is about 9 MHz and the loop settles in roughly 10 input cycles.

The PLL architecture employing the master-slave sampling filter (MSSF) displays several interesting and useful properties. As explained below, compared to the traditional type-I PLL, its capture range is much wider, and, in comparison to type-II PLLs, it achieves a loop bandwidth close to $f_{REF}/2$ settles faster, and avoids the difficulties in low-voltage CP design.

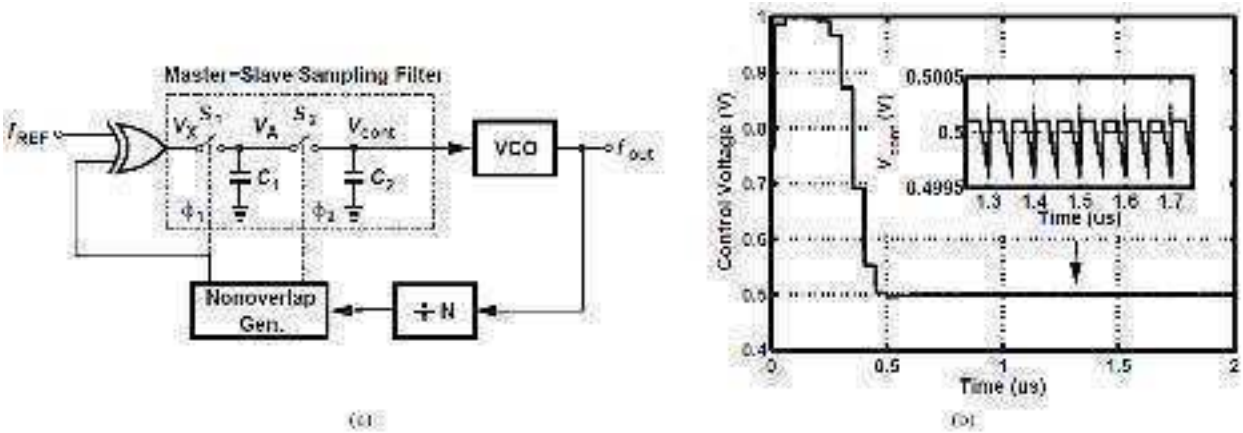

Fig. 3.4. Proposed PLL (a) architecture, and (b) settling behavior.

3.1.2 MSSF Transfer Function

As explained above, the periodic voltage jumps at V_X in Figure 3.4(a) do not reach V_{cont}, implying that the master-slave filter response has notches at the reference frequency and its harmonics. We examine this response in detail here.

As a continuous-time (CT) approximation, we can say that C_1 switches between V_X and V_{cont} periodically, thus acting as a series resistor, R_{eq}, equal to $1/(f_{CK}C_1)$, where f_{CK} denotes the sampling frequency and is equal to f_{REF} when the loop reaches the locked condition. In other words, the filter resembles a first-order section having a response given by

$$H(s) = \frac{1}{1 + R_{eq}C_2 s} = \frac{1}{1 + \frac{C_2}{C_1 f_{CK} s}}.$$

Note that this response accounts for charge sharing between C_1 and C_2, but fails to predict the harmonic notches. It is also a crude approximation if the PLL bandwidth approaches $f_{REF}/2$.

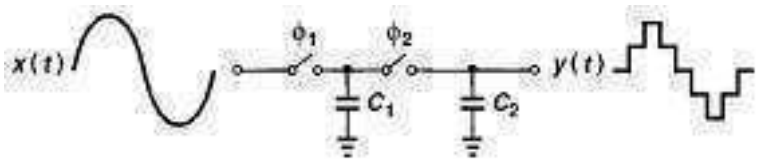

Fig. 3.5. Input and output waveforms of MSSF with zero switch resistance.

A more accurate transfer function is obtained if we consider the MSSF as a zero-order hold (ZOH) circuit. As illustrated in Figure 3.5, the circuit converts a CT input to a discrete-time output. If $C_2 << C_1$ so that charge sharing between the two capacitors can be neglected, then the ZOH output can be expressed as [14]:

$$Y(f) = e^{-j2\pi f T_{CK}/2} \frac{\sin(\pi f T_{CK})}{\pi f T_{CK}} \sum_{-\infty}^{\infty} X(f - \frac{n}{T_{CK}}).$$

For the output component of interest, n = 0 and

$$Y_0(f) = e^{-j2\pi f T_{CK}/2} \frac{\sin(\pi f T_{CK})}{\pi f T_{CK}} X(f). \tag{3.1}$$

This result, of course, predicts the notches at the harmonic of f_{CK} but disregards charge sharing.[2]

[2] A z-domain model can also be constructed but yielding less intuition in terms of closed-loop behavior.

Even though operating as a master-slave storage circuit, the proposed filter exhibits a delay of $T_{CK}/2$, rather than T_{CK}, in the PLL environment. This is because the XOR produces the phase error information twice per cycle. Illustrated in Figure 3.6, this effect can be seen by displacing the f_{REF} edges by a small amount, ΔT, and observing that V_X inherits this change from both the rising edge and the falling edge of f_{REF}. Consequently, V_A changes in about $T_{CK}/2$ seconds and is frozen thereafter. If the MSSF delay were as long as T_{CK}, the PLL would become unstable for a loop bandwidth of $f_{REF}/4$.

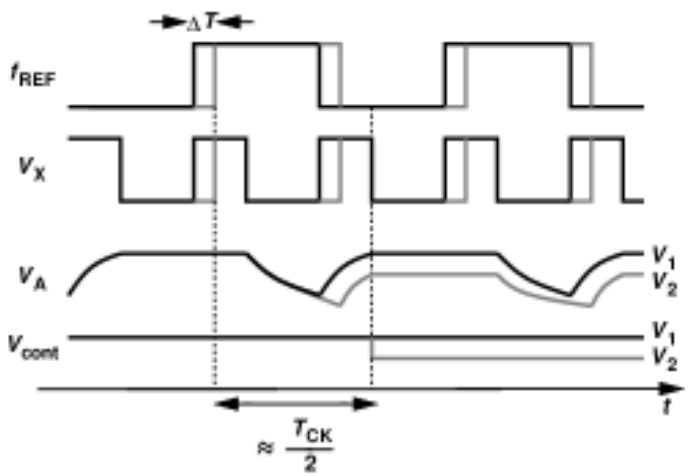

Fig. 3.6. XOR and MSSF time-domain waveforms.

Equation (3.1) is a reasonable MSSF model for our analysis and design efforts described below, especially because we will select C_2 much less than C_1, thus minimizing charge sharing and improving the ZOH approximation. However, a more accurate model, obtained empirically,

is as follows:

$$H_{MSSF}(j\omega) = \frac{1}{1 + \frac{C_2}{C_1 f_{CK}} j\omega} e^{-j\pi f T_{CK}} \frac{\sin(\pi f T_{CK})}{\pi f T_{CK}}. \tag{3.2}$$

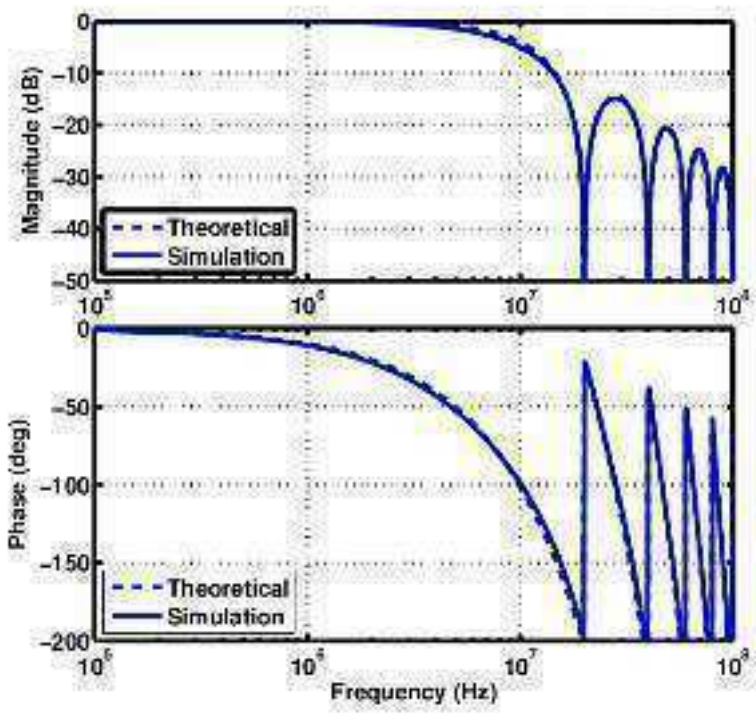

Fig. 3.7. Magnitude and phase responses of MSSF.

Plotted in Figure 3.7 are the magnitude and phase of the MSSF transfer function as predicted by Eq. (3.2) and as obtained from transient circuit simulations. Here, C_1 = 16 pF, C_2 = 1 pF, and f_{REF} = 20 MHz. We observe good agreement between the two. In this example, the filter has a 3-dB bandwidth of 7.4 MHz, at which the phase shift reaches -75°. To minimize this phase shift (which

affects the loop stability), we typically choose $C_1 >> C_2$ and reduce the contribution of the first fraction in Eq. (3.2).

The deep notches in Figure 3.7 distinguish the MSSF from continuous-time filters. These notches suppress the harmonic components generated by the XOR gate in Figure 3.4(a), thereby easing the trade-off between the loop bandwidth and the ripple amplitude. Nonetheless, second-order effects do create some ripple and are addressed later.

3.1.3 Phase Detector Gain

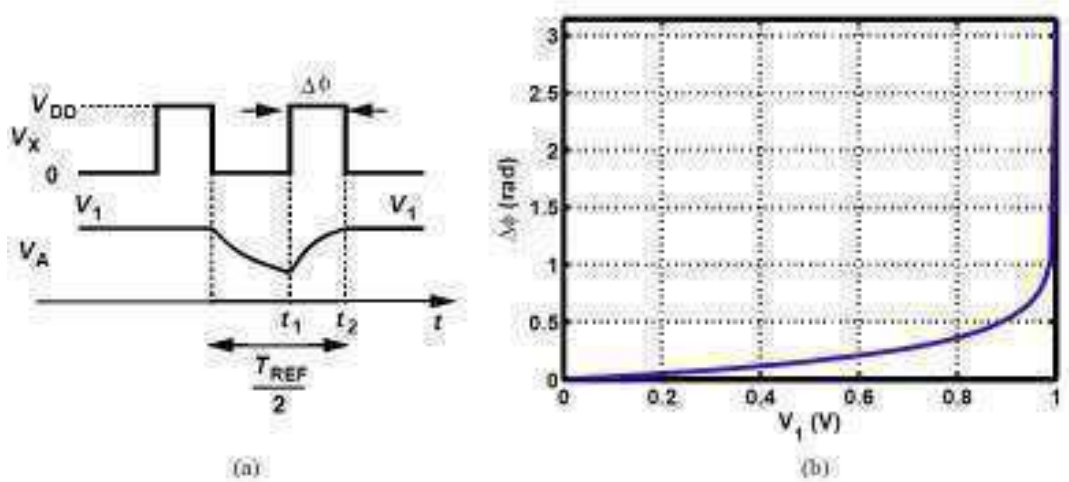

Fig. 3.8. (a) Time-domain waveforms in locked condition, and (b) $\Delta\phi$ versus V_1.

In a traditional type-I PLL, the XOR PD gain, K_{PD}, is constant and equal to V_{DD}/π volts per radian. In our proposed PD/MSSF cascade, on the other hand, the gain varies with the control voltage. To determine the gain, we must compute the output (control) voltage in terms of the phase error and

differentiate the result. As depicted in Figure 3.8(a) for the locked condition with a phase error of $\Delta\phi$, V_A must begin from V_1 and end at V_1, where V_1 is approximately the value necessary for the VCO to operate at Nf_{REF}. Denoting the on-resistance of S_1 in Figure 3.4(a) by R_1 and neglecting the output resistance of the XOR gate, we have at $t = t_1$:

$$V_A = V_1 \exp \frac{-\frac{T_{REF}}{2} + \frac{\Delta\varphi}{2\pi} T_{REF}}{\tau},$$

where $\tau = R_1C_1$ and the duty cycles of the main input and the divider output are assumed 50%. Thus, V_A begins with this initial condition at t_1 and reaches V_1 at t_2:

$$V_1 \exp \frac{-\frac{T_{REF}}{2} + \frac{\Delta\varphi}{2\pi} T_{REF}}{\tau} \exp \frac{-\Delta\varphi \cdot T_{REF}}{2\pi\tau} + V_{DD}\left(1 - \exp \frac{-\Delta\varphi \cdot T_{REF}}{2\pi\tau}\right) = V_1.$$

It follows that

$$V_1 = \frac{V_{DD}\left(1 - \exp \frac{-\Delta\varphi \cdot T_{REF}}{2\pi\tau}\right)}{1 - \exp \frac{-T_{REF}}{2\tau}}. \tag{3.3}$$

Before differentiating V_1 with respect to $\Delta\phi$, we rewrite (3.3) as

$$\Delta\varphi = \frac{-2\pi\tau}{T_{REF}} \ln\left[1 - \frac{V_1}{V_{DD}}\left(1 - exp \frac{-T_{REF}}{2\tau}\right)\right], \tag{3.4}$$

observing that $\Delta\phi = 0$ for $V_1 = 0$ and $\Delta\phi = \pi$ for $V_1 = V_{DD}$. For example, with $\tau = 1.8$ ns, $T_{REF} = 50$ ns, and $V_{DD} = 1$ V, $\Delta\phi$ varies as shown in Figure 3.8(b). We may therefore surmise that the VCO

control voltage can reach 0 or V_{DD} with little change in the ripple amplitude - a behavior in contrast to that of the traditional type-I PLL. However, we must also consider the variation in K_{PD}. From (3.3),

$$K_{PD} = \frac{dV_1}{d\Delta\varphi} = \frac{V_{DD}}{1 - exp\frac{-T_{REF}}{2\tau}} \frac{T_{REF}}{2\pi\tau} exp\frac{-\Delta\varphi \cdot T_{REF}}{2\pi\tau}. \tag{3.5}$$

As $\Delta\phi$ goes from 0 to π, K_{PD} falls by a factor of $\exp[T_{REF}/(2\tau)]$, a very large value if T_{REF} = 50 ns and τ = 1.8 ns. To minimize the K_{PD} variation, we take two measures. First, we consider "valid" only the control voltage range from $0.1V_{DD}$ to $0.9V_{DD}$, i.e., the VCO tuning range should be wide enough for such a voltage compliance. If $V_1 = 0.1V_{DD}$ or $0.9V_{DD}$ in (3.4), the corresponding $\Delta\phi$ can be obtained and substituted in (3.5), yielding a K_{PD} variation by a factor of approximately 9. Second, we increase τ as V_1 goes to lower values by disabling some gate fingers of the NMOS and PMOS devices comprising S_1, thereby correcting for this nine-fold change. This action requires knowledge of V_{cont}, e.g., through the use of an analog-to-digital converter (ADC). We return to this point in Section 3.3.2. Figure 3.9 plots the overall simulated K_{PD} variation for $0.1V_{DD} < V_1 < 0.9V_{DD}$.

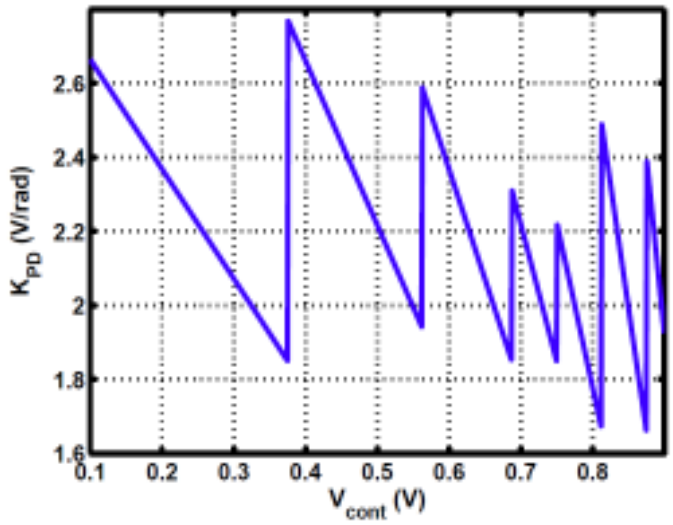

Fig. 3.9. Phase detector gain versus V_{cont} with pre-selected switch size.

3.1.4 Stability Considerations

While greatly suppressing the ripple, our proposed PLL is not unconditionally stable. In this section, we deal with this point. From Eq. (3.2), the loop transmission of the topology shown in Figure 3.4(a) can be expressed as

$$H(j\omega) = \frac{K_{PD}K_{VCO}}{N} \times \frac{1}{j\omega} \times \frac{1}{1 + \frac{C_2}{C_1 f_{REF}} j\omega} e^{-j\pi f T_{CK}} \frac{\sin(\pi f T_{CK})}{\pi f T_{CK}},$$

where have approximated the MSSF sampling rate by f_{REF}. To determine the phase margin, we must examine $\angle H(j\omega)$ at the unity-gain bandwidth, f_{UGB}, i.e., the frequency at which $|\angle H(j\omega)|$ drops to unity. To this end, we make two approximations: (1) as explained in Section III.B, $C_1 >> C_2$ and hence the fraction $1/[1+C_2 j\omega/(C_1 f_{REF})]$ contributes negligibly to $\angle H$ and $|H|$, and (2)

predicting that $f_{UGB} < f_{REF}/2$, we also neglect the effect of the sinc on |H|. It follows that $|H(j\omega)| \approx K_{PD}K_{VCO}/(N\omega)$ and $2\pi f_{UGB} \approx K_{PD}K_{VCO}/N$. The phase contains a -90° contribution by the VCO and $-\pi f T_{REF}$ by the MSSF, $\angle H(j\omega) \approx -\pi/2-\pi f T_{REF}$. The phase margin, $\pi + \angle H(j2\pi f_{UGB})$, is thus equal to

$$PM = \frac{\pi}{2} - \pi f_{UGB} T_{REF} = \frac{\pi}{2} - \frac{K_{PD}K_{VCO}}{2N} T_{REF}. \tag{3.6}$$

Equation (3.6) imposes an upper bound of $f_{REF}/2$ on f_{UGB}. The phase margin reaches about 45° for $f_{UGB} = f_{REF}/4$.

3.1.5 Closed-loop Behavior

As mentioned in Section 2.2.3, the closed-loop input-output bandwidth and the VCO noise transfer bandwidth are of interest. For the former, we have

$$\frac{\emptyset_{out}}{\emptyset_{in}}(j\omega) = \frac{NH(j\omega)}{1 + H(j\omega)}.$$

With the approximation stipulated in Section 3.1.4, $H(j\omega) \approx [K_{PD}K_{VCO}/(Nj\omega)]\exp(-j\pi f T_{REF})$. we denote $K_{PD}K_{VCO}$ by K and write

$$\frac{\emptyset_{out}}{\emptyset_{in}}(j\omega) = \frac{K/\omega}{\left|1 + \frac{K}{jN\omega}\exp(-j\pi f T_{REF})\right|} = \frac{K/\omega}{\sqrt{N^2\omega^2 - 2KN\omega\sin(\pi f T) + K^2}}.$$

Equating the square of this quantity to $N^2/2$ yields the 3-dB bandwidth:

$$N^2\omega_{BW}^2 - 2KN\omega_{BW}\sin\left(\frac{\omega_{BW}T_{REF}}{2}\right) - K^2 = 0.$$

Since $\sin\varepsilon \approx \varepsilon - \varepsilon^3/6$ for $\varepsilon << 1$ rad,

$$\frac{KNT_{REF}^3}{24}\omega_{BW}^4 + (N^2 - KNT_{REF})\omega_{BW}^2 - K^2 = 0.$$

We also denote $KT/N = K_{PD}K_{VCO}/(Nf_{REF}) = 2\pi f_{UGB}/f_{REF}$ by α, obtaining 3-dB bandwidth as

$$2\pi f_{BW} \approx 2\sqrt{3}f_{REF}\sqrt{\frac{\alpha - 1 + \sqrt{(\alpha-1)^2 + \frac{\alpha^3}{6}}}{\alpha}}.$$

Recall from Eq. (3.6) that $f_{REF}/4 < f_{UGB} < f_{REF}/2$ for $45^\circ > PM > 0$, i.e., $\pi/2 < \alpha < \pi$. For this range of α, we have

$$0.55f_{REF} < f_{BW} < 0.71f_{REF}.$$

The key point here is that the closed-loop bandwidth can reach $f_{REF}/2$ with a reasonable phase margin.

The wide bandwidth of the proposed PLL naturally translates to a fast lock transient, e.g., about 10 input cycles as shown in Figure 3.4(b).

For the VCO noise transfer, we have $\Phi_{out}/\Phi_{VCO} = (1+H)^{-1}$. The 3-dB bandwidth is obtained as

$$2\pi f_{n,VCO} \approx 2\sqrt{3} f_{REF} \sqrt{\frac{\alpha + 1 - \sqrt{(\alpha+1)^2 - \frac{\alpha^3}{6}}}{\alpha}},$$

which, for $\pi/2 < \alpha < \pi$, falls in the range of

$$0.16 f_{REF} < f_{n,VCO} < 0.26 f_{REF}.$$

For a fair comparison, we consider only the lower bound and note that, with respect to the two limits prescribed by Eq. (2.2), we have improved the VCO noise suppression bandwidth by about a factor of 2.2 to 4.3. In our synthesizer design, $f_{n,VCO} \approx 0.17 f_{REF}$ for a PM of around 42°. Figure 3.10 shows the simulated settling behavior when PLL input experiences a phase step at 1 us.

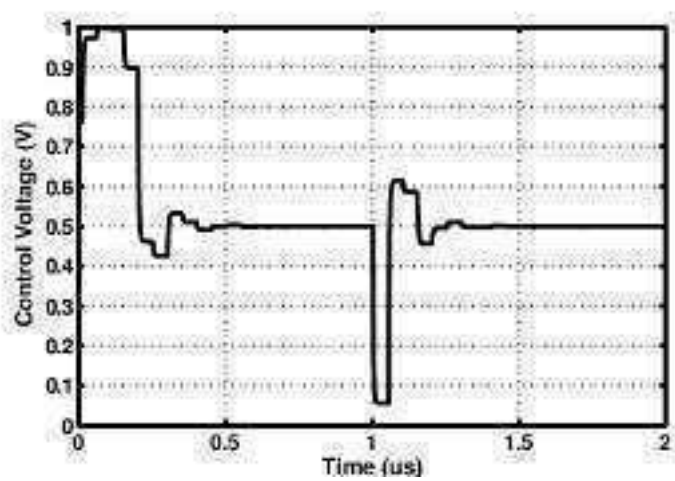

Fig. 3.10. Simulated control voltage with an input phase step at 1 us.

3.1.6 Acquisition Range

The MSSF-based PLL provides a much wider acquisition range than the traditional type-I architecture. Fundamentally, this is because the MSSF in Fig. 3.4(a) is clocked by the feedback signal, thus behaving differently from the continuous-time filter during the acquisition process. In order to formulate the acquisition range, we construct the open-loop configuration shown in Figure 3.11(a), assuming that the VCO operates at a frequency of f_1.

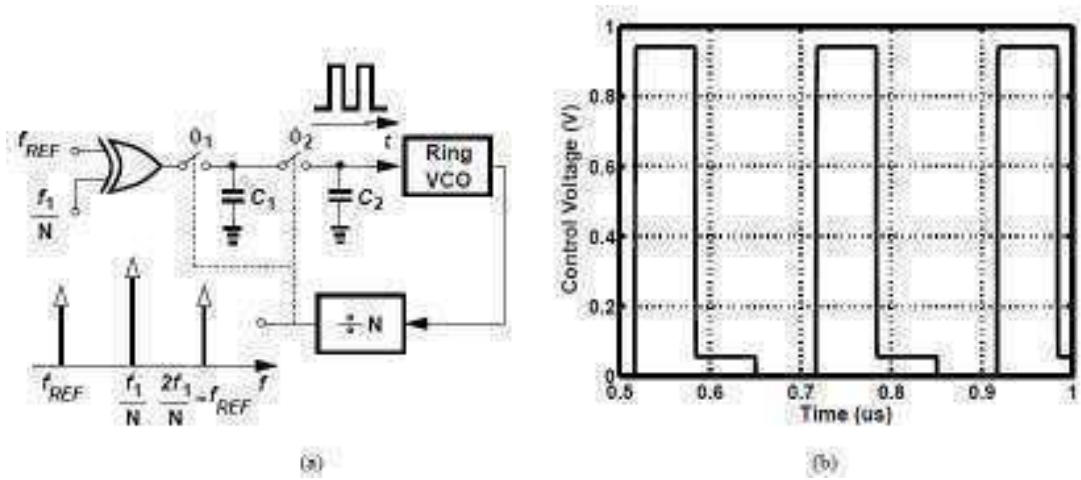

Fig. 3.11. (a) Proposed PLL in open-loop configuration, and (b) simulated control voltage waveform.

We follow the "beat" component generated by the XOR gate, $f_1/N - f_{REF}$, through the sampling filter and consider two cases. First, suppose the sampling process satisfies the Nyquist rate, i.e., $|f_1/N - f_{REF}| < f_1/(2N)$ and hence

$$\frac{2}{3}f_{REF} < \frac{f_1}{N} < 2f_{REF}. \tag{3.7}$$

In this case, the beat component passes through as a "baseband" signal, providing a nearly rail-to-rail voltage swing to the VCO. Figure 3.11(b) plots the simulated control voltage in such a scenario; the VCO is heavily modulated at a rate of $f_1/N - f_{REF}$, producing a strong sideband at the divider output located at $f_1/N-(f_1/N-f_{REF}) = f_{REF}$. In the closed-loop configuration, this sideband yields a dc component at the XOR output, leading to acquisition. Inequality (3.7) can be referred to the output as

$$\frac{2}{3}Nf_{REF} < f_1 < 2Nf_{REF}. \tag{3.8}$$

The loop therefore locks for an initial frequency between 2/3 and 2 times the final value. For example, if the VCO tuning range is from 1.6 GHz to 4.8 GHz, then the loop can always lock to 2.4 GHz. The second case arises if the beat experiences aliasing, i.e., if f_1/N falls outside the range specified by (3.8). The MSSF output now contains a component at $f_1/N-|f_1/N-f_{REF}|$, which does not lead to lock. Circuit simulations confirm these predictions.

3.2 Phase Noise Considerations

The phase noise of the proposed PLL arises from three building blocks, namely, the VCO, the XOR gate, and the sampling filter. We wish to design the VCO according to the overall phase noise specification and reduce to negligible levels the XOR and filter contributions.

3.2.1 VCO Phase Noise

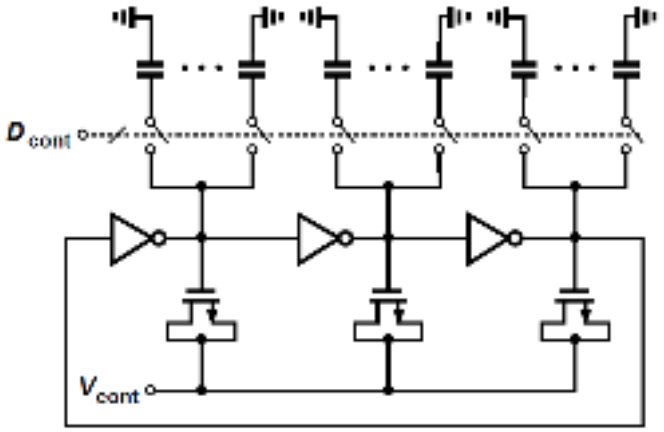

Fig. 3.12. VCO implementation.

The VCO is designed as a three-stage inverter-based ring oscillator. Depicted in Figure 3.12, the circuit employs MOS varactors for fine control and banks of switchable capacitors for coarse control. To achieve low flicker-noise-induced phase noise, we choose W/L = 36 um/0.28 um for both PMOS and NMOS devices in each inverter. The varactors have a W/L of 26 um/0.2 um, providing a tuning range of about 200 MHz, and the capacitor banks consist of twelve 25-fF units,

offering a range from 2 GHz to 3 GHz. The circuit draws 3.1 mW from a 1-V supply at 2.4 GHz and exhibits a phase noise of -96 dBc/Hz at 1-MHz offset.

Three aspects of the VCO design merit remarks. First, simulations suggest that, among various ring oscillator tuning techniques, varactors cause the least degradation in phase noise as the frequency is varied for a given power consumption. In a starved-inverter topology, for example, the starving transistors themselves contribute significant phase noise as the frequency is decreased.

Second, as with other inverter-based rings reported in prior work, the VCO suffers from supply sensitivity. In practice, such VCOs are fed from a low-dropout (LDO) regulator. In our prototype, we have used two separate supply pins for the analog and digital sections.

Third, the three node waveforms within the ring can be combined to generate quadrature phases.[3] A full-size inverter sensing one node and a half-size inverter sensing another can merge their output nodes, generating 90° or 180° from 120° phases.

The shaping of the VCO phase noise deserves a note as well. Unlike type-II PLLs, a type-I PLL cannot force flicker-noise-induced phase noise to zero at zero frequency. To see this point, we

[3] For more precise quadrature generation, the single-ended ring oscillator in [15] can be used.

choose a small ω in the VCO noise transfer function and multiply the magnitude squared of the result by the VCO phase noise profile, e.g., η/ω^3, where η is a constant. The PLL output phase noise emerges as $N^2\omega^2(\eta/\omega^3) = N^2\eta/\omega$, rising as ω falls. Nevertheless, by virtue of its large bandwidth, the proposed PLL still displays a smaller integrated phase noise that a type-II architecture would. Figure 3.13 plots the simulated free-running phase noise of the above VCO and the shaping that it experiences in the two loops. (Here, the charge-pump PLL is assumed to have a loop bandwidth of $f_{REF}/20$,[4] while the type-I PLL is based on our architecture with a bandwidth of $f_{REF}/2$. Our design leads to an integrated phase noise of 0.35° from 100 kHz to 15 MHz, and the type-II loop to 1.14° for the same range. In practice, the charge pump flicker noise makes this comparison more favorable towards the proposed PLL.

[4] For a reference spur level below -60 dBc, reported type-II PLLs have a bandwidth of no more than $f_{REF}/20$; hence this choice for a fair comparison with our architecture.

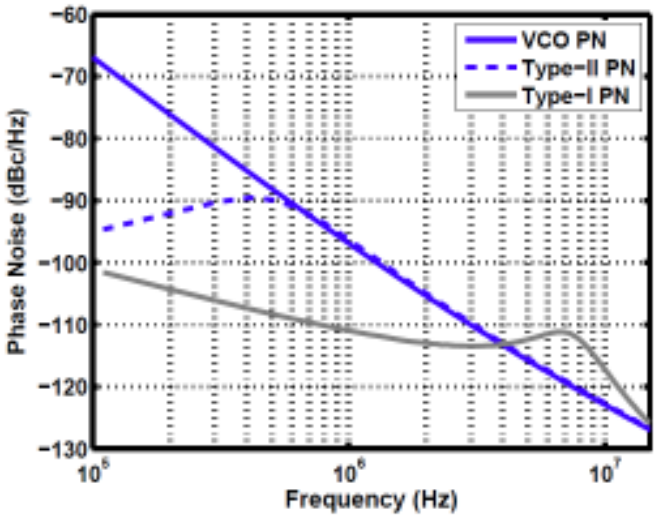

Fig. 3.13. VCO phase noise in free-running mode and in type-II and proposed PLLs.

3.2.2 PD and MSSF Phase Noise

In order to minimize the contribution of the PD/MSSF cascade in Figure 3.4(a), we take several measures. First, the XOR incorporates PMOS and NMOS devices with W/L = 32 um/80 nm and 16 um/80 nm, respectively, achieving a phase noise of -171 dBc/Hz at 5-MHz offset while consuming 86 uW at 20 MHz. This leads to an in-band phase noise at the PLL output equal to -171 dBc/Hz + 20logN = -129 dBc/Hz. Second, since S_1 carries large transient currents and can potentially generate high flicker noise, we choose W/L = 20 um/100 nm for this device. Third, the kT/C noise associated with S_2 and C_2 is reduced by selecting C_2 = 1 pF (C_1 = 16 pF contributes negligibly). This kT/C noise translates to in-band phase noise at the PLL output according to $S_{out,MSSF} \approx [kT/(2C_2)]f_{REF}^{-1}N^2K_{PD}^2$, where the factor of 2 accounts for the fact that

C_2 appears in parallel with C_1 (>> C_2) for about half of the input period. With C_2 = 1 pF and K_{PD} = 2.2 V/rad, we have $S_{out,MSSF}$ = -126 dBc/Hz.

The foregoing study also prescribes a design procedure: we first pick the value of C_2 for negligible phase noise contribution and then choose C_1 to be 10 to 20 times larger. Finally, we size S_1 and the XOR devices for negligible noise as well.

3.3 Spur Reduction

Despite the transfer notches introduced by the sampling filter, we observe sidebands on the order of -50 to -55 dBc at the VCO output. This phenomenon arises from three mechanisms. First, the large VCO varactors (W/L = 26 um/0.2 um) draw a significant gate leakage current (~ 80 nA) from C_2 in Figure 3.4(a), causing a 2-mV droop in each cycle. Second, the leakage, charge injection, and clock feedthrough of S_2 produce another 1 mV_{pp} of ripple. Third, in the presence of ground bond wires, the bounce on the bottom plate of C_1 persists after S_2 turns on, disturbing the control line periodically.

We propose the use of "harmonic" traps to suppress the ripple with little compromise in the bandwidth. Applicable to any PLL architecture and illustrated in Figure 3.14, the idea is to add

one or more series resonant branches in parallel with the control line, forming a low impedance to ground at f_{REF}, $2f_{REF}$, etc.

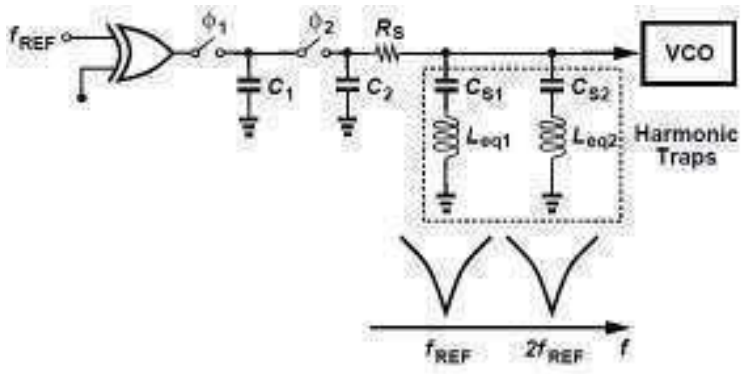

Fig. 3.14. Concept of harmonic traps.

Harmonic traps entail three issues. First, active implementations ultimately present a trade-off between the trap impedance and the power consumption, potentially unable to fight the MSSF output impedance. For this reason, R_S (≈ 2.5 kΩ) is inserted in Figure 3.14. Second, the traps must have a sufficiently high Q so as to contribute negligible phase shift and noise for $f \leq f_{REF}/2$. Third, the traps' resonance frequencies must be calibrated with adequate resolution to deal with PVT variations.

3.3.1 Harmonic Trap Design

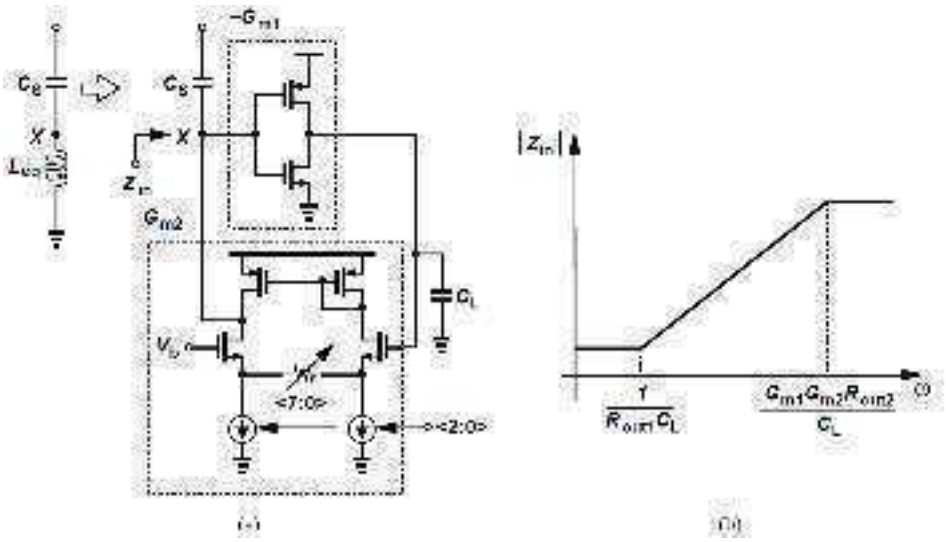

Fig. 3.15 (a) Harmonic trap implementation, and (b) magnitude of gyrator input impedance.

Each trap consists of a capacitor in series with an active inductor, obtained by gyrating another capacitor. As shown in Figure 3.15(a), G_{m1} and G_{m2} constitute a gyrator, transforming C_L to $Z_{in} = L_{eq}s = C_L s/(G_{m1}G_{m2})$ if their output impedances are assumed infinite. For example, the f_{REF} trap uses G_{m1} = 0.92 mS, G_{m2} = 54 uS and C_L = 3.5 pF, creating L_{eq} = 70 uH. The degeneration resistance and the bias currents within G_{m2} are programmable. The power dissipation is 170 uW.

For design purposes, we need a more accurate expression for Z_{in}. If the output impedances of G_{m1} and G_{m2} are denoted by R_{out1} and R_{out2}, respectively, then

$$z_{in} = \frac{(R_{out1}C_L s + 1)R_{out2}}{(R_{out1}C_L s + G_{m1}R_{out1}G_{m2}R_{out2} + 1)}.$$

Plotted in Figure 3.15(b), $|Z_{in}|$ reveals an inductive behavior for $(R_{out1}C_L)^{-1} < \omega < G_{m1}G_{m2}R_{out2}/C_L$. It is important that the trap resonance frequency, ω_{res}, lie well between the zero and pole frequencies so that Z_{in} approaches a pure inductor. We therefore view $(R_{out1}C_L)^{-1} < \omega_{res} < G_{m1}G_{m2}R_{out2}/C_L$ as a guideline for choosing C_L. If Z_{in} is rewritten as $[C_L s/(G_{m1}G_{m2})+(G_{m1}G_{m2}R_{out1})^{-1}]||R_{out2}$, then we recognize that the inductance sees a series resistance equal to $(G_{m1}G_{m2}R_{out1})^{-1}$ and a parallel resistance equal to R_{out2}. Since R_{out2} is sufficiently large in our design, the quality factor is approximately equal to $R_{out1}C_L\omega$, about 15 at f_{REF} = 20 MHz. With the large transistor dimensions chosen in this design, the gyrator input-referred offsets are less than 6 mV. To cover PVT variations, the trap frequency has a programmable range of ±30% around its nominal value with a resolution of 0.6 MHz. Circuit simulations indicate that the traps negligibly affect the loop settling time.

The noise contribution is formulated by modeling the gyrator noise by a current source and subjecting it to a (high-pass) transfer function to V_{cont} and another from V_{cont} to Φ_{out}. Calculations and simulations predict a phase noise of -131 dBc/Hz at 5-MHz offset resulting from the traps.

3.3.2 Notch Calibration

To calibrate the traps, we must seek an error whose value reaches a minimum as the notch frequency reaches the desired value, e.g., f_{REF}. The control ripple amplitude is one such error. But we must also measure this error with reasonable fidelity as, towards the end of calibration, it becomes very small. In our design, for example, a spur level of -60 dBc at the output is equivalent to a ripple amplitude of about 0.28 mV_{pp}.

We employ a Δ modulator as a compact, low-power ADC to measure the ripple waveform and reconstruct it in the digital domain. Shown in Figure 3.16(a), a traditional Δ modulator consists of a comparator and a low-pass feedback network, forcing V_p to track V_{in}. As a result, the running average of the pulsewidth-modulated output also tracks V_{in}, provided that R_DC_D is sufficiently long [Figure 3.17(a)]. Otherwise, the input peaks do not exceed the peaks of V_p, causing failure [Figure 3.17(b)].

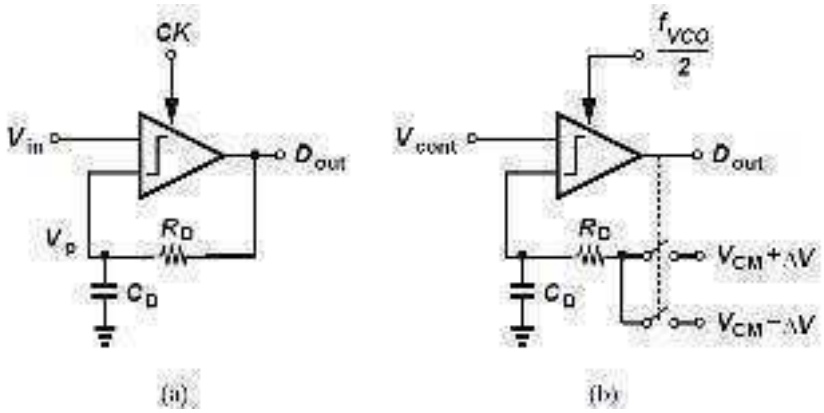

Fig. 3.16. (a) Traditional, and (b) proposed Δ modulator architectures.

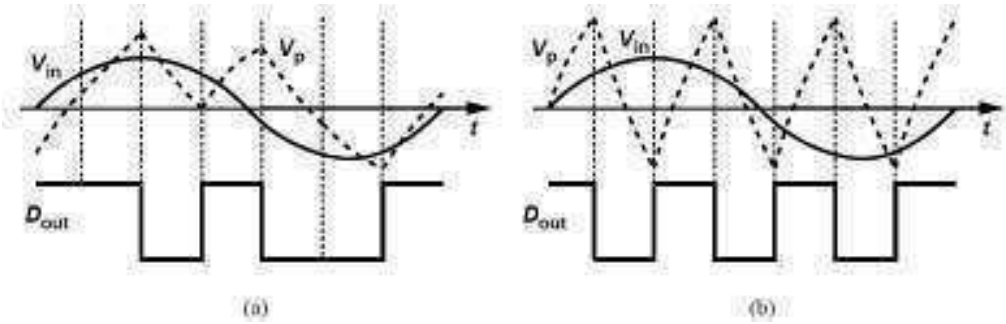

Fig. 3.17. Effect of R_DC_D on Δ modulator operation: (a) long time constant, and (b) short time constant.

Similarly, the Δ modulator of Figure 3.16(a) fails for small or slow input swings; it simply generates a periodic output at half of the clock frequency if the input peaks do not exceed the peaks of V_p. It can be proved that the sensitivity is given by $V_{DD}\{1\text{-}\exp[-T_{CK}/(2R_DC_D)]\}$, where the comparator output is assumed to swing between 0 and V_{DD}. For example, a sensitivity of 0.28 mV_{pp} with $f_{CK} \approx 1.2$ GHz translates to $R_DC_D = 3$ us, demanding very large values for R_D and C_D. To resolve this issue, we modify the architecture as depicted in Figure 3.16(b), where the comparator is clocked at $f_{VCO}/2$ and its output drives a 1-bit DAC with a much smaller swing, ±ΔV. A ΔV of 25 mV, for example, allows a 20-fold reduction in the R_DC_D product. In this design, we have $R_D = 50$ kΩ, $C_D = 4$ pF, and a StrongArm comparator consuming 80 uW.

Since the ripple amplitude is a convex function of the trap resonance frequency, we must somehow decide when the calibration has reached a minimum. As shown in Figure 3.18, we

measure the ripple for three consecutive gyrator codes, D_{k-1}, D_k and D_{k+1}, and consider three cases: (1) if $A_{k-1} > A_k > A_{k+1}$, we are on the descending slope and must increase the code; (2) if $A_{k-1} < A_k < A_{k+1}$, we are on the ascending slope and must decrease the code; (3) if $A_k < A_{k-1}$ and $A_k < A_{k+1}$, then D_k is the optimum value. The calibration runs in the background and compensates for temperature and supply drifts.

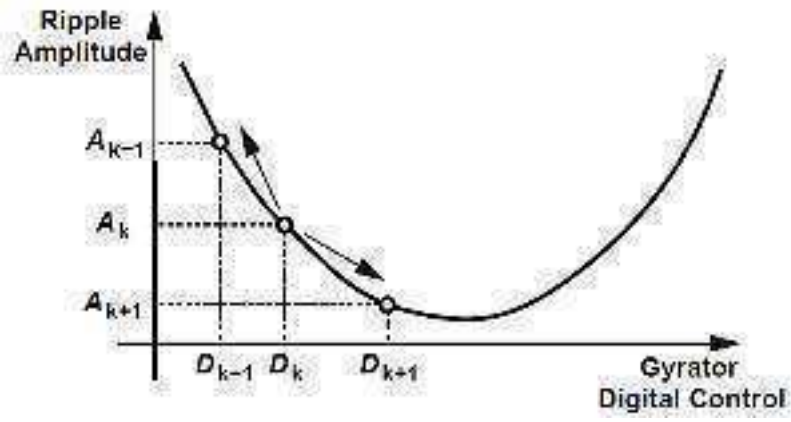

Fig. 3.18. Notch calibration algorithm.

The overall synthesizer architecture is shown in Figure 3.19. The feedback divider provides N = 7 - 220, but only the range from 120 to 124 is used for the 2.4-GHz band. Figure 3.20 shows the simulated phase noise plot before and after harmonic traps are on. As can be seen, the traps contribute negligible phase noise but increases the peaking by 1 dB due to their addtional phase shift.

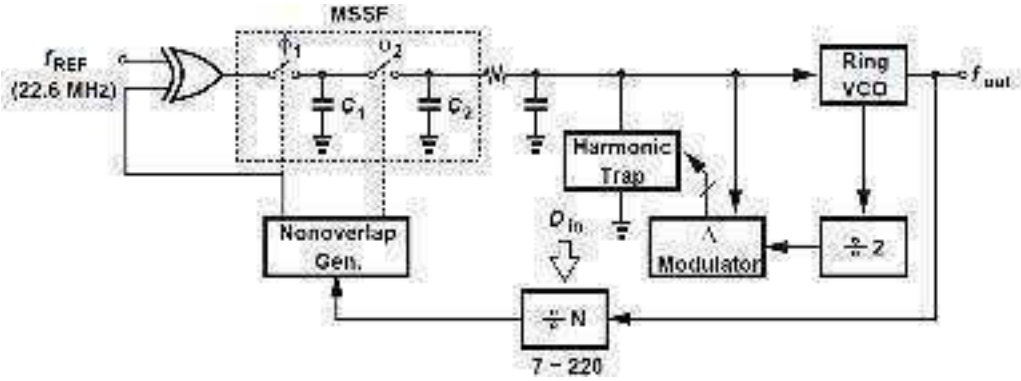

Fig. 3.19. Final proposed architecture of the synthesizer.

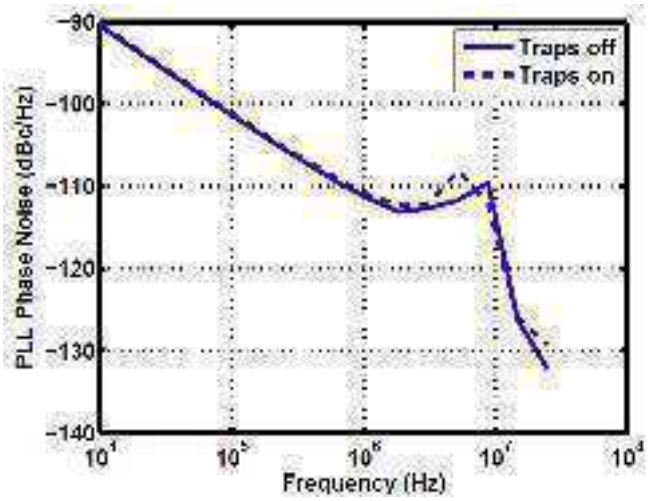

Fig. 3.20. Simulated PLL phase noise before and after harmonic traps are on.

CHAPTER 4

A 2.4-GHz 6.4-mW Fractional-N Inductorless RF Synthesizer

In this chapter, we would like to extend the wideband architecture to the fractional-N loop. We will introduces a cascaded synthesizer architecture that achieves a wide bandwidth to suppress the ring-VCO phase noise.

Section 4.1 reviews the quantization noise reduction techniques in the previous literature. Section 4.2 describes the proposed synthesizer architecture. Section 4.3 analyzes the loop dynamics and delves into the delay-line-based filter and Section 4.4 shows the circuit implementation.

4.1 Prior Art

During the last decade, various techniques have been proposed to cancel or filter out the ΣΔ quantization noise. One example is the DAC feedforward cancellation in [19]. This method, however, is sensitive to mismatches between the DAC and CP. In addition, the DAC itself needs to be linear enough to avoid fractional spur generation. Up till now, numerous methods based on this idea have been developed ([20] - [22]) to achieve better performance. Nevertheless, the stringent requirement on the DAC and the complex calibration loop makes the design difficult.

Another method is to filter out the quantization noise. [23] processes the ΣΔ modulator output by an FIR filter to achieve noise reduction. But this approach requires a number of dividers and CP/PFDs and ends up with a large power consumption.

There are also some works with cascaded architecture to increase the oversampling ratio in the ΣΔ modulator. [24] employs a wideband integer-N PLL as the first stage and a narrow-band fractional-N CPPLL as the second stage. The second stage employs an LC oscillator and has a loop bandwidth of around 1/800 of its input frequency to reduce the ΣΔ noise. If a ring-VCO were used, the phase noise would be too high for RF applications.

All these methods help to resolve the tight tradeoff between the loop bandwidth and the ΣΔ noise suppression. Nonetheless, no successful fractional-N inductorless RF synthesizer has been demonstrated yet. This chapter will present a robust, simple and power efficient architecture to further bring the phase noise of ring-based synthesizers closer to LC-based counterparts.

4.2 Proposed Architecture

4.2.1 Filter after Divider

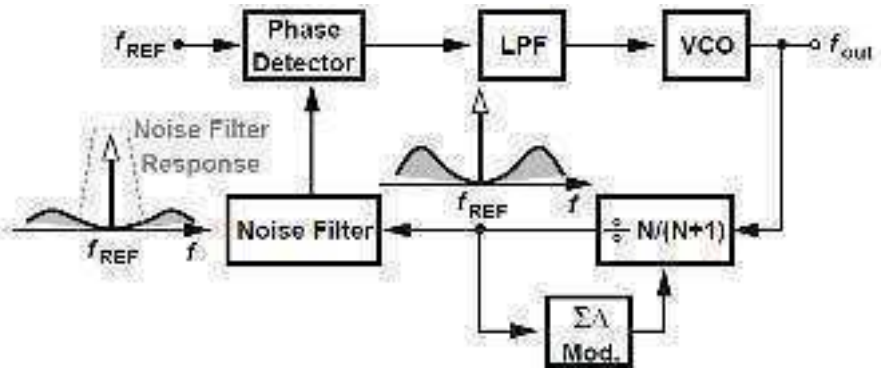

Fig. 4.1. Conceptual synthesizer with noise filter.

The previous noise cancellation techniques require a high linearity and a good matching of CP and DAC. Instead of dealing with these design difficulties, we consider inserting a noise filter after the feedback divider in Figure 4.1. This filter must center at f_{REF} with sharp roll-off to suppress the quantization noise.

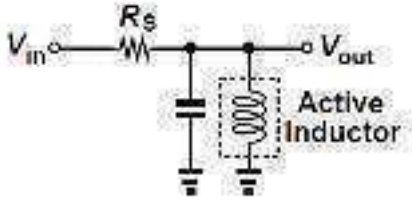

Fig. 4.2. Analog bandpass filter topology.

In the analog domain, we can implement this filter by a parallel resonance branch with active inductors. As shown in Figure 4.2, the resonance branch creates a bandpass impedance at f_{REF}. Hence, the transfer function from V_{in} to V_{out} possesses a bandpass characteristic. The active

inductor can be created with a gyrator and a capacitor. However, the divider output is a rail-to-rail digital signal, which will compress those G_m stages. Even though a small amplitude is preferable for a good linearity, we cannot choose a large R_S to reduce the output swing because this feedback signal must have a large slew rate so as to avoid high flicker noise contribution from the G_m and the following PD. Figure 4.3 shows the simulated results of this bandpass transfer function with small-signal and large signal inputs, respectively. As can be seen from the plot, the bandpass filter turns out to be a low pass filter when the input swing is large enough to cause compression in the G_m stages. The linearity trades with noise and power dissipation, making the analog filter less attractive in this scenario.

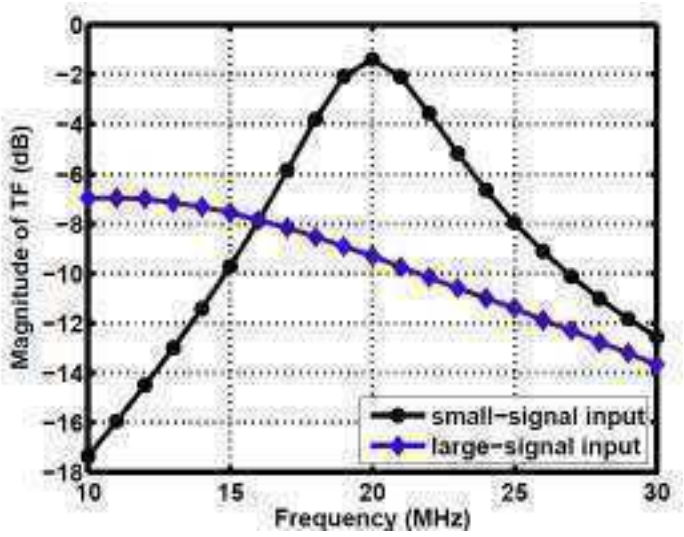

Fig. 4.3. Simulated transfer function with small-signal and large-signal inputs.

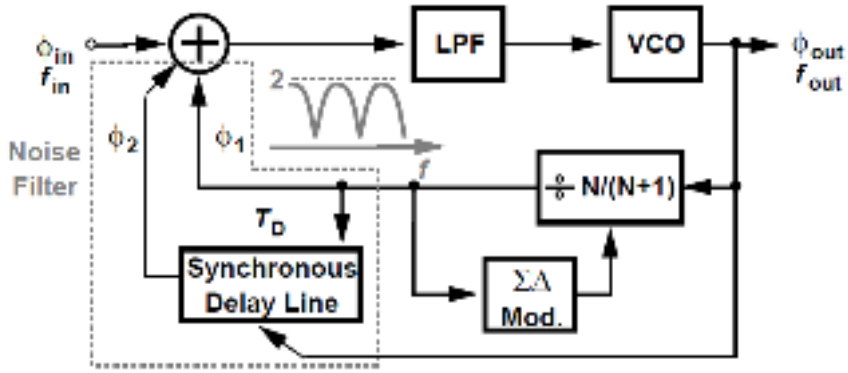

Fig. 4.4. Conceptual synthesizer with delay-line-based noise filter.

Consider the fact that the divider output is a digital signal, a better solution lies in the digital domain. As shown in Figure 4.4, we add the feedback signal to its delayed version, aiming to suppress the noise through this addition. The feedback signal is passed through a synchronous delay line and is delayed by T_D. After adding those two signals, the quantization noise will be filtered. As depicted in Figure 4.4, ϕ_1 represents the feedback signal after divider, ϕ_2 is delayed by T_D from ϕ_1. Therefore, if the delay value is large enough to inverse the phase noise of interest, $\phi_1 + \phi_2$ contains less noise. The transfer function of this noise filter is $1 + \exp(-sT_D)$, which can be simplified to $2\cos(\pi f T_D)\exp(-i\pi f T_D)$, exhibiting notches at

$$f = \frac{2n+1}{2T_D}, n = 0, 1, 2, \ldots$$

With T_D = 10 ns, the transfer function is plotted in Figure 4.5. And notches at (2n+1)·50 MHz are observed.

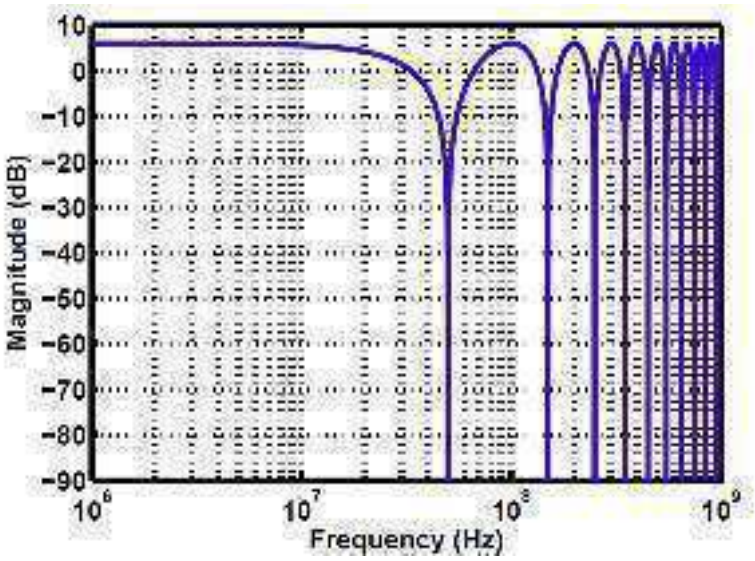

Fig. 4.5. Delay-line-based filter characteristic with T_D = 10 ns.

The delay line used here is a synchronous one consisting of simple flip-flops (FFs). Compared to the asynchronous delay line whose delay value trades with phase noise and power consumption, this synchronous counterpart consumes only 300 uW at 2.4 GHz while generating a 10-ns delay.

4.2.2 Loop Stability

The delay introduced within the feedback path normally degrades the phase margin and affects the loop stability. Interestingly, this synchronous delay used here will not cause stability issue.

Shown in Figure 4.6 is the time-domain waveform of the VCO, divider and FF outputs. Due to the divider delay, the first FF samples a “0” at the first clock rising edge and hence delays the divider output by one VCO cycle, T_{VCO}. Similarly, each of the following FF delays the divider

output by one T_{VCO}. To study the effect on the feedback signal itself, we apply a small phase perturbation on f_{out} and examine how long it takes to propagate to the delay line output. As the grey line shows, the perturbation appears at the last FF output directly because all FFs are clocked by the VCO output. This indicates the VCO output experiences only the clock-to-q delay, not any mT_{VCO} latency, so loop stability is not affected. These FFs in the delay line actually acts like retiming FFs. The above analysis agrees with the previous belief that retiming FFs help loop stability.

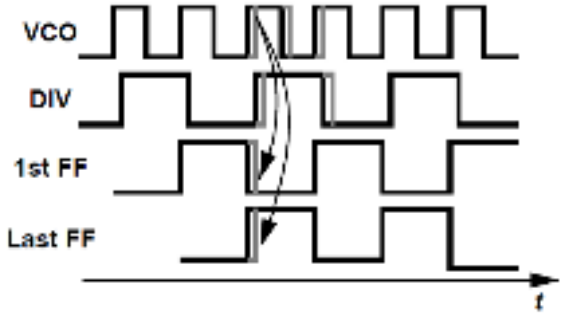

Fig. 4.6. Time-domain waveform of the VCO, divider and delay line outputs.

4.2.3 Cascade Architecture

With a reference frequency of around 20 MHz, we need to create a notch, say at 0.5 MHz, the required delay will be 1 us. For a VCO frequency at 2.4 GHz, that means 2400 FFs have to be used in the synchronous delay line, resulting in a large power dissipation. For example, the clock buffer itself consumes a CV^2f power comparable to the PLL loop.

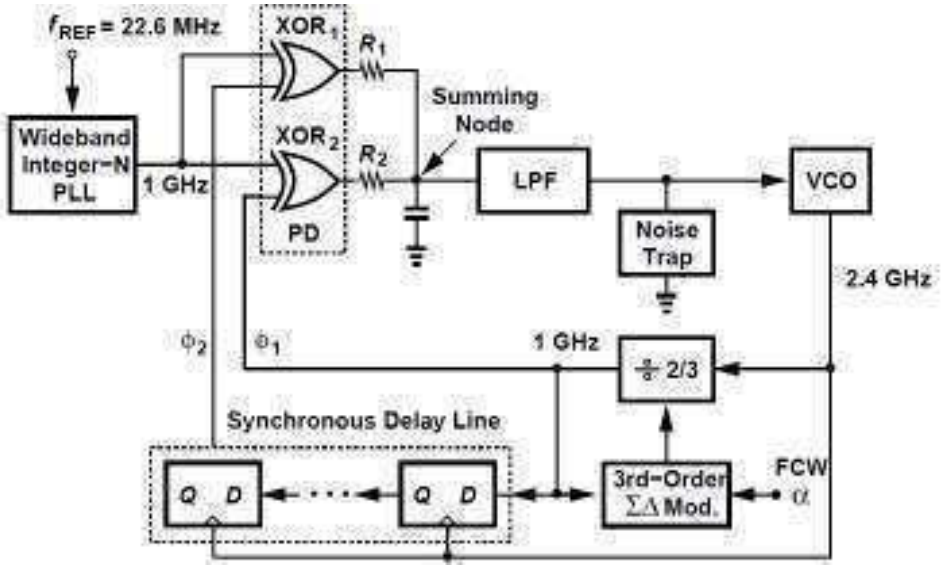

Fig. 4.7. Proposed fractional-N synthesizer architecture.

To reduce the power consumption, we propose a cascaded architecture in Figure 4.7. The first stage (PLL1) is a wideband integer-N PLL based on the architecture in [5]. It generates a 1-GHz output with a loop bandwidth of $f_{REF}/2$. This 1-GHz output, denoting as f_{REF1}, is used as the reference signal for the second stage. Now the second stage (PLL2) achieves the fractional-N operation to generate a 2.4-GHz output. PLL2 has a bandwidth of around $f_{REF1}/80$ (≈ 12 MHz), heavily suppressing the ring-VCO phase noise. The out-of-band quantization noise is reduced by a delay-line-based noise filter and an analog noise trap. The delay line consists of 24 static FFs to generate multiple notches at (2n+1)·50 MHz.

One important question is how we add the divider output and its delayed version. The addition is straightforward at voltage/current domain after the phase detector. However, the phase detector must be linear enough to avoid noise folding since the quantization noise has not been attenuated yet before the summation point. It is known that the CP current mismatch arises nonlinearity. Therefore, we use XOR phase detector at the front. The XOR PD is inherently linear with a constant gain, K_{PD} of V_{DD}/π V/rad. These XOR outputs drive resistors R_1 and R_2, and are combined to perform summation. We should notice that the relative values of R_1 and R_2 determine the path strength. At the summing node, the quantization noise is filtered by these notches. The following low-pass filter further reduces the high frequency noise.

The low-pass filter is a fourth-order filter with resistors and capacitors shown below: $R_3 = R_4 =$ 1 kΩ, R_5 = 3 kΩ, R_6 = 2 kΩ, $C_2 = C_3 = C_4$ = 0.4 pF, C_5 = 0.2 pF. Since the two paths perform addition, we can consider R_1 and R_2 in parallel for the loop transmission. With $R_1 = R_2$ = 4.5 kΩ and C_1 = 3 pF as shown in Figure 4.8, this high order filter has left-plane poles at 14.4 MHz, 65.4 MHz, 294 MHz, 659 MHz and 1.11 GHz, which suppresses the out-of-band quantization noise of the high-order ΣΔ modulator. The loop filter itself contributes a small amount of in-band phase noise: $10\log(4kTR_{tot}N^2/K_{PD}^2) \approx -140$ dBc/Hz.

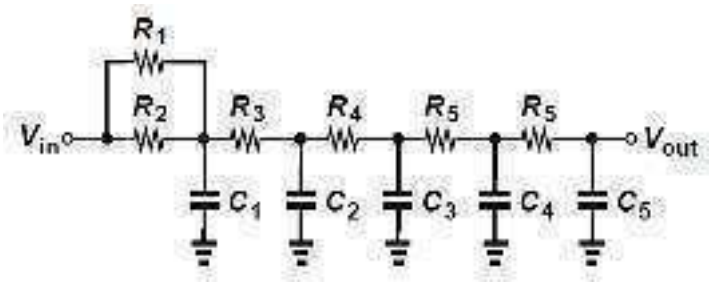

Fig. 4.8. Low-pass filter schematic.

The delay-line-based filter transfer function has multiple peaks at $f = n/T_D$, n = 0, 1, 2, ... That means the peak at 100 MHz, which locates between the first and the second notches, may cause an undesired phase noise bump. Of course, it also depends on the quantization noise shape. In order to achieve additional suppression at around 100-MHz offset frequency, we incorporate an analog noise trap on the control voltage. The trap implementation and analysis will be shown in Section 4.4.1.

4.2.4 Delay-Line-Based Filter Phenomena

Since the divider output has a wideband spectrum from 0 all the way to 2 GHz, one may doubt that aliasing happens after sampling by the 2.4-GHz VCO signal. A time-domain waveform in Figure 4.9 illustrates this point. At t_1, modulus control changes from 2 to 3, making the divider output to swallow one more VCO cycle than the previous divide-by-2 condition. The first FF now samples the divider output and delays it by one T_{VCO}. The same applies to the following FFs. Importantly,

the delayed signal maintains exactly the same shape and duty cycle as the divider output, indicating no distortion or aliasing.

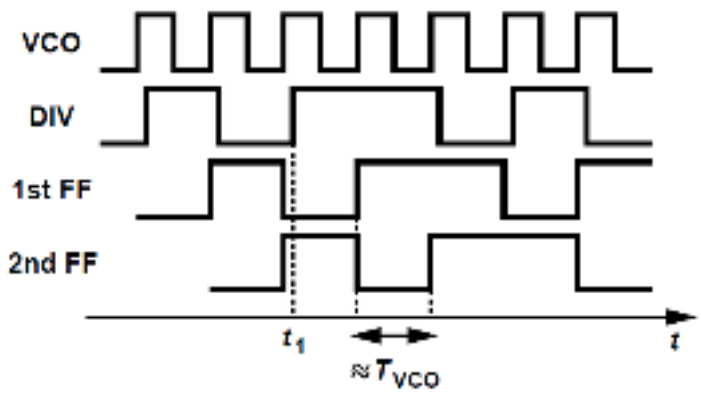

Fig. 4.9. Time-domain waveform of the delay-line when divide ratio changes.

In another perspective, the synchronization between the VCO and divider output avoids aliasing. We break the loop, apply an ideal 2.4-GHz signal to the divider input and set the frequency control word to 0.4. The divider output then contains a 1-GHz (= 2.4 GHz/(2+0.4)) fundamental tone and the surrounding high-pass shaped noise signal. Figure 4.10 shows the magnitudes and phase difference between ϕ_1 and ϕ_2, respectively. The same magnitude of ϕ_1 and ϕ_2 proves that there is no aliasing after passing through this delay line. Meanwhile, the phase difference is initially zero and starts to increase until 180° at around 50 MHz. After that, the difference will decrease to zero at 100 MHz and increase to 180° again at 150 MHz. This repeats as

it goes to higher frequencies. Figure 4.11 shows the magnitude response of $\phi_1 + \phi_2$. It has notches at 50-MHz offset, 150-MHz offset and so on.

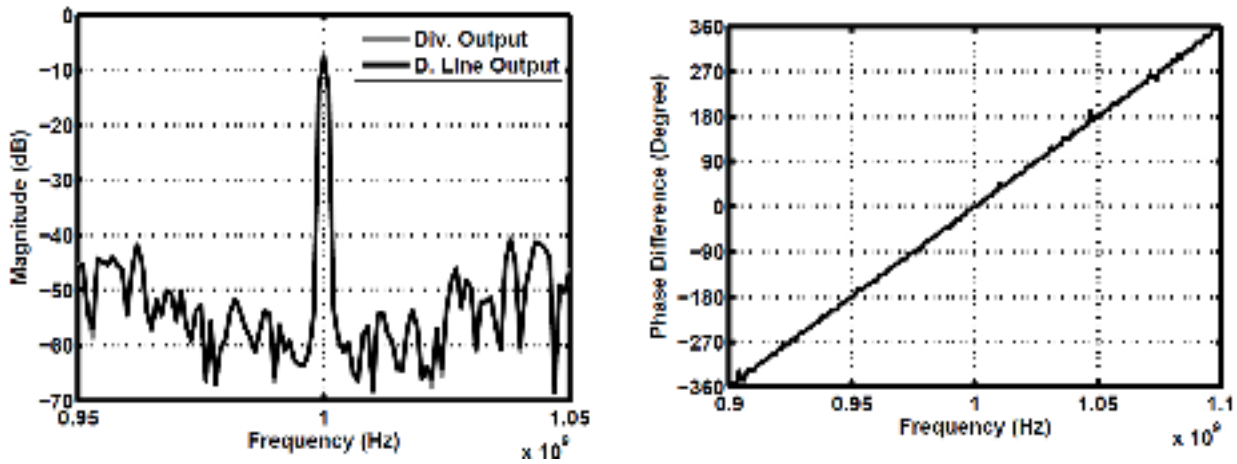

Fig 4.10. Magnitudes of ϕ_1 and ϕ_2 and phase difference between them.

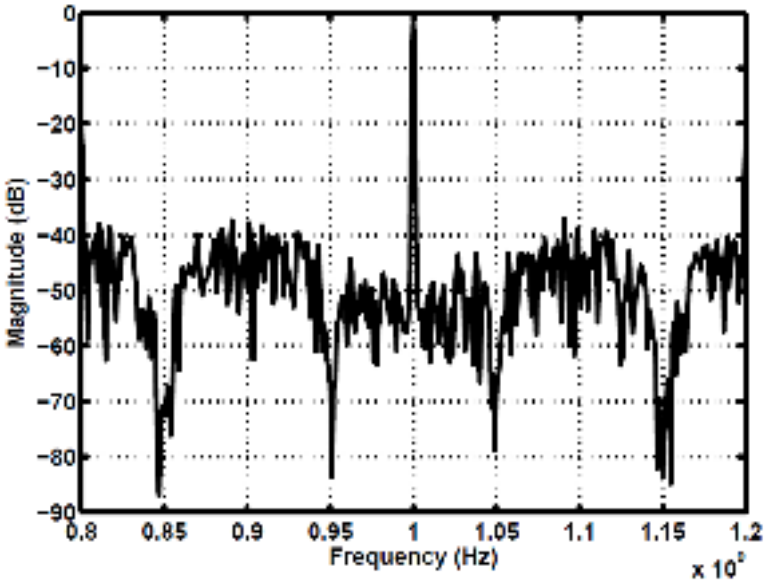

Fig. 4.11. Magnitude of $\phi_1 + \phi_2$.

Another phenomenon is concerned with the DC levels of the two XOR outputs. Since the PD characteristic repeats every 2π rads, the two DC levels will be the same if $T_D = nT_{REF1}$. With 24 FFs, T_D is calculated as

$$T_D = 24T_{VCO} = \frac{24T_{REF1}}{2+\alpha}.$$

If $\alpha = 0.4$, T_D is exactly 10 input cycles. However, when α departs from 0.4, as shown in Figure 4.12(a), the DC level will be different. As long as those two resides on the positive slope, stability will not be affected. Nevertheless, if the difference is large enough to place either XOR at the negative slope as shown in Figure 4.12(b), the loop may become less stable. To alleviate this issue, we can change f_{REF1} in tandem with α. In addition, the delay line length can be programmed to accommodate the change in the divide ratio.

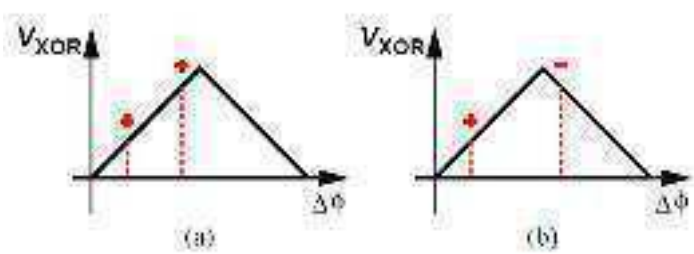

Fig. 4.12. PD characteristics with (a) XORs on the same slope, and (b) XORs on the opposite slopes.

4.3 Bandwidth Considerations

The phase noise of PLL2 mainly comes from three parts: f_{REF1}, the second ring-VCO and the ΣΔ quantization noise. Since the second loop itself must have a wide bandwidth for VCO noise suppression, it has little filtering effect on the noise in f_{REF1}. Consequently, we only consider the noise from the second VCO and ΣΔ modulator, aiming to find an optimum bandwidth. First, the loop transmission and transfer functions must be derived.

4.3.1 Transfer Functions

Analyzed in Section 4.2.2, the delay line has no effect on the VCO output, and hence the loop transmission. Assume the loop filter has a transfer function of $H_F(s)$, the loop transmission can be derived as

$$H_{open}(s) = \frac{K_{PD}K_{VCO}}{Ns} H_F(s).$$

Thus, the PLL input-output transfer function and the VCO noise transfer function can be derived from $H_{PLL}(s) = NH_{open}(s)/[1+H_{open}(s)]$ and $H_{VCO}(s) = 1/[1+H_{open}(s)]$, respectively. These are the same as the traditional PLL loop, however, as mentioned before, the quantization noise transfer function is different. To study this, we short the input to a small signal ground. The output voltage V_s at summing node can be written as:

$$V_s = \frac{R_1}{R_1 + R_2} \emptyset_1 + \frac{R_2}{R_1 + R_2} \emptyset_1 e^{-sT_D},$$

giving a transfer function from ϕ_1 to V_s as:

$$\frac{V_s}{\emptyset_1} = \frac{R_1}{R_1 + R_2} + \frac{R_2}{R_1 + R_2} e^{-sT_D},$$

Since $R_1 = R_2$, the above equation simplifies to:

$$\frac{V_s}{\emptyset_1} = \frac{1 + e^{-sT_D}}{2}.$$

The transfer function has a peak magnitude of 1, which differs from the direct addition by a factor of 2. This means the quantization noise has never been amplified. Combining with the PLL transfer function, the quantization noise transfer function from divider output to PLL output is:

$$H_Q(s) = \frac{NH_{open}(s)}{1 + H_{open}(s)} \cdot \frac{1 + e^{-sT_D}}{2}.$$

In essence, the input-output and the VCO-output transfer functions are the same with the traditional type-I PLL, but the quantization noise transfer function incorporates an additional filter. Figure 4.13 shows the simulated phase noise due to ΣΔ modulator with and without the delay-line-based noise filter. Simulation results confirm the above analysis.[5]

[5] The simulated low frequency noise is not accurate enough because it requires a much longer simulation time.

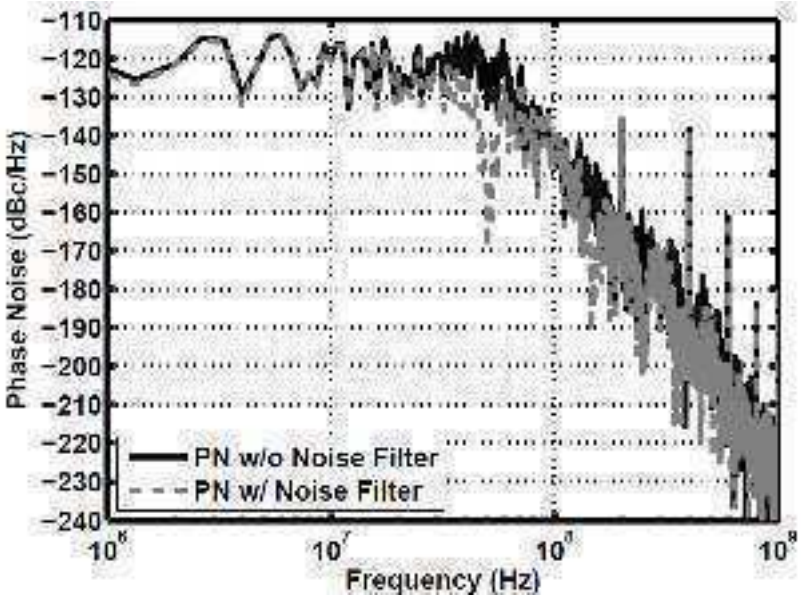

Fig. 4.13. Simulated phase noise from ΣΔ modulator with and without delay-line-based filter.

4.3.2 Optimum Bandwidth

With a large loop bandwidth in the fractional-N synthesizer, the ΣΔ modulation contributes to a high out-of-band noise. In our architecture, we can achieve wideband operation due to the following two reasons. First, the delay-line-based noise filter will suppress the quantization noise, starting from 20-MHz offset and reaches a dip at 50-MHz offset. Second, the ΣΔ modulator in PLL2 operates at 1 GHz, achieving a large oversampling ratio. This ensures a small phase noise contribution up to tens of megahertz offset frequency (Section 4.4.3). However, the trade-off between the VCO noise contribution and the ΣΔ noise contribution drives us to find an optimum loop bandwidth.

As derived in [25], the phase noise at divider output can be expressed as:

$$S_Q(f) = \frac{\pi^2}{3N^2 f_{REF1}} \cdot \frac{1}{[2\sin(\pi f T_{REF1})]^2} |NTF(f)|^2,$$

where NTF(f) denotes the noise transfer function of the third-order ΣΔ modulator and will be discussed in Section 4.4.3. Therefore, the output phase noise contribution from the ΣΔ modulator is:

$$S_{Q-out}(f) = S_Q(f) \cdot \left| \frac{NH_{open}(j2\pi f)}{1 + H_{open}(j2\pi f)} \cdot \frac{1 + e^{-j2\pi f T_D}}{2} \right|^2.$$

Now we can calculate the total integrated noise at the PLL output due to VCO and ΣΔ modulator:

$$\int_0^\infty S_{out}(f)df = \int_0^\infty S_{Q-out}(f)df + \int_0^\infty S_{VCO-out}(f)df.$$

We limit the integration range from 10 kHz to 100 MHz since this region dominates the total phase noise. With a VCO noise shown in Section 4.4.2, a sweep on the loop bandwidth can be done to determine the optimum point.

Figure 4.14 indicates that the optimum bandwidth is around 13 MHz. The prototype design chooses a bandwidth of $f_{REF1}/80$, a number close to this value. Furthermore, the region around the optimum point is relatively flat, meaning the architecture has a high tolerance on PVT variations.

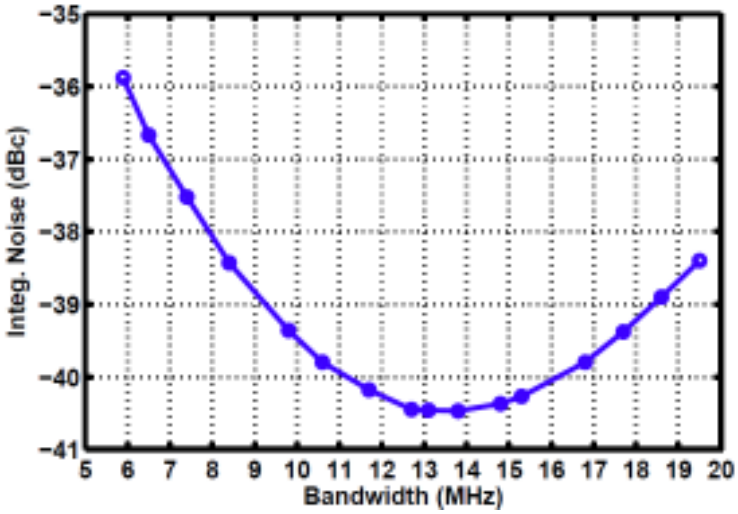

Fig. 4.14. Integrated phase noise versus loop bandwidth for PLL2.

4.4 Circuit Implementations

4.4.1 Noise Trap

The quantization noise peak between the first and the second notch can be reduced by an analog filter. As shown in Figure 4.15, an integrator consisting of G_{m1}, G_{m2} and C_s drives a gyrator load. The gyrator rotates C_L to create an active inductance at node X. Without the front integrator, the active inductance resonates with C_s to form an analog notch filter. With the presence of the integrator, a pole is introduced to bend the high frequency part down.

There are four considerations about this analog filter. First, it must have a high Q to achieve sufficient suppression. Second, it needs to prove wideband filtering. Third, the in-band noise

contribution must be small. Last but not the least, it must accommodate rail-to-rail input common mode (CM) range.

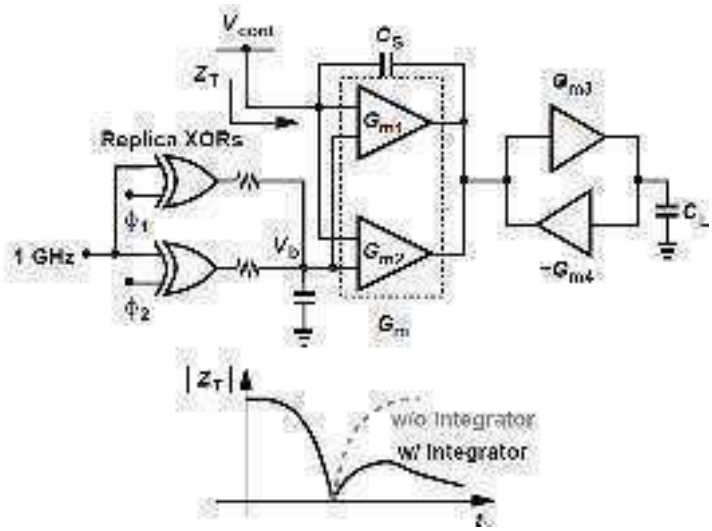

Fig. 4.15. Noise trap topology.

Assume the active inductance is $L = C_L/(G_{m3}G_{m4})$, the input impedance of this trap can be derived as:

$$Z_T = \frac{1 + LC_s s^2}{C_s s(1 + G_m L s)}.$$

Apparently, the notch happens at $1/(2\pi\sqrt{LC_s})$. The pole at $1/(2\pi G_m L)$ provides additional attenuation, making the wideband suppression feasible. The trap implementation is shown in Figure 4.16. The complementary differential pairs at the input can handle almost rail-to-rail CM range. The bias voltage V_b at the CM input comes from a heavily scaled replica path, where its

low-pass corner frequency is only 2 MHz. This voltage tracks the control voltage faithfully without the disturbance from the quantization noise. Also, G_{m4} is programmable such that the notch location can be tuned. In the prototype design, $G_{m1} \approx 0.4$ mS, $G_{m2} \approx 0.4$ mS, $G_{m3} \approx 0.4$ mS, $G_{m4} \approx 0.12$ mS, $C_L = 1.2$ pF, $C_s = 0.1$ pF. Therefore, the active inductance is 25.3 uH with a Q of 20. Loadded by the output impedance of G_{m3} and G_{m4}, the Q drops to around 15. The notch locates at 100 MHz.

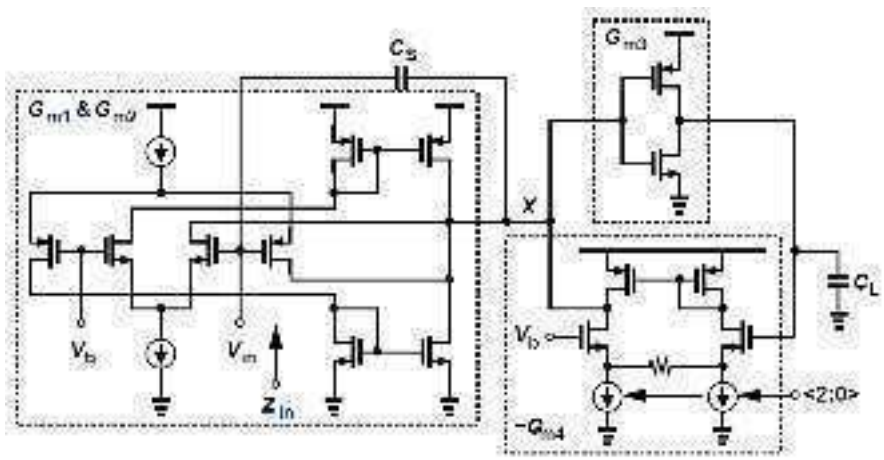

Fig. 4.16. Implementation of analog noise trap.

To calculate the introduced noise voltage on the PLL control terminal, the input noise current density, $\overline{I_{in}^2}$, needs to be derived. Assume the input noise voltage density of these G_m stages are $\overline{V_n^2}$, $\overline{V_{n3}^2}$, $\overline{V_{n4}^2}$, respectively. Then $\overline{I_{in}^2}$ is:

$$\overline{I_{in}^2} = \left(\overline{V_{n3}^2}\left|\frac{G_{m3}G_{m4}}{C_L s}\right|^2 + \overline{V_{n4}^2}G_{m4}^2 + \overline{V_n^2}G_m^2\right)\left|\frac{LCs^2}{1+LCs^2}\right|^2.$$

Thus, the square-root current density is approximately 0.08 pA/$\sqrt{Hz}$ at 5-MHz offset, creating a mean-square voltage density of 0.8 nV/$\sqrt{Hz}$ on the control node. The induced phase noise amounts to -164 dBc/Hz at PLL output. The phase noise contribution from the analog noise trap is negligible because the gyrator absorbs the noise current at low frequencies. Furthermore, the small divide ratio in the second PLL results in a much smaller amplification than the first stage.

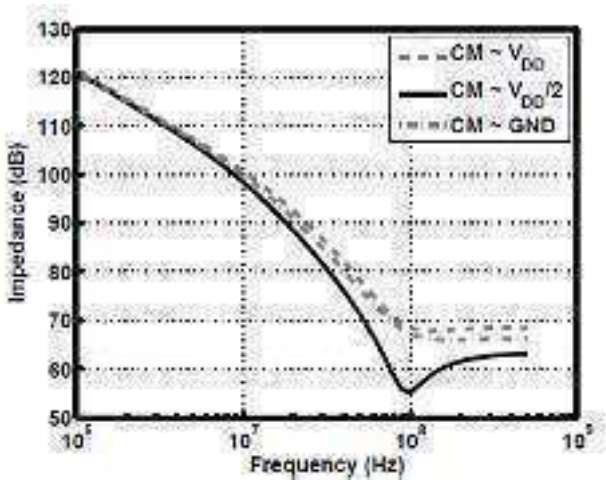

Fig. 4.17. Simulated trap impedance with different input CM levels.

Figure 4.17 plots the simulated trap impedance with different input CM levels. When the input CM level is at $V_{DD}/2$, the attenuation is largest, around 25 dB. It degrades to around 12 dB towards the two supply rails due to the variation of the amplifier gain. Presented on the control node, this impedance alters the loop filter transfer function, bringing in a notch and an additional pole. Shown in Figure 4.18 is the magnitude response of the loop transfer function with and

without the noise trap. The attenuation starts from 50 MHz and continues all the way to 300 MHz with a peak at 100 MHz. Figure 4.19 shows the simulated phase noise from the ΣΔ modulator with and without the noise trap. Apparently, the trap achieves a wideband suppression as predicted from the previous analysis without affecting the loop bandwidth.

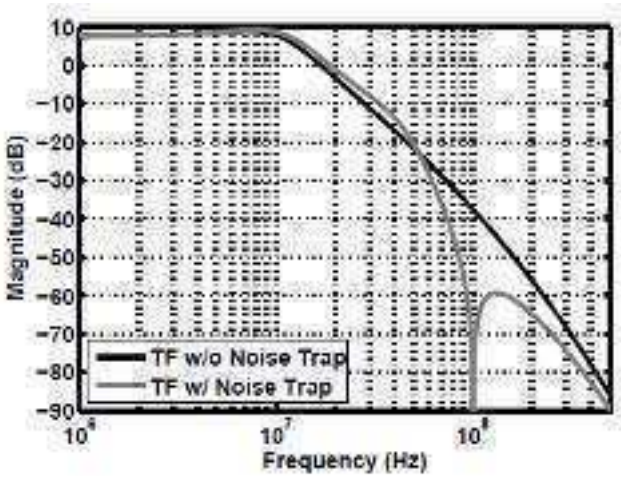

Fig. 4.18. Simulated loop transfer function with and without noise trap.

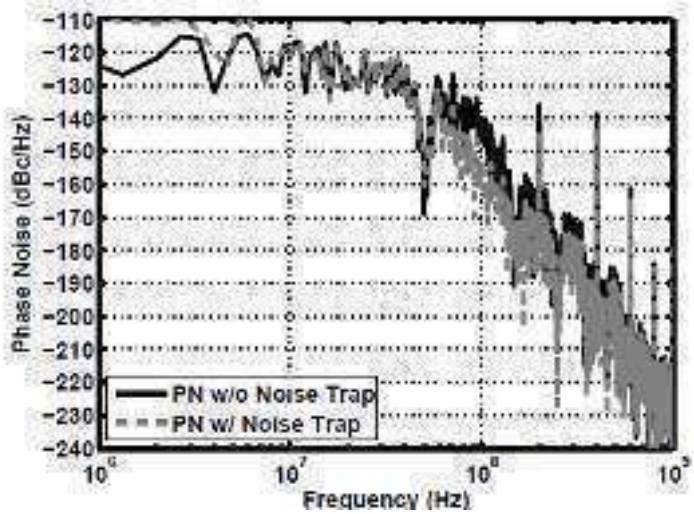

Fig. 4.19. Simulated quantization-noise-induced phase noise with and without noise trap.

4.4.2 VCO Design

VCO2 employs the same topology as VCO1 [5]. Since PLL2 has a wider bandwidth than PLL1, VCO2 can be designed with a higher phase noise and hence a smaller power dissipation. In the prototype design, VCO1 has a K_{VCO} of 120 MHz/V. With 9 discrete capacitor banks, the tuning range is from 900 MHz to 1.1 GHz. VCO1 consumes 2.7 mW at 1 GHz. VCO2 ranges from 2.3 GHz to 2.6 GHz with both continuous and discrete tuning. It consumes 2.25 mW at 2.4 GHz. Their phase noise and K_{VCO} are plotted in Figure 4.20.

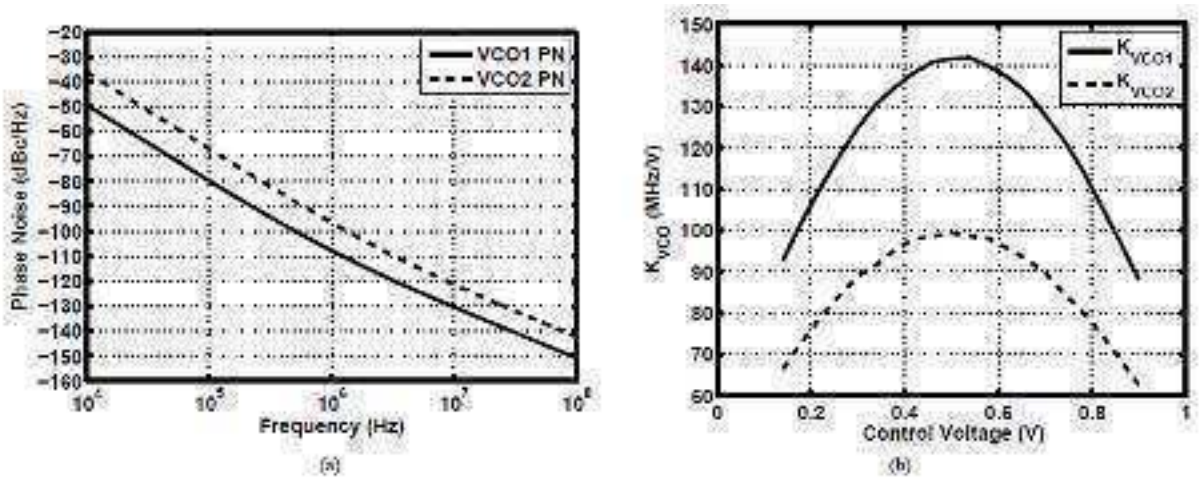

Fig. 4.20. Simulated (a) VCO phase noise, and (b) gain.

The nonlinearity of the VCO gain can potentially cause noise folding. Since PLL1 has a tiny variation on the control voltage at the locked state, the nonlinearity on K_{VCO1} has a negligible effect on the phase noise. PLL2 works in the fractional-N mode, with a control voltage jump of 30

mV_{pp} at the locked stage. This jump experiences the gain nonlinearity, a worst case of ±2.7% when the control is close to the supply rails. Since the quantization noise is already heavily suppressed by the noise filter and loop filter, the noise folding issue causes negligible degradation on the in-band phase noise. Circuit simulations confirm these predictions. The final PLL output phase noise without ΣΔ quantization noise is plotted on Figure 4.21. The in-band noise of PLL1 is around -121 dBc/Hz. After amplifying by PLL2, the noise is increased to -113.4 dBc/Hz. The noise floor of PLL2 is around -117 dBc/Hz. These two adds up to -111 dBc/Hz at the final PLL output. As simulated in Section 4.4.1, the in-band noise contribution of the ΣΔ modulator is approximately -120 dBc/Hz, rising the final PLL output noise floor to -110.5 dBc/Hz.

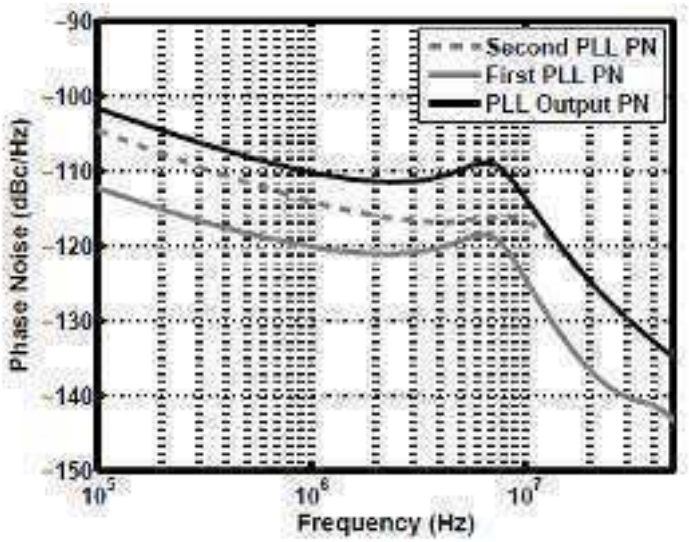

Fig. 4.21. Simulated PLL phase noise without ΣΔ quantization noise.

4.4.3 Low Power Digital Design

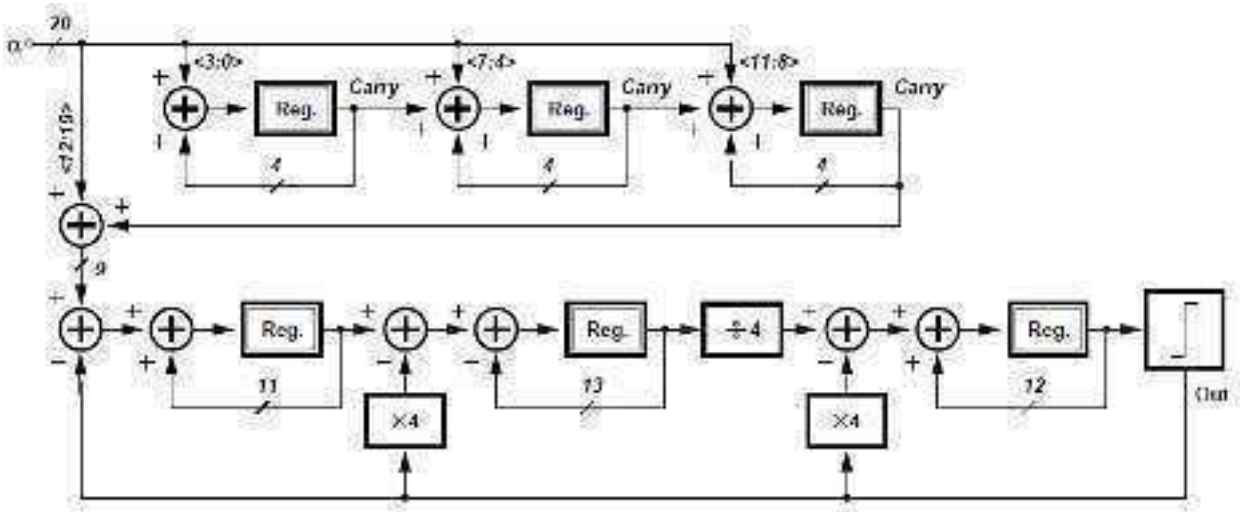

Fig. 4.22. ΣΔ modulator architecture.

A third-order ΣΔ modulator is chosen in the prototype design for its low in-band noise contribution. Since f_{REF1} is approximately 1 GHz, the frequency control word needs to have 20-bit length so as to achieve a frequency resolution of 1 kHz. This results in a large power consumption in the registers and adders. Instead, we employ the bus-splitting technique [24], [26] to save hardware and power. As shown in Figure 4.22, the input drives a cascade of three first-order modulators, which generate a partially-shaped output. This output is added to the input MSBs, <12:19>, and applied to a single-loop third-order modulator. The LSB generated by the cascade modulators works as a dither signal, eliminating strong fractional spurs. The simulated output spectrum is shown in Figure 4.23 for an input of 0.4. Note that the spectrum flattens out at around 50 MHz,

which is different from the $(1-z^{-1})^3$ shape. This is because the quantization noise experiences a function of

$$NTF = \frac{(1-z^{-1})^3}{1+z^{-1}-4z^{-2}+2.25z^{-3}}.$$

The above single-loop modulator can accommodate an input range of 0.25 - 0.75, which is sufficient for the cascaded architecture. This range avoids the integer boundary and results in a better fractional spur performance. All registers used are resettable TSPC FFs to save power. The entire ΣΔ modulator consumes only 500 uW at 1-GHz frequency.

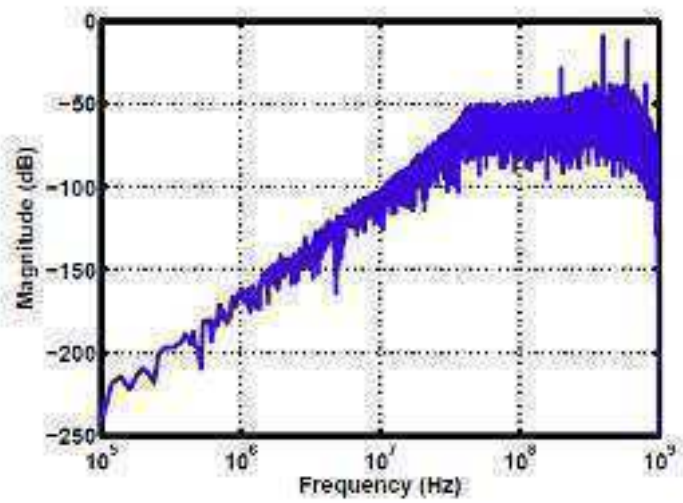

Fig. 4.23. Simulated spectrum of ΣΔ modulator.

CHAPTER 5

Experimental Results

This chapter will show the experimental results for two synthesizer chips. The first one is a 2.4-GHz integer-N inductorless synthesizer and the second one is a 2.4-GHz fractional-N inductorless synthesizer.

5.1 Measurement Results of the 2.4-GHz Integer-N Synthesizer

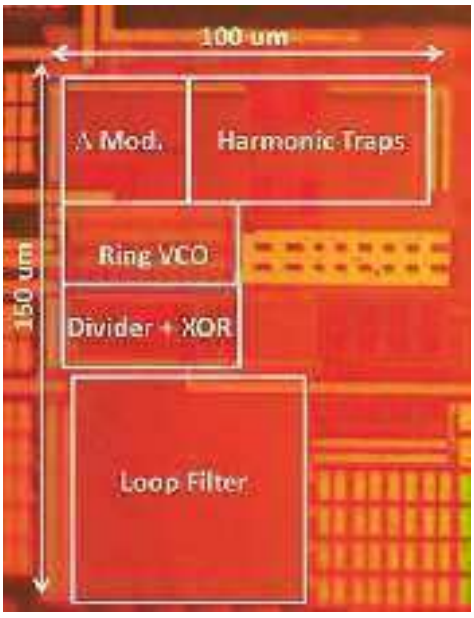

Fig. 5.1. Die micrograph of the integer-N synthesizer.

The integer-N synthesizer has been fabricated in the TSMC 45-nm digital CMOS technology. As shown in Figure 5.1, the die measures 100 um × 150 um. Tested with a 1-V supply, the

synthesizer operates from 2 GHz to 3 GHz and consumes 4 mW at 2.4 GHz. The 22.6-MHz input reference is produced by a low-noise crystal oscillator (hence the departure from 20 MHz) and the output is measured by an Agilent spectrum analyzer. The Δ modulator output is sent off-chip and processed in Matlab, and the control codes are written back to the chip through a serial bus.

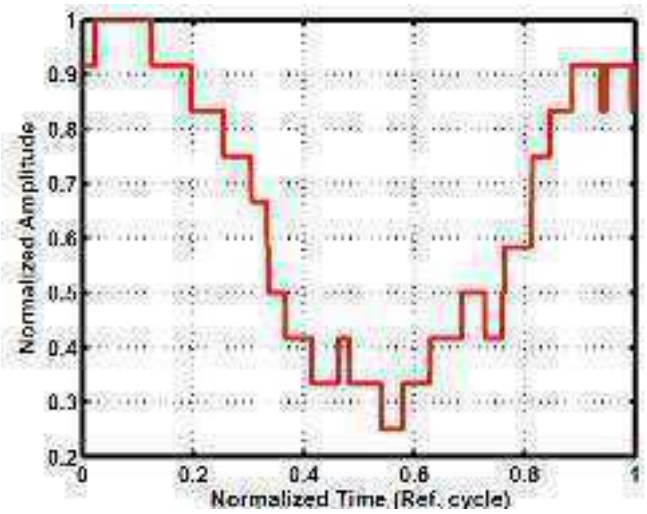

Fig. 5.2. Reconstructed ripple waveform as sensed by Δ modulator.

Upon power-up, the PLL locks with the harmonic traps off and then the traps are turned on and calibrated. The initial calibration takes approximately 400 input cycles, but for subsequent frequency changes (initiated by a modulus change), the calibration settings remain constant because the notch frequencies do not depend on the output frequency. Figure 5.2 shows the reconstructed control voltage ripple waveform as sensed by the Δ modulator. The output spectra

of the synthesizer with the harmonic traps off and on are plotted in Figure 5.3. The first-order spur falls from -47 dBc to -65 dBc, and the second-order spur falls from -55 dBc to -68.5 dBc. The measured phase noise is shown in Figure 5.4. The in-band phase noise reaches -114 dBc/Hz. Integrated from 1 kHz to 200 MHz, the integrated jitter is equal to 0.97 ps_{rms}, which satisfies the IEEE 802.11 b/g standard. For all coarse VCO settings from 2 GHz to 3 GHz, the loop is observed to lock.

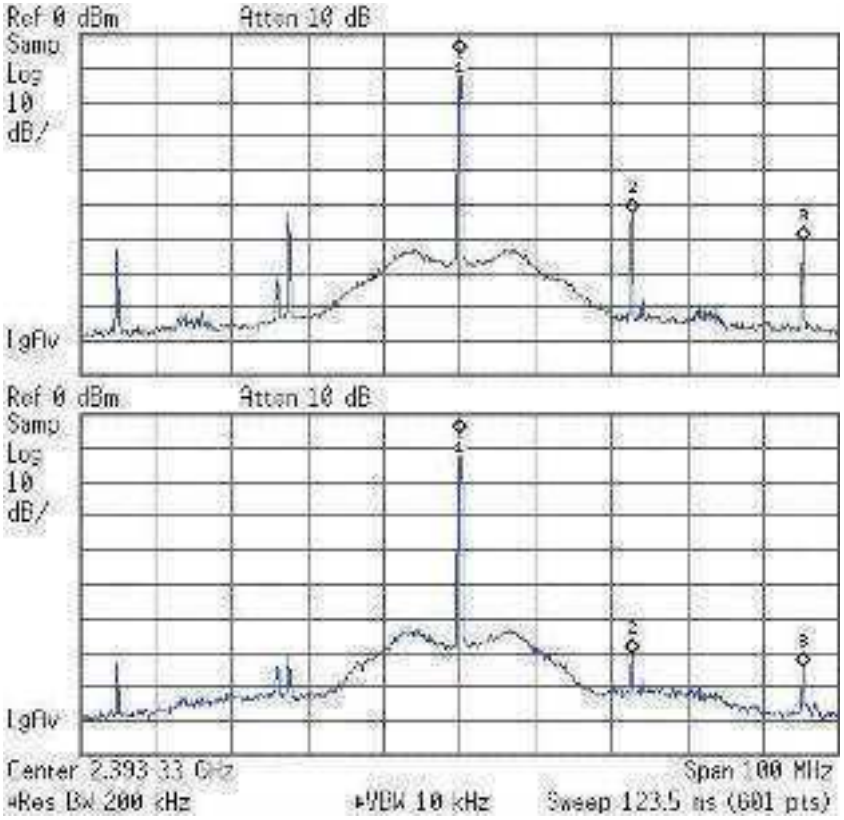

Fig. 5.3. Measured output spectrum with harmonic traps turned off (top) and turned on (bottom).

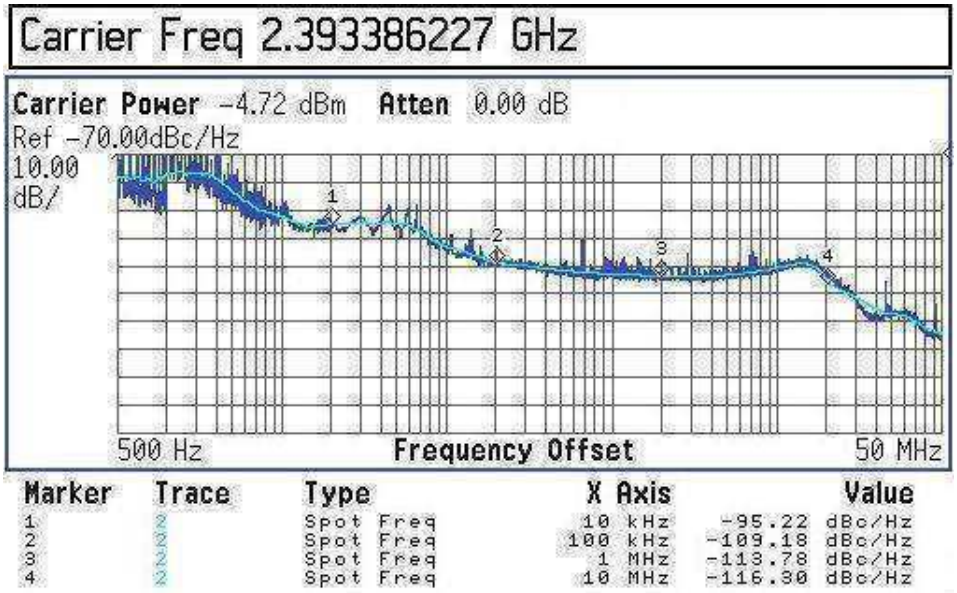

Fig. 5.4. Measured integer-N synthesizer phase noise.

The measurement is also done with different supply voltages (0.95V, 1.05V). After re-calibration, the worst-case reference spur is -62 dBc while the worst-case jitter is 1.14 ps_{rms}. Among five measured chips, the phase noise plateau varies by about 1 dB. Table 5.1 summarizes the performance of our design and compares it to recently reported synthesizers in the range of 2.3 GHz to 3.1 GHz. The proposed synthesizer achieves an FoM of -234.1 dB based on the integrated jitter and an FoM of 175.4 dB based on the phase noise.

	ISSCC'12 [16]	ISSCC'14 [17]	ISSCC'14 [18]	This Work
Oscillator Topology	Ring	Ring	LC	Ring
Reference Freq. (MHz)	36	26	48	22.6
Output Freq. (GHz)	3.1	2.4	2.3	2.4
Phase Noise @ 1 MHz offset (dBc/Hz)	−98	−94	−117	−113.8
RMS Jitter (ps) Integ. range (MHz)	2.23 (N/A)	3.29 (0.01~40)	0.3 (0.01~30)	0.97 (0.001~200)
Ref. Spur (dBc)	N/A	−75	−55	−65
Power (mW)	25.8	6.4	17.3	4
Area (mm^2)	0.32	0.013	0.75	0.015
Tech. (nm)	65	40	180	45
FoM_1 (dB)	−218.9	−221.6	−238	−234.1
FoM_2 (dB)	153.7	153.6	171.9	175.4

$$FoM_1 = 10\log_{10}\left[\left(\frac{\text{Jitter}}{1\,s}\right)^2\left(\frac{\text{Power}}{1\,mW}\right)\right] \quad FoM_2 = 10\log_{10}\left[\left(\frac{f_{osc}}{\Delta f}\right)^2\left(\frac{1\,mW}{\text{Power}}\right)\right] - \text{Phase Noise (dBc/Hz)}$$

Table 5.1. Performance summary of the integer-N synthesizer.

5.2 Measurement Results of the 2.4-GHz Fractional-N Synthesizer

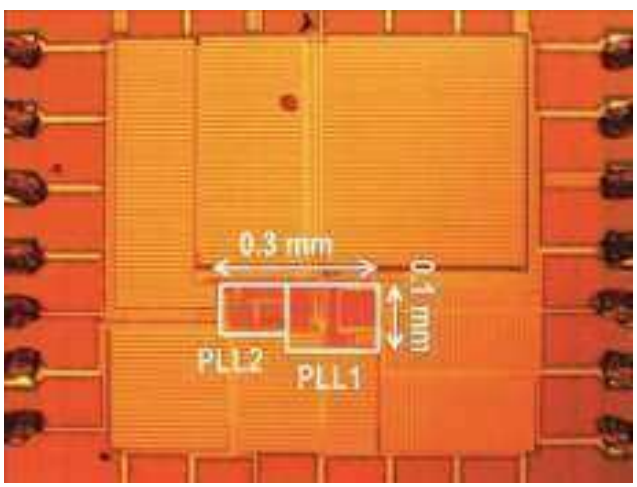

Fig. 5.5. Die micrograph of the fractional-N synthesizer.

The cascaded synthesizer has been fabricated in TSMC 45-nm digital CMOS technology. Shown in Figure 5.5 is the die micrograph. Its active area measures 300 um × 100 um. The prototype

takes a 22.58-MHz crystal oscillator as a reference, and generates an output frequency from 2.3 GHz to 2.6 GHz. Tested with a 1-V supply, the power consumption is 6.4 mW: 3.1 mW in the first PLL and 3.3 mW in the second PLL. Figure 5.6 shows the measured output spectra before and after the noise filter and noise trap are turned on. In this test, the first PLL has a divide ratio of 45 while the second has a fractional division of roughly 2.3346. As can be seen, the phase noise suppression starts from 20-MHz offset and reaches 17 dB at 50-MHz offset. The highest reference spur lies at $2f_{REF}$ offset and has a magnitude of -70 dBc. Figure 5.7 shows the spectra when the integrated noise is smallest. In this scenario, 4-dB peaking is observed at the edge.

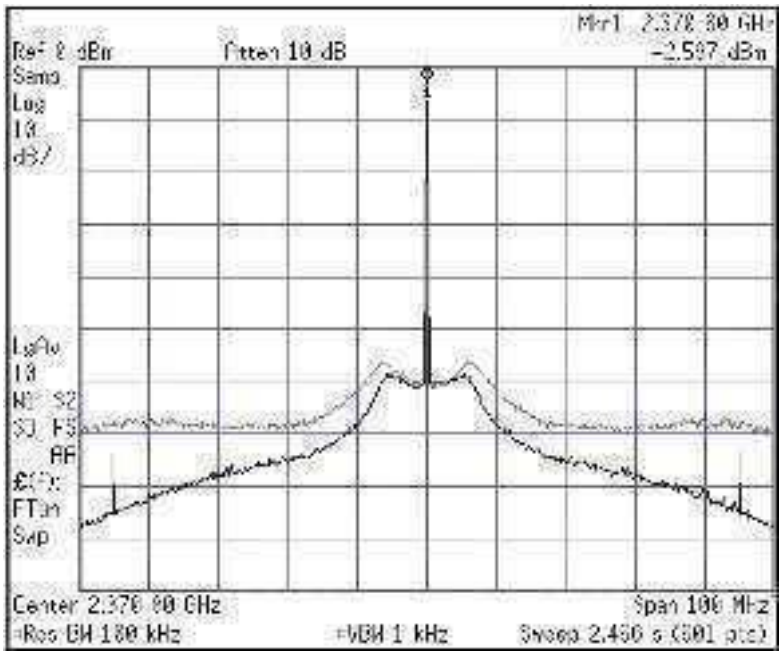

Fig. 5.6. Measure output spectra before and after noise filter and noise trap are turned on.

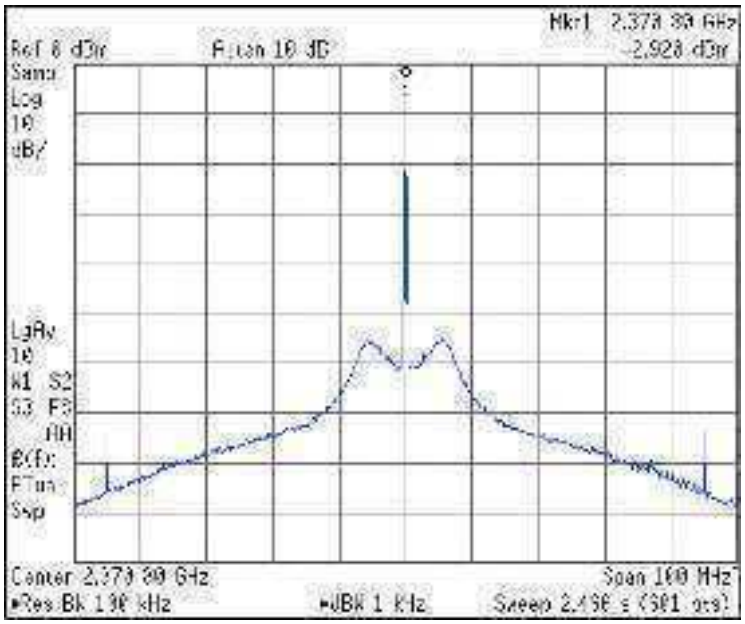

Fig. 5.7. Measured output spectrum with smallest integrated noise.

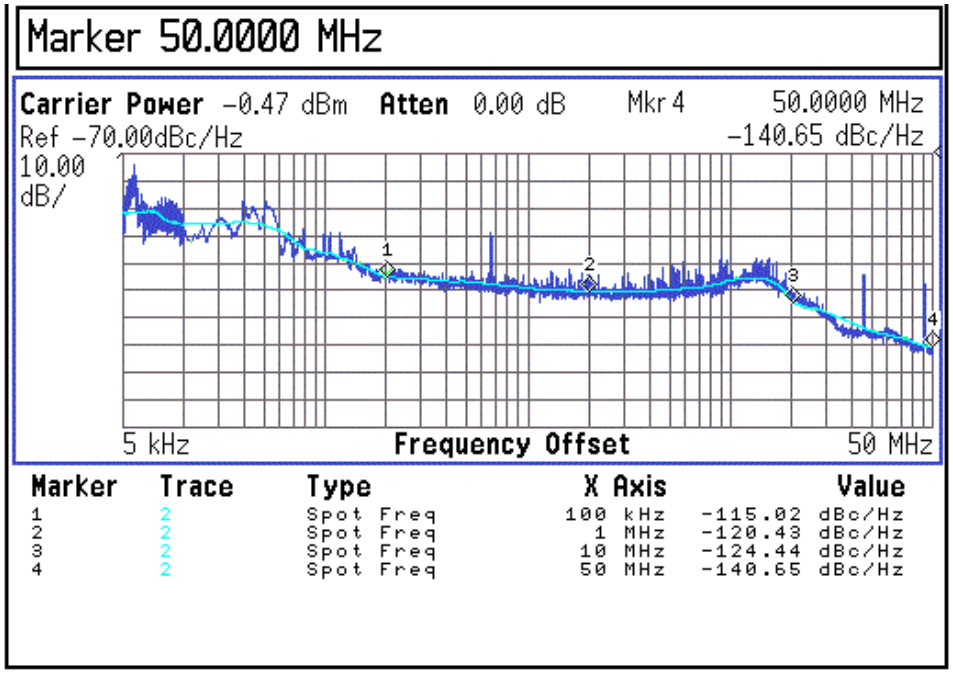

Fig. 5.8. Measured first PLL phase noise.

Figure 5.8 plots the measured phase noise of the first PLL. Its in-band noise is around -120.4 dBc/Hz. Figure 5.9 shows the measured PLL output phase noise. The in-band plateau is -109 dBc/Hz and the integrated jitter from 10 kHz to 50 MHz is equal to 1.68 ps_{rms} (rising to 2.8 ps_{rms} if the all the techniques are off). Also plotted in Figure 5.10 is the fractional spur level as a function of the fractional offset. The spur levels satisfy both IEEE 802.11 a/g and Bluetooth blocking requirements. Table 5.2 summarizes the performance of our design and compares it to recently reported synthesizers in the range of 1.9 GHz to 2.4 GHz. Compared to other ring-based fractional-N designs, the proposed synthesizer achieves the best FoM of -227.4 dB based on the integrated jitter.

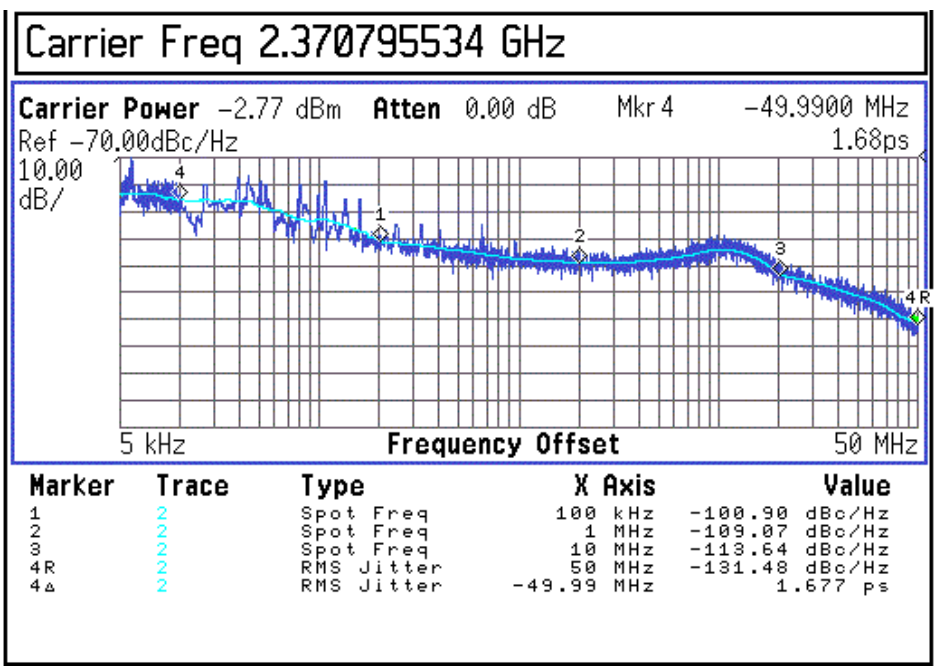

Fig. 5.9. Measured fractional-N synthesizer output phase noise.

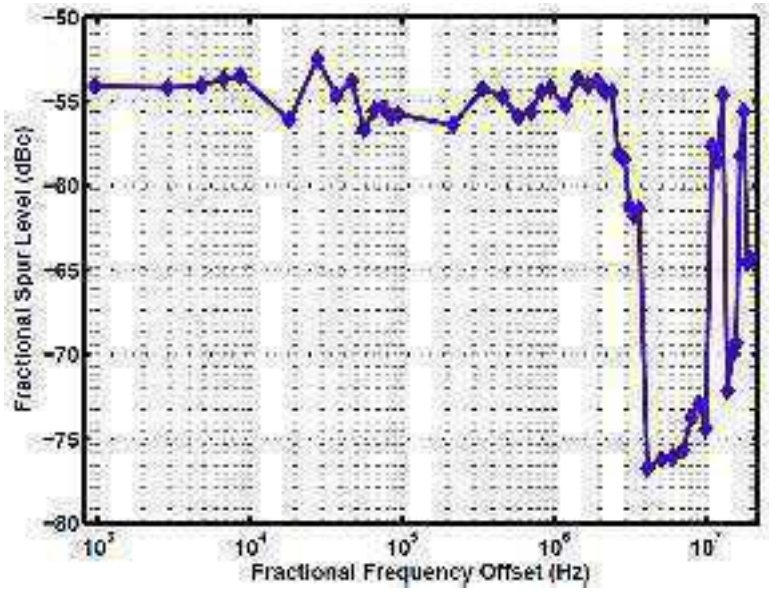

Fig. 5.10. Measured fractional spur versus fractional frequency offset.

	ISSCC'13 [27]	ISSCC'14 [18]	ISSCC'15 [22]	This Work
Oscillator Topology	Ring	LC	Ring	Ring
Reference Freq. (MHz)	26	48	26	22.6
Frequency Range (GHz)	1.87 ~ 1.98	2.2 ~ 2.4	2	2.3 ~ 2.6
Phase Noise @ 1MHz offset (dBc/Hz)	−98	−117	−98	−109
RMS Jitter (ps) Integ. range (MHz)	3.4 (0.004~2)	0.3 (0.01~30)	2.36 (0.001~40)	1.68 (0.01~50)
In-band Frac. Spur (dBc)	−50	−53	−70	−52.5
Ref. Spur (dBc)	−67	−55	−87	−70
Power (mW)	10	17.3	9.1	6.4
Area (mm^2)	0.047	0.75	0.046	0.03
Tech. (nm)	40	180	40	45
FoM_1 (dB)	−219.4	−238	−223	−227.4
FoM_2 (dB)	153.9	171.9	154.4	168.4

$FoM_1 = 10\log_{10}[(\frac{Jitter}{1\ s})^2(\frac{Power}{1\ mW})]$ $FoM_2 = 10\log_{10}[(\frac{f_{osc}}{\Delta f})^2(\frac{1\ mW}{Power})] - Phase\ Noise\ (dBc/Hz)$

Table 5.2. Performance summary of the fractional-N synthesizer.

CHAPTER 6

Conclusion

This dissertation presents both an integer-N and a fractional-N inductorless synthesizer architecture for 2.4-GHz RF applications. A spur reduction approach based on harmonic traps is also introduced that measures the ripple on the control voltage by means of a Δ modulator and, using a three-point algorithm, forces the ripple to minimum. To reduce the quantization noise in the fractional-N loop, a synchronous delay-line-based noise filter and an analog noise trap are proposed to allow a wideband operation.

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