Reconfigurable and Simultaneous Dual Band Galileo/GPS Front-end Receiver in 0.13μm RFCMOS

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Abstract- **A reconfigurable and simultaneous dual band Galileo/GPS front-end receiver has been realized on 0.13-μm RFCMOS technology. The front-end uses only one fixed frequency PLL and VCO on a superheterodyne architecture to down-convert two RF (Radio Frequency) signals into two IF (intermediate frequency) signals in the range of 50MHz to 150Mhz. L1 and E1 signals are directly converted on one channel with one mixing stage. L2, E6, E5, E5a, E5b signals are down-converted with a double stage (two mixers) conversion.**
The two IF down-converted channels are filtered and then undersampled by two on chip ADC (Analog to Digital Converter). The satellite channels can be selected and reconfigured only by changing the ADC sampling frequency according to the frequency plan and the off chip RF/IF filters. No PLL and VCO reconfiguration is need.

INTRODUCTION

Galileo is the European global navigation satellite system, providing a highly accurate, guaranteed global positioning service under civilian control. It is inter-operable with GPS and GLONASS, the two other global satellite navigation systems. Galileo system has a widely bands availability compared to GPS system. GPS only transmits on the so called L1 band (about 1.5GHz) for civil applications and on the so called L2 band (about 1.2GHz) for military applications.

Galileo satellite navigation program is promoted by the European Union and the European Space Agency to reduce the Europe's dependency on the US GPS or Glonass. Four bands exist in Galileo: E5a (1176.45 MHz), E5b (1207.14), E6 (1278.75 MHz) and L1-E1 (1575.42 MHz).

The four frequency bands (E5a, E5b, E6 and L1-El) used provide a large bandwidth for transmission of the Galileo Signals, and allowing an efficient use of the Radio-Navigation Satellite Services (RNSS) allocations.

All Galileo transmitting Satellites, making use of Code Divided Multiple Access (CDMA), will share the same frequency bands. Spread Spectrum signals will be transmitted including different Ranging Codes per signal and for each Galileo Satellites. They will he transmitted in Right-Hand Circular Polarization (RHCP).

This paper describes the design of a front-end receiver IC realized in a 0.13μm RF CMOS technology, operating on all Galileo and GPS frequencies and able to receive such bands on two simultaneous channels (i.e. L1 & E6 or L1 & E5a, L1 & E5b, L1 & E5 L1 & L2).

RECEIVER ARCHITECTURE

The receiver architecture proposed is a superheterodyne and it is the most widely used reception technique. It comes in a variety of combinations, but essentially relies on the same idea: the RF signal is first amplified in a frequency selective low-noise stage, then translated to a lower intermediate frequency (IF), with significant amplification and additional filtering, and finally down-converted to baseband.

One of the main goals of the receiver is to perform the down-conversion not only of the upper-bands (E1, L1) but also of the lower-bands (L2, E5, E5a, E5b, E6) and furthermore the reception needs to be simultaneous.

Looking to the spectrum it can be seen that the main lobe of E5, E6 is wider compare to that of upper-band (L1, E1). The E5, E6 main lobe bandwidth is in the range of 40-50MHz instead of 2-6MHz of the L1, E1 ones as shown in Figure 1.
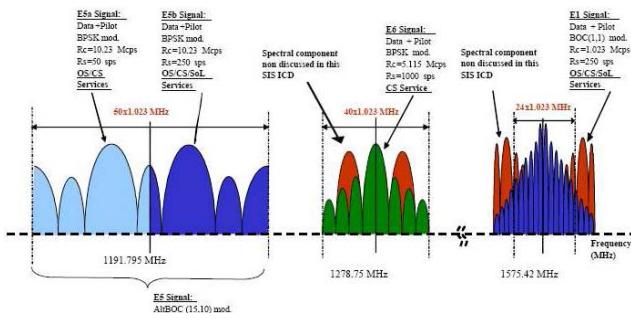
Figure 1 Galileo frequency spectrums

This translates in tailoring a classical superheterodyne approach since a Low-IF would suffer of limited image-rejection and higher power consumption.

In order to choose a common architecture solution for upper and lower Galileo bands the superheterodyne even if not the most integrated architecture is the best compromise.

In fact it is able to handle wider E5 and E6 main lobes and it allows the use of only one VCO for simultaneously operation for both upper and lower bands.

It is here reported a frequency plan that shows how it is possible to use only a common LO frequency.

Band	Carrier (MHz)	IF1 (MHz)	IF2 (MHz)	Flo	DIV	BW (MHz)
L2	1227,60	117,18		1110,42		10,00
E6	1278,75	168,33		1110,42		20,00
Ea5	1176,45	66,03		1110,42		25,00
Eb5	1217,14	106,72		1110,42		25,00
L1/E1	1575,42	465,00	94,86		3,00	6,00

Figure 2 Frequency plan

Figure 3 shows the receiver architecture with the main building blocks.

As shown the receiver is composed by some external components, basically passive filters and VGA and integrates the following functional blocks: RF Amplifier, Mixer 1, Mixer 2, IF Amplifier, VCO/PLL and ADCs.

It has to be highlight that the front-end rely on an external LNA (active antenna) thus relaxing the noise figure requirements of the IC.

In the following paragraph will be described in more details the main integrated building blocks, divided into different sections.

CHIP DESIGN

A. RF SECTION

The goal of the RF-amplifier is to further amplify the incoming signal in order to reduce the noise contribution of the following stages without degrade too much the system linearity.

The proposed topology is a common source configuration with inductive degeneration (Figure 4).

The input stage has to satisfy the following requirements: source impedance matching, minimum noise contribution, maximum transconductance gain.

Furthermore, the IIP3 (linearity) of the RF Amplifier should be maximized.
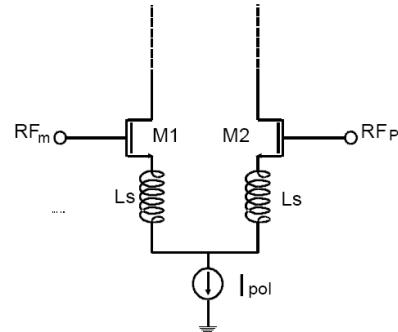
Figure 4 RF Amplifier input stage schematic

Figure 3 Architecture overview

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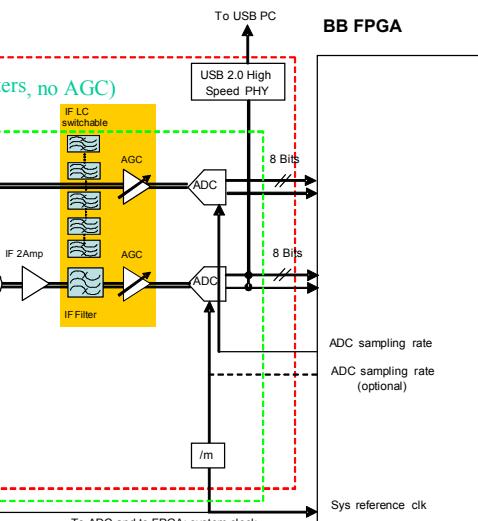
Fig. 4 shows the RF Amp core. M1 and M2 constitute the core of the differential pair and M3 and M4 are the cascode transistors. Addition of M3 and M4 improves the input/output isolation as well as the circuit stability.

Inductors Ls1 and Ls2 are degeneration inductors and they improve the linearity of the circuit. These inductors also change the input impedance of the transistor which is purely capacitive introducing a real part to the input impedance.

The input impedance of the circuit should also be matched to the impedance of the antenna or filter that precedes it. This goal is achieved by designing a matching network for the circuit.

Table I summarizes the main simulation (post-layout simulation with parasitic extraction) results.

Table I RF Amplifier simulation performance

Parameter	Value	Units
Operating Frequency (L1 band)	1575	MHz
Voltage Gain	13.3	dB
Noise Figure	3.8	dB
IIP3	0	dBm
S11	-11.8	dB
Current consumption	5	mA

In Figure 5 it is reported the layout of the block. It can be noticed that the size of the cell is dominated by the integrated inductors.
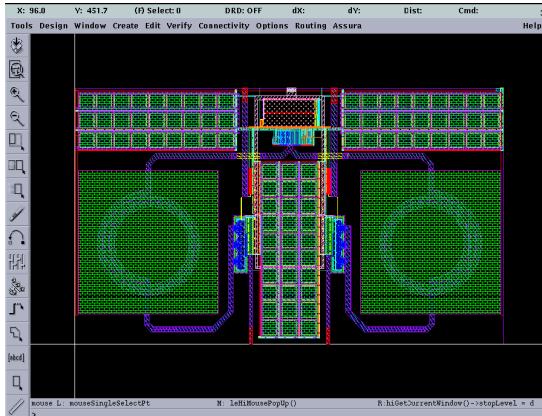
Figure 5 RF-amplifier layout

The mixer follows directly the RF amplifier.

This block has the main task to translate the RF input signal to the intermediate IF frequency. It has been chosen an active mixer approach. The proposed topology is a Gilbert cell like mixer (Figure 6). It can be divided into main sections: the switching stage that represent the Gilbert core and the output stage realized by resistors[1].
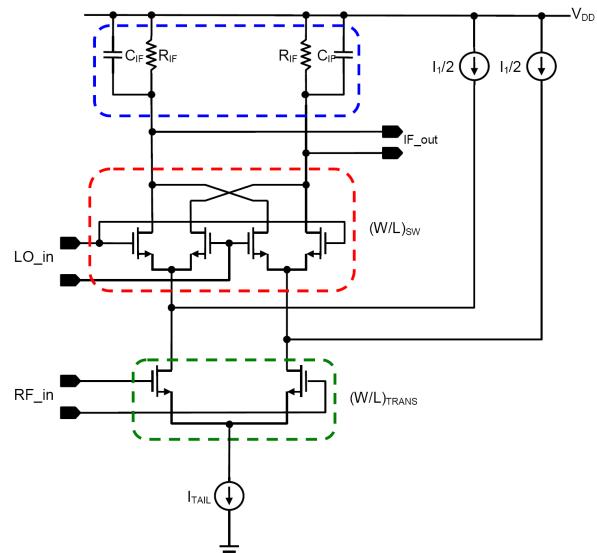
Figure 6 Mixer 1 schematic

The switching stage has been sized taking into account linearity and noise requirements.

The same topology of the Mixer 1 is still valid for the second mixer, named Mixer 2, used in the upper band receiver chain. The main difference is represented by the input impedance that in this case should be matched with the external SAW filter. For the input matching it is suggested to use a transconductance stage in front of the switching pairs to allow together with external components the input impedance of 50 Ohms.

B. PLL

The PLL integrates a Phase Frequency Detector (PFD), a Low Pass Filter (LPF), a Voltage Controlled Oscillator and other associated circuit.

In Figure 7 is reported the basic structure.
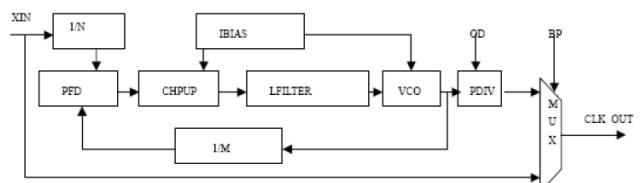
Figure 7 PLL block diagram

In Table II it is reported the main PLL characteristic.

Table II PLL main characteristic

Parameter	Symbol	Min	Typ	Max	Unit
Input clock frequency	XIN/N	5		50	MHz
VCO frequency	VOUT	800		1600	MHz
Output clock frequency	CLK_OUT	100		1600	MHz
Duty cycle		40		60	%

C. IF Section

Within the chain of dual-band Galileo/GPS receiver, the Intermediate Frequency Amplifier (IFA) is placed after the down conversion of Radio Frequency (RF) by mixing it with the Local Oscillator (LO).

The architecture chosen is fully-differential, because of its better immunity from the power-supply noise and its intrinsic lower distortion with respect to the single-ended (absence of even order harmonics [2]). In particular, the output impedance of the IFA should be well defined in order to match with the characteristic impedance of the external IF SAW filter that follows. Furthermore, the IFA stage should provide a linear transfer function within the interval of interest for input saturation region (non-linear behaviour). In other words, given the I_{bias} current (e.g., from static power constraints) and the range of variability for differential input signal for a specific application, R_1 must be chosen higher than the minimum value expressed as follow:

$$R_1 > R_{1,min} = \frac{\Delta V_{in}|_{max}}{I_{bias}}$$

For a non-saturated IFA, the formula of differential voltage gain can be easily obtained by observing the circuit in Figure 8. A current signal ΔI is generated by the differential input signal ΔV_{in} ($\Delta V_{in} = \Delta V_{in}/R_1$) and subtracted (added) to drain-source current of M3 (M7). Next, given the two current mirrors M3-M4 and M7-M8, current signals are mirrored and amplified by m factor (current mirror gain) to the output stages. Multiplying both output currents signals by R_2 and expressing the output differential voltage signal $\Delta V_{out} = \Delta V_{outP} - \Delta V_{outN}$ as a function of differential input signal, one can get the differential voltage gain:

$$A_v = 2\, m\, \frac{R_2}{R_1}$$
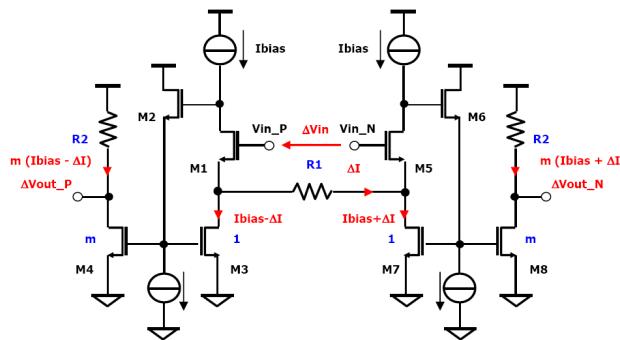
Figure 8. IFA simplified schematic

Within IFA stage, transistors are properly sized to satisfy noise, bandwidth and linearity requirements. Table III compares the

differential signals (ΔV_{in} (t)$\in$ [-90 mV, +90 mV] for this application).

Figure 7 shows the circuit which meets the above cited requirements, where the biasing details are removed for simplicity. Considering the left half circuit (the same discussion can be done for the right half thanks to the symmetry), transistors M1, M2 and M3 form a linearized voltage buffer that, through the mechanism of feedback, causes a constant current flowing from drain to source in M1. As a result, the input differential voltage experiences a nearly constant level shift and it is placed across R1. This is true until the peak current flowing through R_1 is lower than I_{bias} ($I_{R1, max} = \Delta V_{in, max}/R1 < I_{bias}$). When $I_{R1, max}$ reaches Ibias, the feedback breaks down and the amplifier enters in target values of important parameters from specifications with the actual ones.

Table III. IFA target and simulation performance

Parameter	Target	Simulation	Units
Frequency of operation	50-200	1-205	MHz
Gain	10	20	dB
Noise Figure	20	16-18	dB
IIP3	5	0.5	dBm
Current consumption	3	2.5	mA

In Figure 9 it is reported the layout of the block.
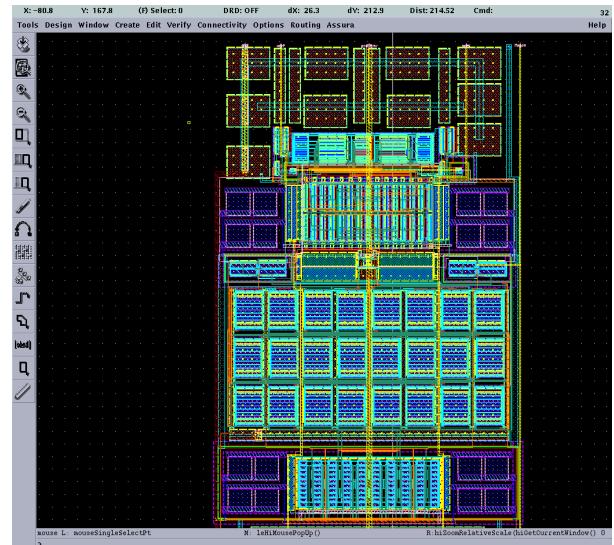
Figure 9 IF-amplifier layout

After channel selection, realized by IFA stage, it is needed the digitization of the signal. Due to very limited dynamic range of the Galileo signal no more than four bits would be required [3]. Looking into details the system frequency plan it can be seen that it is convenient to use an undersampling technique. When a signal is sampled at less than the Nyquist rate, the aliased signal appears at fs – fi, where fs is the sampling frequency and fi is the frequency of the input signal. The integrated ADC is a

pipeline 6-stage architecture that consumes 25mA while delivering a 45dB Signal to Noise Ratio Plus Distorsion (SINAD) at 60MHz.

SUMMARY RESULTS

A chip prototype in an RF 0.13μm CMOS technology (Figure 10) has been integrated. It has an active area of 20mm^2, due to some test structures, but can be optimized and consumes roughly 100mW. The chip will be tested on a 4 layers FR4 test-board. On the same board a preliminary proof of concept of the proposed receiver architecture was realized with discrete commercial components.

The overall expected conversion gain is about 50dB for both bands and the RFIC Noise figure is expected to be lower than 10dB.

In the Table IV table is reported the performance of E5/E6 path of the receiver chain simulated with parasitic extraction.

Figure 10. Chip Layout

Table IV. E5/E6 Receiver path simulation results

Parameter	Value	Units
Input frequency	1176 - 1278	MHz
Output frequency	66 - 168	MHz
Conversion-Gain @ Mixer output	27.9 @100MHz	dB
Conversion-Gain @ IFAmp output	46@100MHz	dB
Noise Figure (total)	8	dB
P1dB @ Mixer output	-25	dBm
IIP3 @ Mixer output	-15	dBm

CONCLUSIONS

A reconfigurable and simultaneous dual band Galileo/GPS front-end receiver on 0.13-μm RFCMOS has been presented.

It is highlighted that is based on a robust superheterodyne architecture and that it is using only one VCO for all bands simultaneously reception.

REFERENCES

[1] D. Leenaerts and W. Readman-White, "1/f noise in   passive CMOS mixer for low and zero IF integrated receivers" in Proceedings of 27th European Solid-State Circuits Conference, 2001.

[2] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2001.

[3] D. Shaeffer et al., "A 115 mW, 0.5 _m CMOS GPS   receiver with widedynamic-range active filter," IEEE J.Solid-State Circuits, vol. 33, no.12, pp. 2219–2231, Dec. 1998.

[4] J. Kim, S. Cho, and J. Ko, "L1/L2 dual-band GPS receiver," in Proc. Eur.Solid-State Circuits Conf., 2004, pp. 87–90.

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