Replica Compensated Linear Regulators for Supply-Regulated Phase-Locked Loops

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***Abstract*—Supply-regulated phase-locked loops rely upon the VCO voltage regulator to maintain a low sensitivity to supply noise and hence low overall jitter. By analyzing regulator supply rejection, we show that in order to simultaneously meet the bandwidth and low dropout requirements, previous regulator implementations used in supply-regulated PLLs suffer from unfavorable tradeoffs between power supply rejection and power consumption. We therefore propose a compensation technique that places the regulator's amplifier in a local replica feedback loop, stabilizing the regulator by increasing the amplifier bandwidth while lowering its gain. Even though the forward gain of the amplifier is reduced, supply noise affects the replica output in addition to the actual output, and therefore the amplifier's gain to reject supply noise is effectively restored. Analysis shows that for reasonable mismatch between the replica and actual loads, regulator performance is uncompromised, and experimental results from a 90 nm SOI test chip confirm that with the same power consumption, the proposed regulator achieves at least 4 dB higher supply rejection than the previous regulator design. Furthermore, simulations show that if not for other supply rejection-limiting components in the PLL, the supply rejection improvement of the proposed regulator is greater than 15 dB.**

***Index Terms*—Phase-locked loops, power supply noise, regulators.**

I. Introduction

As SUPPLY to threshold voltage ratios have decreased, supply-regulated phase-locked loops (PLLs) using CMOS buffers, as proposed by von Kaenel *et al.* [1] and extended for adaptive bandwidth by Sidiropolous *et al.* [2], have become attractive because of their relaxed headroom requirements and simple VCO buffer design (Fig. 1). For the loop to achieve low jitter, particularly in harsh mixed-signal environments, the linear regulator driving the VCO must maintain high supply rejection across a broad range of frequencies. Since the regulator represents additional poles in the PLL, to maintain stability the regulator bandwidth must be kept well above the closed-loop bandwidth of the PLL. Finally, allowing the VCO supply voltage to be as high as possible maximizes its attainable operating frequency, and hence the regulator must have a low dropout voltage.

Low dropout regulators are typically implemented as shown in Fig. 2. The common-source pMOS output stage uses a low overdrive to maintain a low dropout, which leads to a large output device. If an amplifier with high output impedance—such as a current mirror loaded differential pair shown in the inset of Fig. 2—is used, a relatively low-frequency pole will result from the large input capacitance (C_{gate}) of the output stage. This pole is in addition to the pole formed at the supply of the VCO, which will also be low in frequency due the large decoupling capacitance used to suppress VCO switching noise and power supply noise. Therefore, regulators of this type have two closely spaced poles, and require compensation circuitry to stabilize the regulator feedback loop.

While many techniques (such as Miller or RC compensation [3]–[5]) exist to stabilize a loop that nominally has two closely spaced poles, these techniques usually achieve stability by lowering the amplifier bandwidth. Unfortunately, as will be shown in the following section, lowering the bandwidth of the amplifier reduces the gain available to the regulator to suppress supply noise at midrange frequencies where the attenuation of the output RC filter (formed by C_{decap} and the output resistances at V_{reg}) is still relatively low, causing the dynamic supply rejection of these regulators to suffer.

The regulator topology proposed by Sidiropolous *et al.* in [2] solves the stability problem by generating all of its gain at the output stage, as shown in Fig. 3. However, in order to keep the bandwidth of the transconducting first stage high enough to avoid stability issues and maintain reasonable input referred offsets, the current mirroring ratio (M) must be fairly small, causing this topology to have high power dissipation (typically 3–5 times the VCO current [2], [6]).

To compensate the regulator without sacrificing supply rejection or increasing power consumption, we propose the use of a secondary, replica loop to apply negative feedback to the amplifier, lowering its forward gain and increasing its bandwidth, as shown in Fig. 7(c). Since supply noise is common to both the main and replica loops, stability is achieved without reducing the gain available to combat supply noise. This topology makes use of a replica load to track the VCO in order to enhance its performance, and therefore we provide example replica load topologies and examine the effects of mismatch. The proposed regulator has been implemented in a 90 nm SOI technology as

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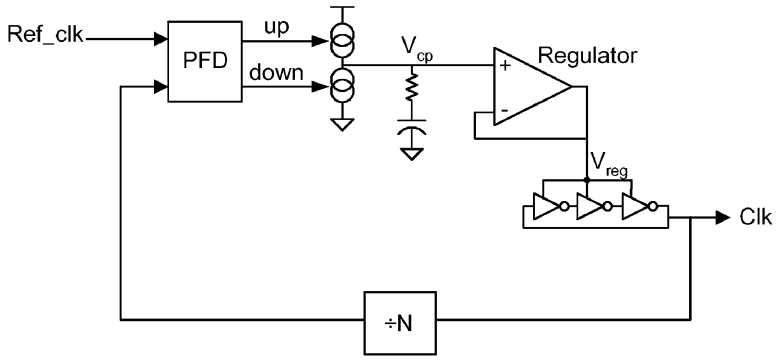

Fig. 1. Supply regulated PLL block diagram. Since the regulator is in the forward path of the PLL, both its dynamics and its drop-out voltage are important for good overall performance.

part of a PLL on a test chip for characterization of the parallel interface described in [7], and experimental results demonstrating improvement in the supply sensitivity of this PLL over the sensitivity of a PLL which made use of the previous regulator design are presented.

II. Regulator Power Supply Rejection

In order to show that previous compensation schemes degrade regulator dynamic power supply rejection, we will examine the supply sensitivity of the general regulator topology from Fig. 2. Throughout the supply rejection analysis in this paper, we will make the simplifying assumption that $V_{\rm bp}$ is perfectly coupled to $V_{\rm dd}$ across all frequencies—in other words, that variations in supply voltage do not directly alter the gate overdrive of the output device (except through the action of the amplifier). In addition, we will also assume that capacitive coupling from $V_{\rm dd}$ to $V_{\rm reg}$ (e.g., through the output device's drain to body capacitance) is negligible. Finally, since $C_{\rm decap}$ is implemented on-chip and minimizing its effective series resistance (ESR) is desirable for high supply rejection (and can be achieved with proper layout techniques), we will not include any ESR in the analysis. These assumptions clearly do not hold for all regulator designs; however, they do not change the insight imparted by the analysis and clarify the supply sensitivity behavior of the regulator.[1]

A simplified small-signal model of the regulator is shown in Fig. 4; g_m and r_o model the transconductance and output resistance of the pMOS output transistor, and $r_{\rm vco}$ models the VCO's linearized output resistance $(dV_{\rm reg}/dI_{\rm vco})$. The transfer function from $V_{\rm dd}$ to $V_{\rm reg}$ can be written as

$$\frac{V_{\rm reg}(s)}{V_{\rm dd}({\rm s})} = \frac{S_{\rm Vdd}(1+s/\omega_a)}{(1+s/\omega_o)(1+s/\omega_a)+A_aA_o} \qquad (1)$$

where the open-loop supply sensitivity $S_{\rm Vdd} = r_{\rm vco}/(r_{\rm vco}+r_o)$ is the resistive voltage divider from $V_{\rm dd}$ to $V_{\rm reg}$, $A_o = g_m(r_{\rm vco}||r_o)$ is the DC gain of the output device, $\omega_o = [(r_{\rm vco}\,||\,r_o)C_{\rm decap}]^{-1}$ is the pole at $V_{\rm reg}$, A_a is the DC gain of the amplifier, and ω_a is the pole of the amplifier. To minimize the area overhead of the regulator, the channel length of the output device is usually kept short, and therefore in advanced technologies $S_{\rm Vdd}$ is often only roughly 1/4 to 1/2.

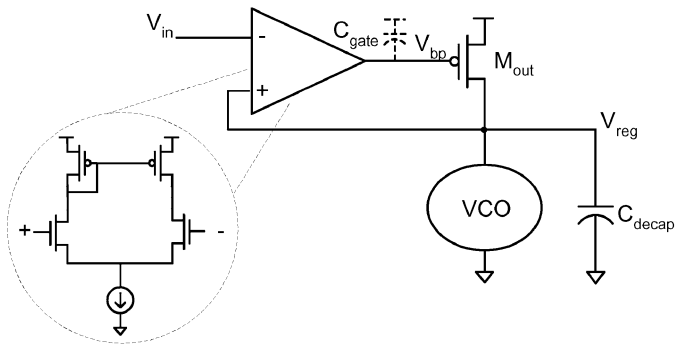

Fig. 2. Low-dropout linear regulator topology with example amplifier implementation. The pMOS device $(M_{\rm out})$ must be large to achieve a low drop-out voltage, which with a high output impedance amplifier creates a relatively low-frequency pole. Regulator stability is an issue because of the interaction of this pole with the pole at the regulator's output (due to $C_{\rm decap}$).

In order to maximize the worst-case supply rejection, the amplifier bandwidth must be as high as possible—preferably high enough that the output pole becomes dominant (i.e., $\omega_o \ll \omega_a$). To clarify this statement, consider two regulators whose transfer functions from $V_{\rm in}$ to $V_{\rm reg}$ are identical; one whose dominant pole is set by ω_o, the other's by ω_a. To maintain stability, in both cases the nondominant pole is set at a much higher frequency than the closed-loop regulator bandwidth.

The supply sensitivities for these two regulators are shown in Fig. 5. For the regulator (a) with a high-bandwidth amplifier, as the supply noise frequency passes ω_o, the RC filter formed by $r_{\rm vco}, r_o$, and $C_{\rm decap}$ begins to decrease the magnitude of the open-loop supply sensitivity. However, due to this same RC filter, the gain of the output device—and hence the gain of the regulator feedback loop—also begins to drop; these two effects initially cancel each other such that there is no net change in the supply sensitivity. Past its closed-loop bandwidth $(\omega_{\rm bw})$ the regulator can no longer actively attenuate supply noise, and therefore the supply sensitivity is set entirely by the output RC filter. At $\omega_{\rm bw}$, the attenuation of the output RC filter approaches the regulator's open-loop gain, and therefore past the regulator bandwidth the supply sensitivity falls with the single pole roll-off of the RC filter.

[1]Imperfect coupling of $V_{\rm bp}$ to $V_{\rm dd}$ can be thought of as a (frequency-dependent) reduction in the output impedance of the output device, and can be modeled by appropriately modifying the open-loop sensitivity $S_{\rm Vdd}$ from (1). Capacitive coupling directly from $V_{\rm dd}$ to $V_{\rm reg}$ simply limits the high-frequency rejection of the regulator. While capacitor ESR can improve regulator stability, it too limits the high-frequency supply rejection of the regulator.

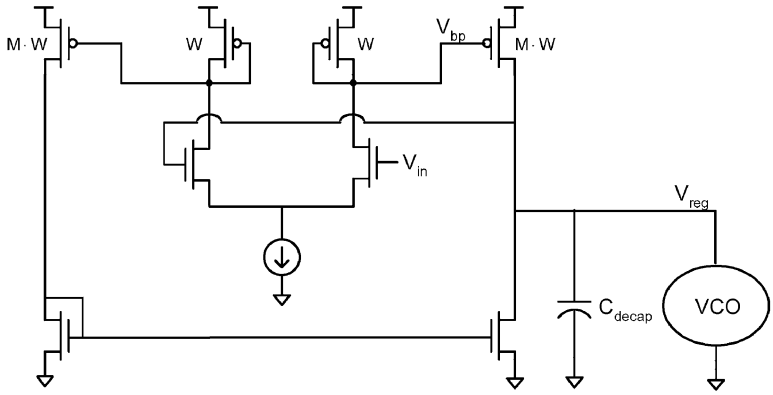

Fig. 3. Alternative linear regulator topology from Sidiropolous [2]. A low output impedance amplifier was used to mitigate the issue with the pole at the amplifier output and eliminate the stability problem, but this solution leads to significant power consumption in the amplifier.

The supply sensitivity of the regulator for which the amplifier is the dominant pole (b) behaves quite differently. As soon as the supply noise surpasses the amplifier bandwidth, the amplifier gain begins to drop and the supply sensitivity increases. Past the closed-loop bandwidth of the regulator, the sensitivity flattens out at S_{Vdd}—in other words, the peak sensitivity is roughly $A_a A_o$ times worse than it was with a high-bandwidth amplifier. Only once the bandwidth of the RC filter has been passed will the sensiivity begin to drop from this peak value.

Clearly, for a regulator to achieve good dynamic supply rejection, the amplifier must have both as high of a bandwidth as possible in addition to large gain. Techniques such as those used in [4] and [5] stabilize the regulator by reducing the natural bandwidth of the amplifier—which as we have just shown has the effect of widening the passband of the supply sensitivity transfer function, making the regulator (and overall PLL) more susceptible to supply noise.

III. Replica Compensated Regulator

To arrive at the proposed structure, we will begin by considering the use of an additional negative feedback loop on the regulator's amplifier, as shown in Fig. 6(a). As the feedback gain k is increased, the bandwidth of the amplifier will rise [3]. Formally, defining the transfer function of the amplifier as $A_a(s) = A_a/(1 + s/\omega_a)$, and that of the output stage as $A_o(s) = A_o/(1 + s/\omega_o)$, the additional negative feedback changes the regulator's transfer function to

$$\frac{V_{\mathrm{reg}}(s)}{V_{\mathrm{in}}(s)} = \frac{A_{a\_\mathrm{eff}}(s)A_o(s)}{1 + A_{a\_\mathrm{eff}}(s)A_o(s)},$$
$$A_{a\_\mathrm{eff}}(s) = \frac{A_a(s)}{1 + kA_a(s)} = \frac{A_{a\_\mathrm{eff}}}{1 + s/\omega_{a\_\mathrm{eff}}}. \qquad (2)$$

Once the amplifier bandwidth $(\omega_{a\_\mathrm{eff}})$ has been extended by the local feedback enough that the output pole becomes dominant, the overall regulator will be stabilized. However, since the improvement in amplifier bandwidth is accompanied by a reduction in effective amplifier gain (A_{a_eff}), the low-frequency supply noise sensitivity of the regulator would be degraded.

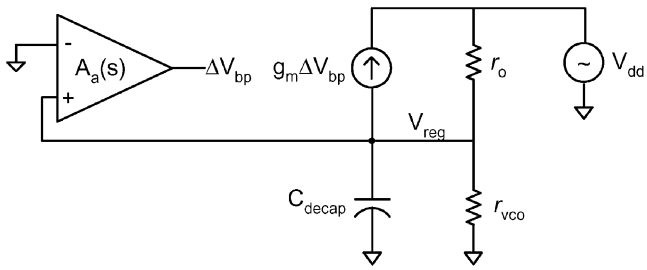

Fig. 4. Simplified small-signal model for regulator power supply rejection. The pMOS output transistor is replaced by its small-signal model (g_m and r_o), and the VCO is modeled by its linearized output resistance (r_{vco}).

To make amplifier feedback an attractive stabilization solution, the amplifier must use all of its available gain to reject supply noise. Conceptually, this goal can be achieved by creating a replica signal V_{rep} that is indicative of the supply noise at V_{reg} in the local feedback path of the amplifier, as shown in Fig. 6(b). The amplifier responds to the replica noise signal in addition to the actual noise; as long as the static supply sensitivity of the replica is nearly identical to that of the VCO (so that V_{rep} is a good indicator of the noise on V_{reg}), the amplifier will apply all of its gain against the noise. As will be described shortly, since no additional low-pass filtering is required on V_{rep} (in fact it is undesirable), the regulator can be stabilized by the secondary feedback loop without sacrificing supply noise rejection. Furthermore, the stabilization need not be costly in terms of power or area because as long as the shapes of the replica and actual *I–V* curves match, the replica load current can be a fraction of the actual load current.

In order to simplify the implementation of the regulator, we can restructure the amplifier and its local feedback loop by separating the forward and feedback gain paths as shown in Fig. 7(a). Since the addition between the feedback from the replica and the feedback from the actual output occurs at the output of their respective amplifiers, as shown in Fig. 7(b) the summation could easily be implemented in the current domain by shunting together the outputs of the transconductance stages that implement the amplifiers.

Notice that in this configuration the total g_m of the two amplifiers is proportional to $1 + k$ while the g_m tied to the input voltage is fixed and independent of k, causing the regulator gain

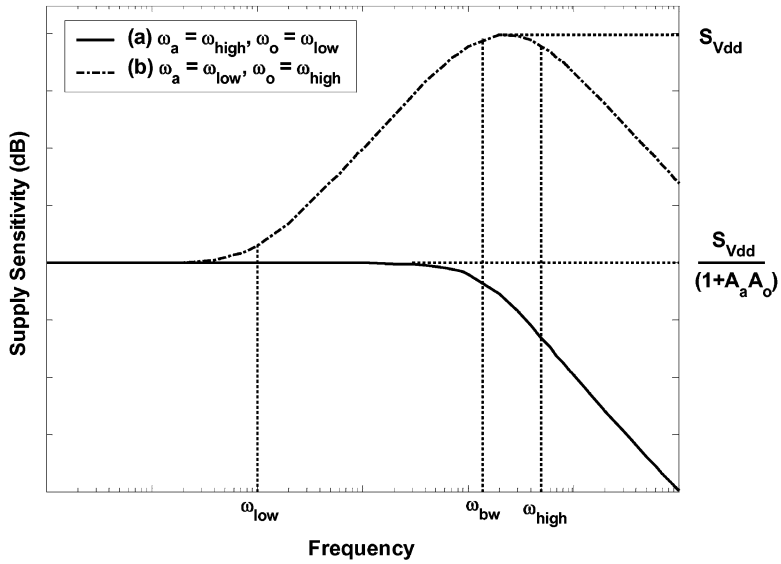

Fig. 5. Example supply sensitivity for a regulator with (a) $\omega_a = \omega_{\rm high}, \omega_o = \omega_{\rm low}$, and (b) $\omega_a = \omega_{\rm low}, \omega_o = \omega_{\rm high}$.

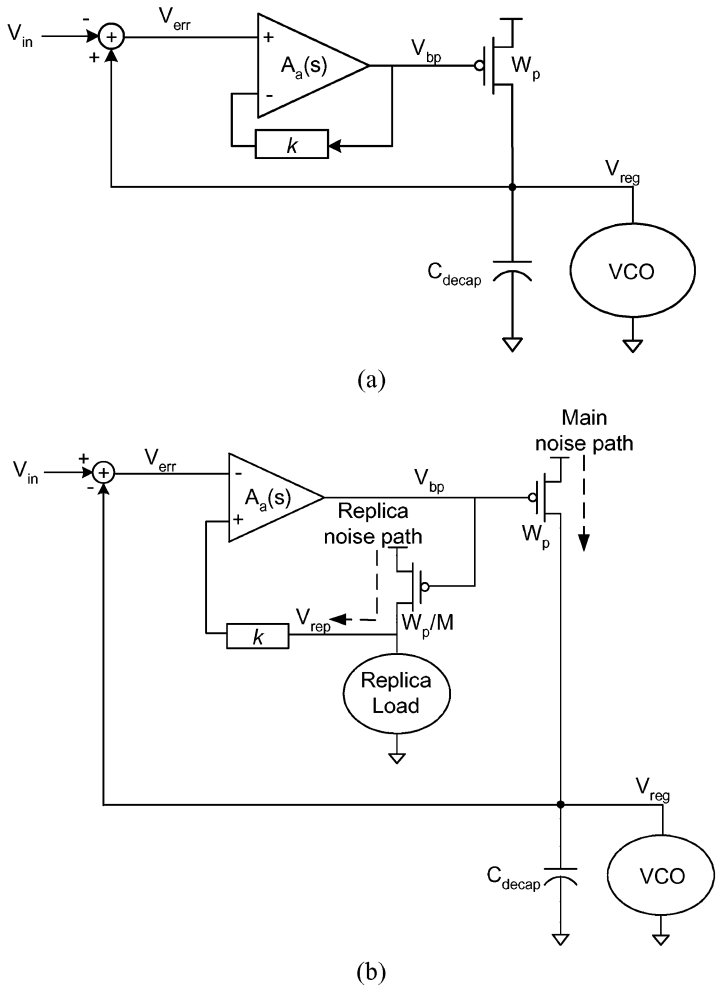

Fig. 6. (a) Application of an additional, local negative feedback loop to the regulator's amplifier. (b) Addition of replica to amplifier feedback to improve regulator supply noise sensitivity.

to drop below unity as k is increased.[2] We can avoid this issue by maintaining a constant total g_m and allocating it between the two paths—i.e., scaling the forward path gain by $1 - k$. The final replica compensated regulator is shown in Fig. 7(c)—two

[2]The DC input to output transfer function of Fig. 7(b) is $A_a A_o/(1 + (1 + k)A_a A_o) \approx 1/(1 + k)$.

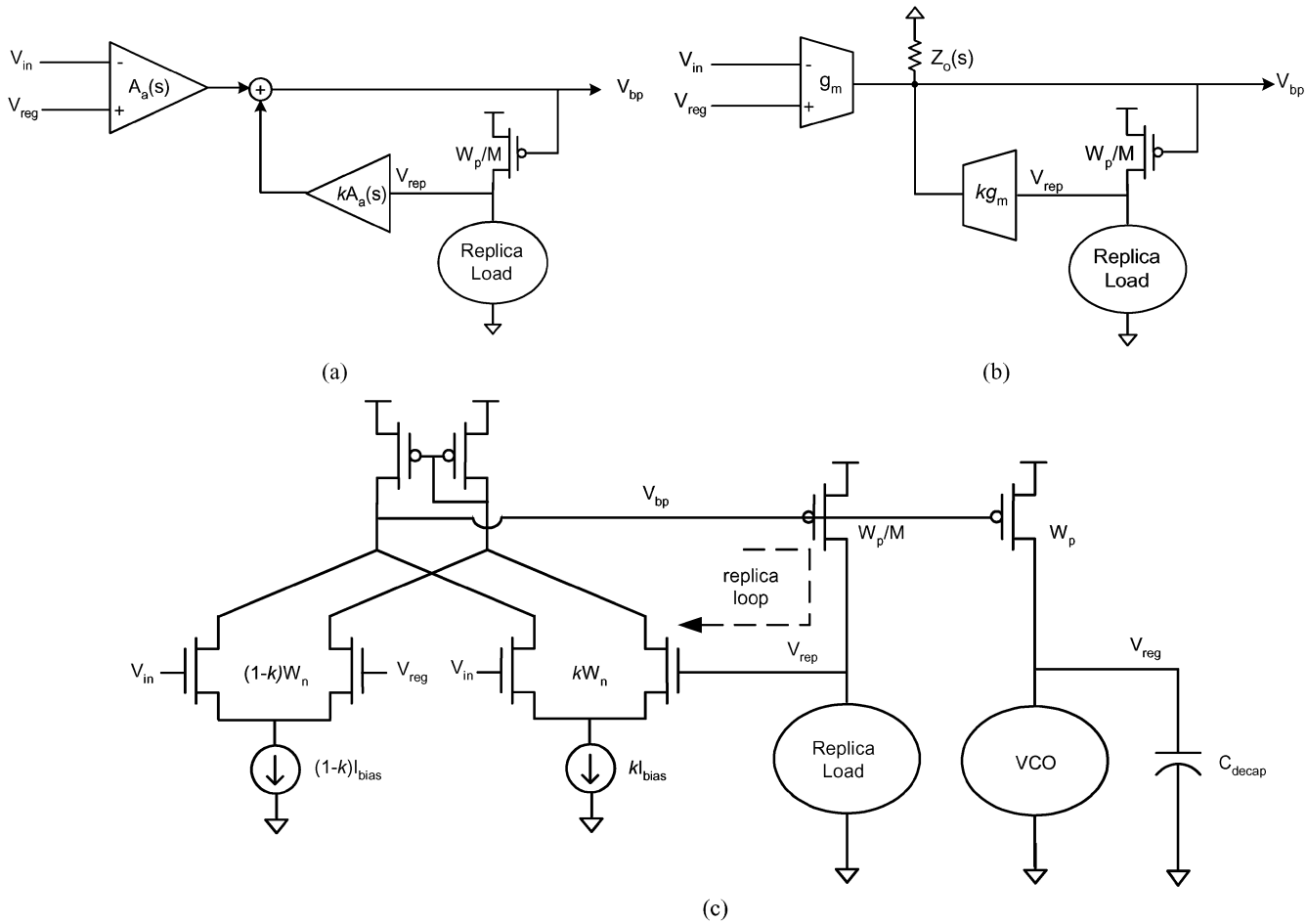

Fig. 7. (a) Separation of the amplifier feedforward and feedback paths. (b) Feedforward and feedback amplifiers implemented using transconductance stages with their outputs summed in the current domain. (c) Circuit implementation of the replica compensated regulator with two differential pairs sharing a single current-mirror load.

differential pairs share a single current-mirror load and the local feedback gain k is set by the current and device width allocated to each pair.

A. Stability Analysis

Defining A_{o_rep} (s) as the transfer function of the replica output stage, the closed-loop transfer function of the regulator is

$$\frac{V_{\mathrm{reg}}(s)}{V_{\mathrm{in}}(s)} = \frac{A_a(s)A_o(s)}{1 + A_a(s)\left((1-\mathrm{k})A_o(s) + kA_{o\_\mathrm{rep}}(s)\right)}. \quad (3)$$

To make the local feedback applied to the amplifier more apparent, this transfer function can be manipulated to match the form of (2) with

$$A_{a\_\mathrm{eff}}(s) = \frac{A_a(s)}{1 + kA_a(s)(A_{o\_\mathrm{rep}}(s) - A_o(s))}. \quad (4)$$

The $A_{o\_\mathrm{rep}}(s) - A_o(s)$ term in (4) shows that the local feedback is only applied to the amplifier at frequencies where the gain of the replica output stage is large compared to that of the actual output stage. At low frequencies, A_{o_rep} should match A_o so that the amplifier maintains its full gain against supply noise, whereas at frequencies between ω_o and ω_{o_rep} (the pole due to the parasitic capacitances at V_{rep}) the feedback takes full effect and extends the amplifier bandwidth, thus stabilizing the regulator. Therefore, ω_{o_rep} should be at a high enough frequency that the local feedback maintains the extended amplifier bandwidth until well beyond the open-loop cross-over frequency.

Fig. 8 shows the root locus of the regulator transfer function as k is swept from zero to one with example values for the gains and poles. Initially, as the effective bandwidth of the amplifier is increased with k, the output pole becomes more dominant and the phase margin of the regulator improves. Once ω_{a_eff} has been increased enough that the overall regulator becomes overdamped, the closed-loop dominant poles of the regulator (ω_{bw} and $\omega_{2\mathrm{nd\_order}}$) meet on the real axis and split. In this region, the regulator bandwidth is approximately set by the output pole,

$$\omega_{\mathrm{bw}} \approx \frac{(1 + A_aA_o)}{(1 + kA_aA_o)}\omega_o \approx \frac{1}{k}\omega_o. \quad (5)$$

Since at this point the output pole is already completely dominant, further increases in amplifier bandwidth do not affect the stability of the loop; hence as k is increased ω_{bw} begins to decrease because of the reduction in effective amplifier gain. Of course, once all of the gain has been allocated to the replica loop (i.e., $k = 1$), the regulator becomes replica biased (as described by den Besten and Nauta for a regulator in [8] and by Maneatis for a PLL or DLL in [9]), with its bandwidth set by ω_o and the

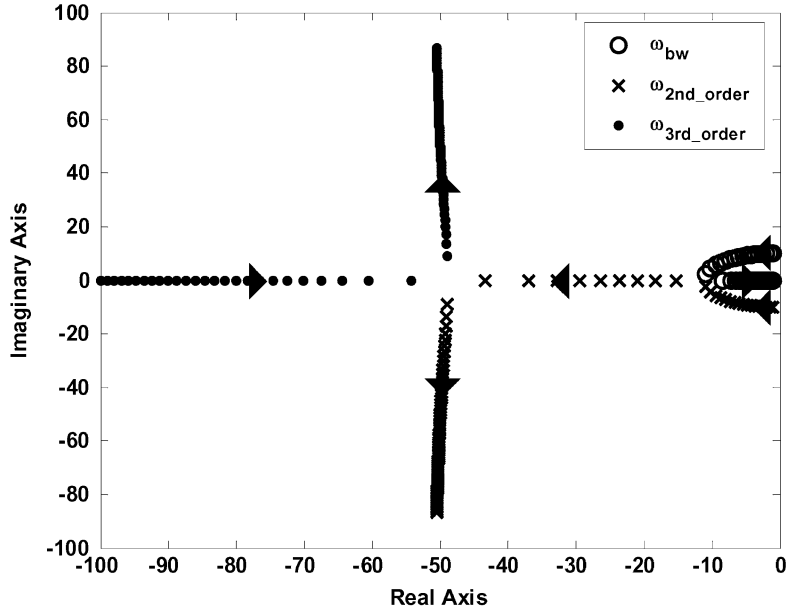

Fig. 8. Replica compensated regulator root locus versus k with $A_a = A_o = 10, \omega_o = \omega_a$, and $\omega_{\rm rep} = 100\omega_o$.

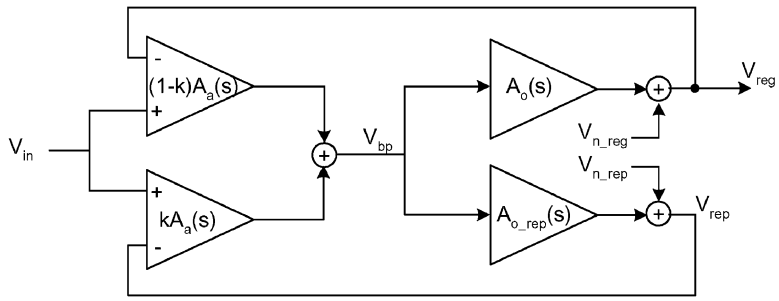

Fig. 9. Noise transfer functions model of the replica compensated regulator.

other two poles ($\omega_{\rm 2nd\_order}$ and $\omega_{\rm 3rd\_order}$) at the closed-loop poles of the replica loop. As shown in the example of Fig. 8, the replica loop may itself be underdamped; therefore, in order to avoid any peaking in the response of the regulator, k should be within the range that makes all three poles of the regulator purely real and negative.

B. Power Supply Rejection Analysis

In order to analyze the supply rejection properties of the regulator, we will derive the noise sensitivity transfer functions using the model shown in Fig. 9. Defining the voltage noise terms as $V_{n\_\rm reg}$ and $V_{n\_\rm rep}$, the transfer functions are

$$\frac{V_{\rm reg}(s)}{V_{n\_\rm reg}(s)} = \frac{1 + kA_a(s)A_{o\_\rm rep}(s)}{1 + A_a(s)\left((1-k)A_o(s) + kA_{o\_\rm rep}(s)\right)} \quad (6a)$$

$$\frac{V_{\rm reg}(s)}{V_{\rm n\_rep}(s)} = \frac{-kA_a(s)A_o(s)}{1 + A_a(s)\left((1-k)A_o(s) + kA_{o\_\rm rep}(s)\right)}. \quad (6b)$$

For noise sources which affect only the regulator output and not the replica signal (e.g., load current variations), the reduction in the effective gain of the amplifier due to the replica feedback degrades the rejection of the regulator. However for a noise source whose DC effects on the output can be replicated (i.e., supply noise), the amplifier will apply its full gain to attenuate the noise. Specifically, if the static sensitivity and DC gain of the replica output stage match those of the actual load, the supply noise transfer function is

$$\frac{V_{\rm reg}(s)}{V_{\rm dd}(s)} = \frac{S_{\rm Vdd}(s)}{1 + A_{\rm reg}(s)} = \frac{S_{\rm Vdd}(s)}{1 + A_a(s)\left((1-k)A_o(s) + kA_{o\_\rm rep}(s)\right)} \quad (7)$$

where $S_{\rm Vdd}(s)$ is the transfer function of the RC filter from $V_{\rm dd}$ to $V_{\rm reg}$.

As mentioned in the previous subsection, in order to avoid any peaking in its response the regulator should be designed such that all three of its poles are purely real and negative. If the regulator is designed in this manner, it is straightforward to predict its sensitivity to supply noise. The dominant pole of the regulator must be set at a frequency 5 to 10 times higher than the PLL bandwidth in order to maintain the PLL's stability, therefore in analyzing supply rejection we will make the additional assumption that the closed-loop bandwidth of the regulator is higher than the open-loop bandwidth of the amplifier.

By sensing the supply noise on both $V_{\rm reg}$ and $V_{\rm rep}$, the replica compensated regulator makes use of all of the gain available to the amplifier to reject supply noise. Therefore, once the supply noise frequency passes the open-loop bandwidth of the amplifier (ω_a), the amplifier's gain drops and the regulator will have

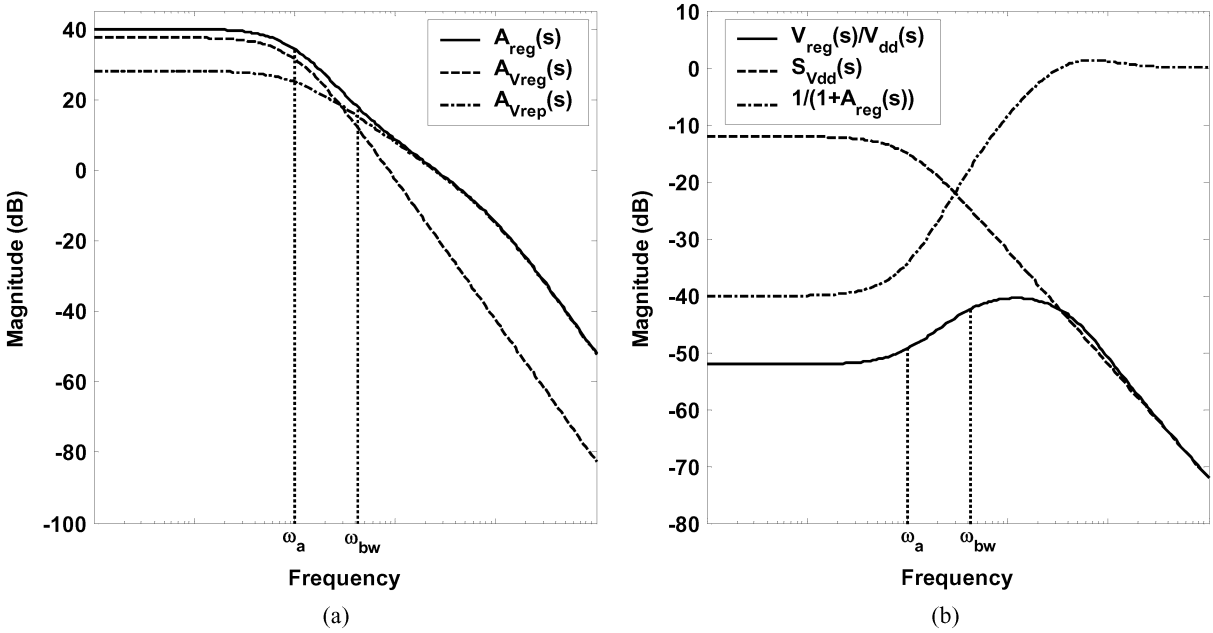

Fig. 10. Replica compensated regulator (a) open-loop gains and (b) supply sensitivity components with $A_a = A_o = 10, \omega_o = \omega_a, \omega_{\rm rep} = 100\omega_o, k = 0.25$, and $S_{\rm Vdd} = 0.25$. $A_{\rm reg}(s)$ is the total gain the regulator applies against supply noise, $A_{\rm Vreg}(s)$ is the gain the regulator feedback applies to noise sensed on $V_{\rm reg}$, and $A_{\rm Vrep}(s)$ is the gain applied by the replica path to noise sensed on $V_{\rm rep}$.

less total gain $A_{\rm reg}(s)$ to combat the noise. Just as it did for the traditional regulator, this effect causes the appearance of a zero at ω_a in the supply noise transfer function of the replica compensated regulator (Fig. 10).

In a manner also identical to that of the traditional regulator, when the supply noise frequency passes ω_o, both the gain of the output device and the coupling of $V_{\rm reg}$ to $V_{\rm dd}$ begin to drop, and hence no additional change in the noise sensitivity is observed. However, the bandwidth of the RC filter on $V_{\rm rep}$ is much higher than ω_o, and hence both the gain of the replica output device and the coupling from $V_{\rm dd}$ to $V_{\rm rep}$ will remain unattenuated. Therefore, as shown in Fig. 10(a), there will be a frequency at which $A_{\rm reg}(s)$ is dominated by the gain through the replica path—this frequency is the closed-loop bandwidth of the regulator, $\omega_{\rm bw}$. As shown in Fig. 10(b), once the supply noise frequency passes $\omega_{\rm bw}$ the supply sensitivity of the regulator reaches its maximum value before it begins to roll off again due to the attenuation of the output RC filter.

Knowing that the DC sensitivity of the regulator is $S_{\rm Vdd}/(1 + A_aA_o)$, and that at $\omega_{\rm bw}$ the amplifier gain has dropped by $\omega_a/\omega_{\rm bw}$, the maximum sensitivity $(S_{\rm max})$ can be simply approximated by

$$S_{\max} \approx \frac{\omega_{\rm bw}}{\omega_a}\frac{S_{\rm Vdd}}{(1+A_aA_o)} \approx \frac{\omega_o}{\omega_a}\frac{S_{\rm Vdd}}{(1+kA_aA_o)}. \quad (8)$$

Clearly, there is a direct tradeoff between regulator bandwidth and worst-case supply rejection. Increasing regulator bandwidth linearly increases the worst-case sensitivity; equivalently, increasing k improves the regulator's supply rejection but decreases its bandwidth. In fact, in a manner completely analogous to the well-known gain-bandwidth product of feedback amplifiers [3], the product of minimum supply rejection $(R_{\rm min})$ and regulator bandwidth is independent of the feedback gain k, and is given by

$$R_{\min} \cdot \omega_{\rm bw} \approx \omega_a A_a A_o R_{\rm Vdd} \quad (9)$$

where $R_{\rm Vdd} = 1/S_{\rm Vdd}$. Therefore, in order to maximize the worst-case supply rejection of the regulator, the amplifier should have as high of a gain bandwidth product as possible. Furthermore, the regulator should be designed to have the lowest possible bandwidth that maintains PLL stability.

It is important to note that in order to achieve this rejection-bandwidth product for all choices of regulator bandwidth, the regulator must remain stable (i.e., exhibit no peaking) no matter how close the amplifier's pole (ω_a) is set relative to the output pole (ω_o). This is exactly the characteristic that traditional regulator topologies lack, and hence the ability to retain stability while making the amplifier's bandwidth as high as possible (without being forced to make the amplifier's bandwidth larger than the regulator's bandwidth) is the key advantage offered by the replica compensation technique.

IV. Replica Loads

In addition to *I–V* curve matching, the replica load should have low parasitic capacitance in order to make the replica compensation technique effective. The choice of replica load depends on the specific VCO topology used in the PLL, and may involve tradeoffs between *I–V* curve tracking, switching noise generation, and parasitic capacitance.

One of the most straightforward options for a replica load is a scaled copy of the main VCO [Fig. 11(a)]. There are some disadvantages to this approach however; the parasitic capacitance at the supply node of the replica will be relatively large, which can limit the performance of the replica compensated regulator. In addition, the scaled VCO will generate switching noise that due

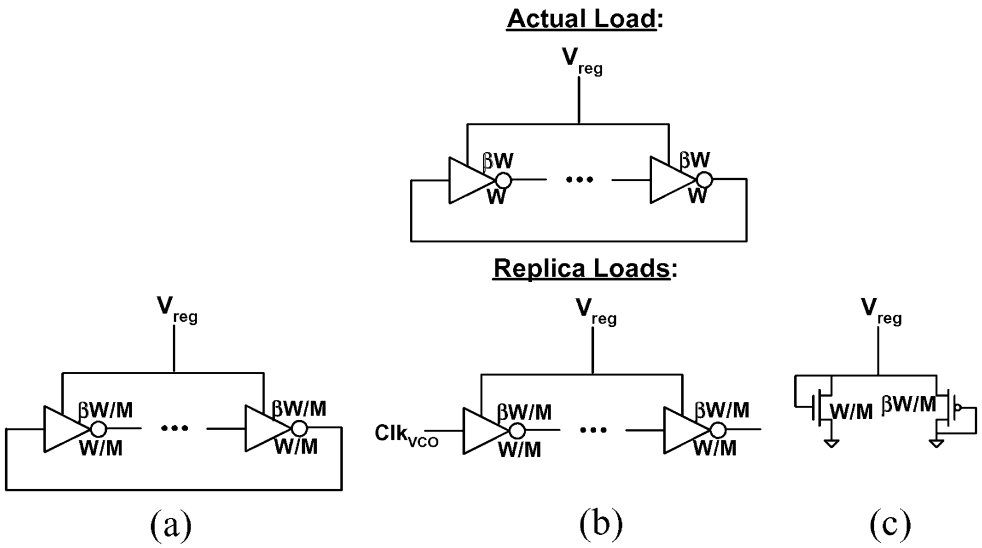

Fig. 11. Replica load options. (a) Scaled copy of the actual VCO. (b) Delay line with the same number of stages as the VCO fed by the VCO clock. (c) Diode-connected devices.

to mismatch may not be aligned in frequency with the real VCO. As shown in Fig. 11(b), this issue can be alleviated by using a delay line fed by the VCO clock instead of a scaled VCO, but this replica load will still have high parasitic capacitance.

The most desirable replica load is one that does not generate switching noise as well as has a low parasitic capacitance. To find a replica with these characteristics, consider the current drawn by a CMOS inverter-based ring oscillator. Ignoring crowbar and leakage currents

$$I_{\rm vco} = n_{\rm stages} C_{\rm stage} V_{\rm reg} f_{\rm osc} \tag{10}$$

where $n_{\rm stages}$ is the number of stages in the ring and $C_{\rm stage}$ is the effective capacitance driven by each inverter in the oscillator. If the capacitance seen by each inverter is roughly the same for both the rising and falling transitions, the period of the VCO ($T_{\rm osc} = 1/f_{\rm osc}$) is

$$\begin{aligned} T_{\rm osc} &= \frac{n_{\rm stages} C_{\rm stage} V_{\rm reg}}{2 I_{\rm on\_p}} + \frac{n_{\rm stages} C_{\rm stage} V_{\rm reg}}{2 I_{\rm on\_n}} \\ &= \frac{n_{\rm stages} C_{\rm stage} V_{\rm reg}}{2 \cdot (I_{\rm on\_p} || I_{\rm on\_n})} \end{aligned} \tag{11}$$

where $I_{\rm on\_p}$ and $I_{\rm on\_n}$ are the saturated drain currents of the pMOS and nMOS transistors in the inverters, respectively. Combining (10) and (11), the current drawn by the VCO is simply twice the parallel combination of the two on-currents:

$$I_{\rm vco} = 2(I_{\rm on\_p} || I_{\rm on\_n}). \tag{12}$$

Therefore, if the inverters in the oscillator are sized such that the on currents for both rise and fall transitions are roughly equal (which as shown by Hajimiri *et al.* [10] is desirable for phase noise considerations), the VCO current will equal $I_{\rm on}$ and can be mimicked by appropriately sized diode-connected transistors. As implied by (12) and shown in Fig. 11(c), a parallel combination of nMOS and pMOS devices is desirable to track variations between the device types.

A diode-connected transistor is an attractive replica load because of its static current and small parasitic capacitance, but it may not match the *I–V* curves of all VCO topologies well—particularly those that draw large amounts of crowbar current. In these cases, the replica load may need to be augmented by additional structures (e.g., an element which mimics crowbar current) in order to improve its *I–V* curve tracking.

V. Mismatch Analysis

A replica-compensated regulator relies on matching between the replica load and the VCO *I–V* curves to minimize output voltage offset and to achieve optimal supply rejection; therefore in this section we analyze the effects of mismatch (both random and systematic) on these parameters. The analysis shows that as long as the mismatch is small enough that the small-signal characteristics of the real and replica output drivers remain matched, variations in the replica load cause only a voltage offset in the output and a shift in the effective feedback gain k. Hence, as long as the regulator is designed with enough margin to withstand small variations in k, the effects of mismatch will be relatively benign.

As shown in Fig. 12, mismatch in the replica *I–V* curve can be split into two components—a static error current $(I_{\rm err})$ and a change in the small-signal output resistance $(r_{\rm rep})$ of the replica load. We will first describe the voltage offset created by the error current, and then examine the effects of mismatch in $r_{\rm rep}$ on the stability and supply rejection of the regulator.

A. Effect of Mismatch on Voltage Offset

If $I_{\rm err}$ is small enough that the linearized characteristics of the replica pMOS driver do not significantly deviate from their matched values, we can model the effect of $I_{\rm err}$ by simply converting it into an error voltage $(V_{n\_\rm rep})$ through the small-signal resistance at $V_{\rm rep}$; the effect of this error voltage on the regulator output has already been shown in (6b). As k is increased a larger percentage of this error voltage is transferred to the regulator output, but for reasonable offsets this is not a large concern

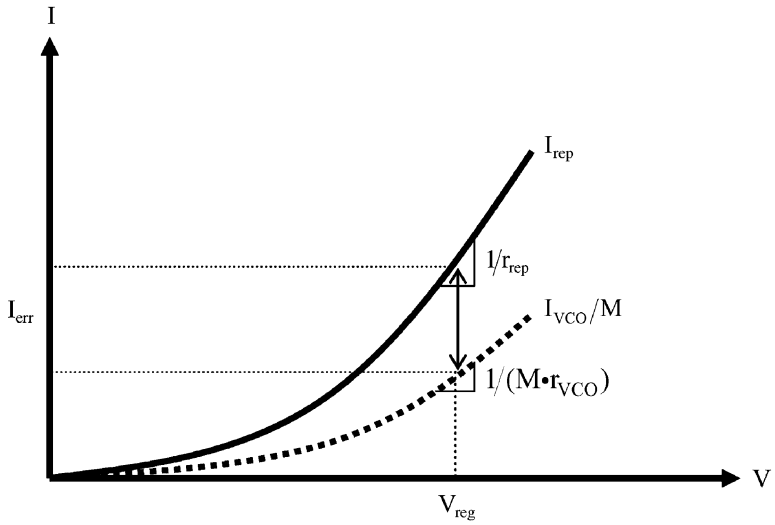

Fig. 12. *I–V* curves of a VCO (scaled by M) and a replica load showing the offset ($I_{\rm err}$) and output resistance ($r_{\rm rep}$) mismatch components.

because the PLL will adjust the regulator's input voltage to keep the VCO oscillating at the proper frequency.

B. Effect of Mismatch on Stability

Mismatch in the replica load has two effects on the stability of the overall regulator; the gain of the replica output stage no longer matches that of the main output stage, and the location of the parasitic pole $\omega_{\rm rep}$ is shifted. Since $\omega_{\rm rep}$ should be well above the regulator's closed-loop bandwidth, the more dominant effect is the change in the gain of the replica output stage.

If the DC gain of the replica output stage is $A_o+\Delta A_o$, where A_o is the gain of the output stage with perfect matching and ΔA_o is the gain error term, the regulator transfer function becomes

$$\frac{V_{\rm reg}(s)}{V_{\rm in}(s)}=\frac{N_{\rm matched}(s)}{D_{\rm matched}(s)+kA_a\Delta A_o(1+s\omega_o)} \tag{13}$$

where $N_{\rm matched}(s)$ and $D_{\rm matched}(s)$ are the numerator and denominator of the transfer function with perfect matching (3). The main effect of the additional term is that it adjusts the feedback gain of the replica loop, shifting the entire root locus of Fig. 8 to the right if $\Delta A_o<0$ or to the left if $\Delta A_o>0$. For small k values, this is equivalent to changing the gain allocation to $k_{\rm eff}$, where

$$k_{\rm eff}=\left(1+\frac{\Delta A_o}{A_o}\right)k. \tag{14}$$

As long as the nominal k is chosen so that small perturbations in its value do not affect the nature of the regulator's closed-loop poles (e.g., two real poles become underdamped and leave the real axis), mismatch does not limit the stability of the regulator.

C. Effect of Mismatch on Supply Rejection

As explained in the previous subsection, mismatch causes the gain of the replica output driver to differ from that of the main output driver. To understand how this affects the supply rejection of the regulator, consider a simple example in which mismatch increases the gain of the replica output driver. The increased gain of the replica loop attenuates the effect of the supply noise on the replica load, decreasing the error signal fed to the amplifier and hence increasing the effect of the noise on the regulator's true output.

Mismatch also causes the supply sensitivity of the replica ($S_{\rm Vdd\_rep}$) to differ from that of the VCO. An increase in the sensitivity of the replica load causes the amplifier to pull the true output in a direction opposite that of the supply noise; with large enough mismatch the sign of the coupling from the supply to the regulator output can even become negative (i.e., an increase in supply voltage leads to a decrease in output voltage).

We can formally model these two effects by re-deriving the supply sensitivity transfer function with $A_{o\_\rm rep}=A_o+\Delta A_o$ and $S_{\rm Vdd\_rep}=S_{\rm Vdd}+\Delta S_{\rm Vdd}$:

$$\frac{V_{\rm reg}(s)}{V_{\rm dd}(s)}=\frac{N_{\rm vdd}(s)+kA_aA_o(\Delta A_o/A_o-\Delta S_{\rm Vdd}/S_{\rm Vdd})}{D_{\rm vdd}(s)+kA_a\Delta A_o(1+s\tau_o)}. \tag{15}$$

The effect of mismatch on supply sensitivity can be further simplified if we continue to assume that $I_{\rm err}$ is small enough in magnitude that it does not cause a significant shift in the small-signal characteristics of the replica output driver ($g_{m\_\rm rep}=g_m/M$ and $r_{o\_\rm rep}=r_o\cdot M$). In this case, the source of both error terms (change in gain and change in supply sensitivity) is the mismatch in the small-signal output resistance of the replica load, $r_{\rm rep}$.

With this simplifying assumption, we can derive the error terms $\Delta S_{\rm Vdd}/S_{\rm Vdd}$ and $\Delta A_o/A_o$ in terms of the output resistance mismatch $\Delta r_{\rm rep}(r_{\rm rep}=r_{\rm vco}\cdot M+\Delta r_{\rm rep})$ and the small-signal parameters of the output driver. Starting from the matched gain $A_o=g_{m\_\rm rep}\cdot(r_{\rm rep}\|r_{o\_\rm rep})$ and supply sensitivity $S_{\rm Vdd}=r_{\rm rep}/(r_{\rm rep}+r_{o\_\rm rep})$, we find that the two error terms are in fact equal to each other:

$$\frac{\Delta A_o}{A_o}=\frac{\Delta S_{\rm Vdd}}{S_{\rm Vdd}}=\left(\frac{\Delta r_{\rm rep}}{r_{\rm rep}}\right)\cdot\left(\frac{r_{o\_\rm rep}}{r_{\rm rep}+\Delta r_{\rm rep}+r_{o\_\rm rep}}\right). \tag{16}$$

This result simplifies the analysis of mismatch on supply rejection because the two error terms in the numerator of (15) cancel each other and the only remaining perturbation lies in the denominator, which as discussed above can be approximated as a change in the gain allocation k.

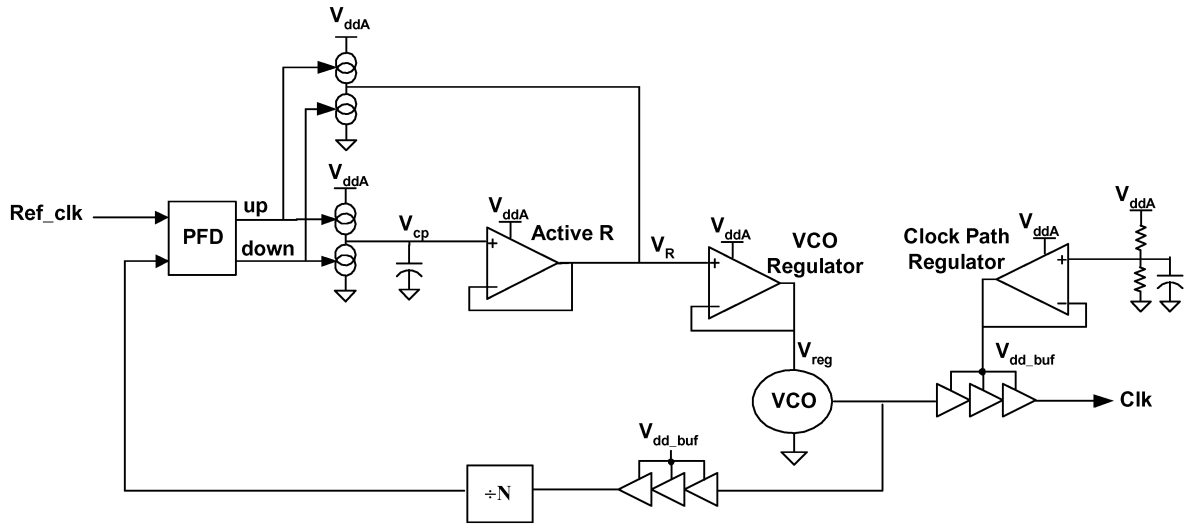

Fig. 13. PLL and clock distribution architecture of the test chip for characterization of the parallel interface described in [7]. The stabilizing resistor for the PLL's loop filter is created by the output resistance of the unity gain buffer labeled "Active R". Nominally, $V_{\mathrm{ddA}} = 1.5$ V, and $V_{\mathrm{dd\_buf}} \approx 0.73 \cdot V_{\mathrm{ddA}}$.

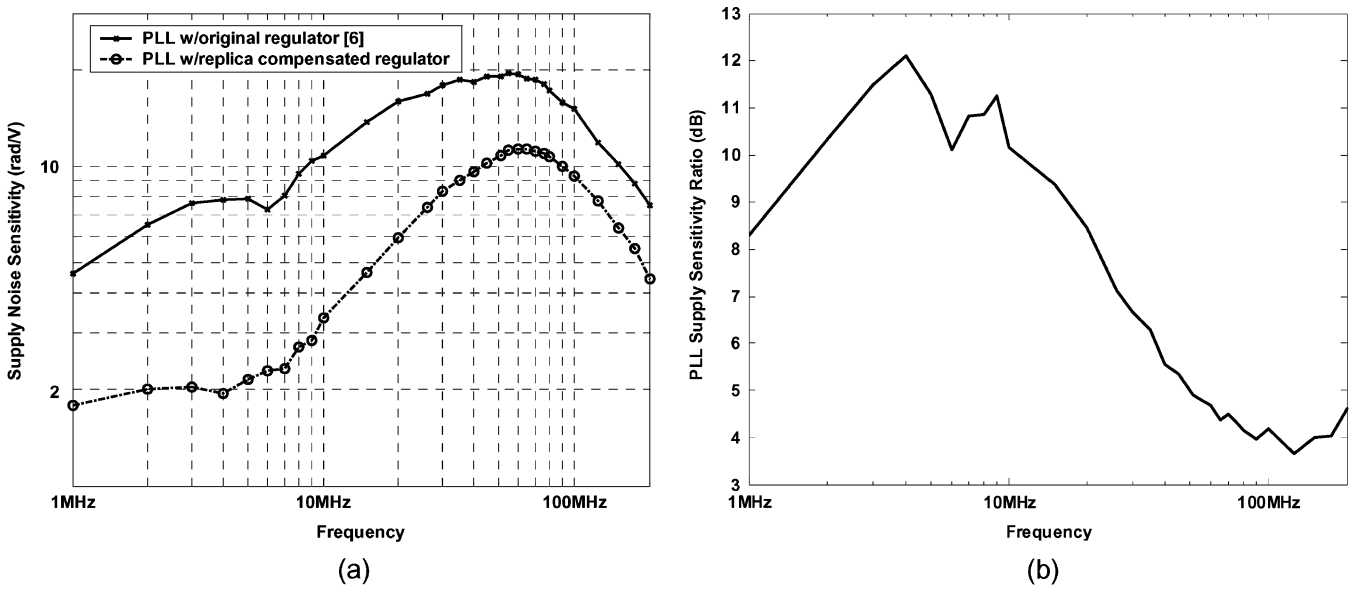

Fig. 14. (a) Measured supply noise sensitivity versus frequency for the PLL with the original regulator design and for the PLL with the replica compensated regulator. (b) Sensitivity of the original PLL divided by sensitivity of the PLL with the replica compensated regulator.

VI. Experimental Results

The replica compensated regulator was implemented in a 90 nm SOI process as part of one of the PLLs on a test chip for characterization of the parallel interface described by Chang *et al.* in [7]. Each transmit or receive byte-wide link has a multiply-by-5 PLL to generate its high-speed clock; the PLL architecture (Fig. 13) is based upon a previous design [6].

For the purpose of comparison, two transmit byte-wide parallel links were fabricated; with all other components identical (including the decoupling capacitance used on the VCO supplies), the PLL for one of the links used a VCO regulator based on [2] and [6], and the VCO regulator in the other link was replica compensated. For this application, the power consumption of the regulator was less important than its supply rejection, and therefore the replica compensated regulator was designed to achieve the best rejection possible while consuming roughly the same amount of power as the original regulator. For the replica compensated regulator, a parallel combination of nMOS and pMOS diode-connected transistors served as the replica load.

While the test chip did not include the capability to directly measure the regulator output voltage (and hence the regulator supply noise sensitivity), it did include supply noise generators and measurement circuits similar to those described by Alon *et al.* in [11]. Therefore, we used the generators to inject sinusoidal noise onto the power supply, measured the resulting jitter by sending a clock pattern through the transmitter, and normalized this jitter by the measured supply noise magnitude to obtain the supply noise sensitivity for the two PLLs. The results of this measurement for both PLLs operating at 2.5 GHz are shown in Fig. 14(a).

The measured data clearly shows that the PLL with the replica compensated regulator has lower supply sensitivity. To better

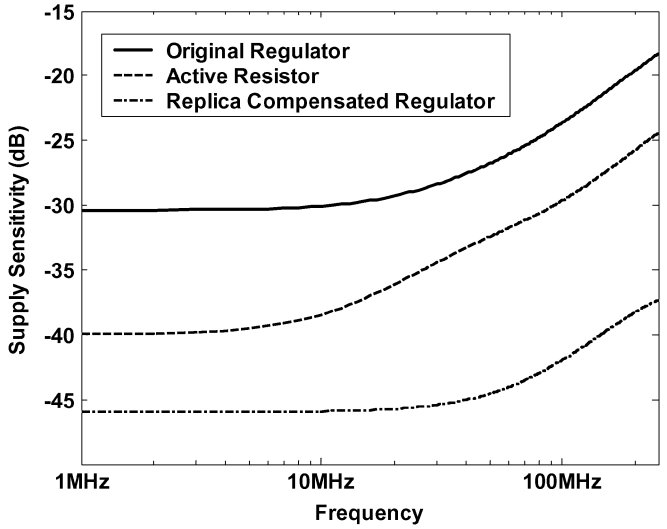

Fig. 15. Simulated supply noise sensitivities for the original regulator, active resistor, and replica compensated regulator.

isolate the sensitivity differences due to the regulators from the filtering that the PLL itself applies to the noise (as described by Mansuri *et al.* in [12]), Fig. 14(b) shows the measured sensitivity of the original PLL divided by the sensitivity of the PLL with the replica compensated regulator. Because of the additive supply noise paths through the active resistor and clock buffers, the ratio shown in Fig. 14(b) will not directly match the ratio of regulator sensitivities—but it does provide a lower bound on the improvement of the replica compensated regulator over the previous design.

The measurement shows that the additional gain stage of the replica compensated regulator improves the low-frequency noise sensitivity[3] by at least $\sim$10 dB. In fact, the simulation results of Fig. 15 show that even at higher frequencies the additional gain stage reduces the replica compensated regulator's sensitivity enough that the active resistor becomes the dominant contributor of noise coupling from V_{ddA} to the VCO supply.[4]

The fact that the active resistor is the dominant source of sensitivity to supply noise in the PLL with the replica compensated regulator unfortunately makes it difficult to isolate the replica compensated regulator's sensitivity; however, the sensitivity ratio does provide a lower bound on the relative improvement of the replica compensated design. Thus, the measured ratio shows that with roughly the same power consumption, the replica compensated regulator achieves a minimum of $\sim$4 dB higher supply rejection than the previous design. Furthermore, the typical corner simulations from Fig. 15 indicate that the regulator in isolation achieves an improvement of greater than 15 dB in supply noise rejection.

[3]Because of the integration from the charge pump/loop filter, it is normally expected that the supply sensitivity of an overdamped PLL rises at 20 dB/dec at low frequencies (i.e., below $\sim$1/10th of the PLL bandwidth). The sensitivity of the original PLL displays this behavior, but the low-frequency sensitivity of the PLL with the replica compensated regulator is essentially flat—leading to the low-frequency slope in the sensitivity ratio. The floor in the noise sensitivity of the PLL with the replica compensated regulator is most likely due to mismatch between the clock buffers on the forward path and those in the feedback path, and hence it is unlikely that the low-frequency slope in the sensitivity ratio is due to the behaviors of the two regulators.

[4]Note that the reason for the increase in sensitivity of the active resistor and original regulator that begins at 10–20 MHz is most likely the reduction in effective output impedance of body-contacted SOI devices at frequencies where the resistive body contact is no longer effective [7]. Due to differences in sizing and topology, the active resistor displays this behavior at a lower frequency than the original regulator, leading to the reduction in measured sensitivity ratio that begins at $\sim$10 MHz shown in Fig. 14(b).

VII. Conclusion

By analyzing the properties of common-source pMOS output regulators, we have shown that in order to have optimum supply rejection characteristics the dominant pole of the regulator must be at the regulated supply output. However, using traditional implementations it is very expensive in terms of power consumption to make the amplifier bandwidth high enough that the output pole is completely dominant, and therefore in order to avoid stability issues supply noise rejection is sacrificed and the amplifier is often designed to either be the bandwidth limiter of the regulator or simply have very low gain.

The replica compensated regulator topology allows synthesis of a high-bandwidth amplifier without excessive power consumption by making use of a local replica feedback loop. This feedback loop extends the bandwidth of the amplifier by reducing its forward gain. However, because the replica loop responds in the same manner as the main loop to supply noise, the gain the amplifier applies to combat supply noise is not reduced, allowing the replica compensated regulator to maintain high supply rejection.

For all regulators in which the open-loop bandwidth of the amplifier is not higher than the bandwidth of the output stage, there is a direct tradeoff between the bandwidth of the regulator and its supply rejection. The key advantage of the replica compensated regulator is that it can achieve this product while meeting the regulator's bandwidth requirement, whereas traditional regulator topologies are forced to sacrifice supply rejection because of the stability issues associated with two closely spaced poles.

While the replica compensation technique is based upon matching between the replica load and the VCO, analysis shows that as long as the mismatch between the replica load and the actual VCO is moderate, the effects of this mismatch can be easily absorbed by an appropriate margin in the gain allocation of the replica compensated regulator. Indeed, measurement results confirm that at the same power consumption and with otherwise identical PLLs, a replica compensated design achieves superior supply rejection performance over the previous regulator topology.

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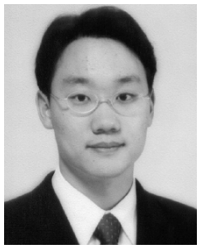

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