Transistor matching in analog CMOS applications.

Marcel J.M. Pelgrom, Hans P. Tuinhout and Maarten Vertregt
Philips Research Laboratories, Bldg. WAY5, Prof. Holstlaan 4, 5656AA Eindhoven, the Netherlands,
FAX +31-40-2744657, e-mail: pelgrom@natlab.research.philips.com

Abstract

This paper gives an overview of MOSFET mismatch effects that form a performance/yield limitation for many designs. After a general description of (mis)matching, a comparison over past and future process generations is presented. The application of the matching model in CAD and analog circuit design is discussed. Mismatch effects gain importance as critical dimensions and CMOS power supply voltages decrease.

Introduction

MOS transistor matching is an important design parameter in many CMOS applications. MOS transistor matching in analog CMOS applications deals with statistical device differences between pairs of identically designed and identically used transistors. In analog circuit blocks, like A/D converters, threshold voltage differences of millivolts or less can determine the performance and/or yield of a product. Figure 1

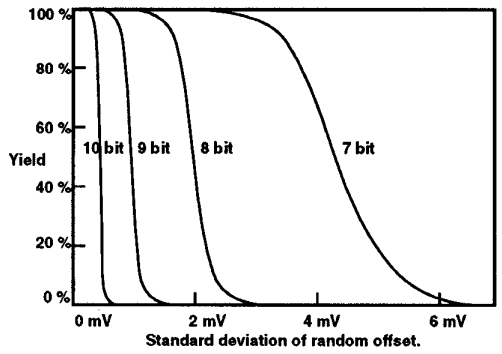

Fig. 1. The yield of 7..10 bit Analog-to-digital converters as a function of the standard deviation of the input transistor pair mismatch.

shows an example where the physical effect of transistor matching affects the yield of an analog-to-digital converter[1]. The standard deviation of the random offset of the transistor pair that forms the input of the comparator, is shown. Although the random offset is in the millivolt range, it has a significant effect on the yield of the circuit.

In high performance CMOS ICs parallel processing of signals is a necessity: as a consequence the equality of these parallel paths (e.g. in multiplexers, comparators, input stages etc.) is important. Figure 8 will give an example of how transistor matching influences clock delay differences in clock trees. Hence, unequal paths lead to performance or yield loss in analog circuits or reduce robustness in digital circuits.

Threshold matching

The difference ΔVT between the threshold voltages of a pair of MOS transistors (mismatch) is usually described[2], [3], [4], [5], [6], [7] by its standard deviation:

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}} = \frac{qt_{ox}\sqrt{2Nt_{depl}}}{\epsilon_0\epsilon_{ox}\sqrt{WL}} \quad (1)$$

This description is based on the assumptions that mismatch is caused by independent random disturbances of physical properties and that the correlation distance of the statistical disturbance is small compared to the active device area. These assumptions lead to

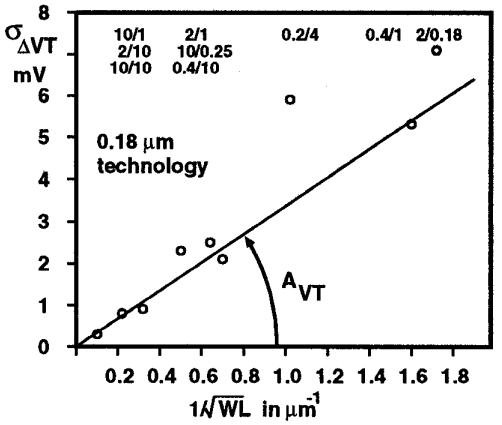

Fig. 2. The standard deviation of the NMOST threshold versus the inverse square root of the area, for a 0.18 μm (3.3-nm gate oxide) process.

a proportionality of the standard deviation with the inverse square root of the area, see Figure 2. The most important contribution to the proportionality constant A_{VT} is the uncertainty in the number of active doping atoms in the depletion layer (N). The statistical variation in $N = (N_a + N_d)$ determines the matching (while control of the net value $(N_a - N_d)$ determines the threshold voltage V_T). As indicated in

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formula 1, the matching coefficient for different processes reduces with decreasing gate oxide thickness (t_{ox}). Examples of other statistical disturbances that contribute to MOS matching are: dimensional variations, interface states, etc.

Figure 3 shows the evolution of the matching coefficient A_{VT} with process generation. The improvement of A_{VT} with oxide thickness is clearly observed[2], [4], [8]. Transistor scaling practice forces the doping level under the gate to increase, hence the depletion width (t_{depl}) reduces with $N^{-0.5}$. To first order, the overall dependence of A_{VT} with the doping is proportional to $N^{0.25}$, which means that A_{VT} will decrease less than the predicted oxide thickness scaling in future process generations.

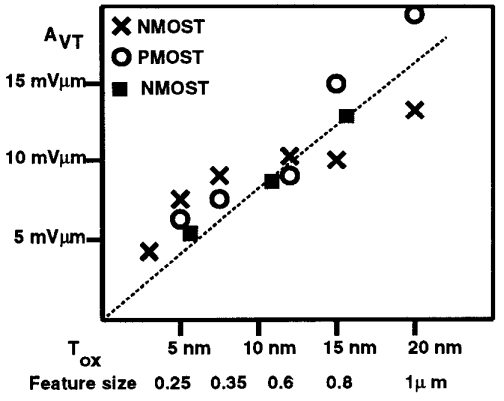

Fig. 3. Evolution of matching coefficient over process generation. Squares are derived from[4], the other measurements are by the authors.

Figure 2 also demonstrates that excessive dimensional variations near the lithographical limits of the used stepper (for the 0.2/4 μm as well as for the 2/0.18 μm transistors) result in increased standard deviations. Various improvements of the elementary $1/\sqrt{WL}$ law have been proposed [9], [10], aiming at improved prediction for small feature sizes. Other work[8], [11], [12] suggests that by using effective W and L values, corrected for depletion region charge sharing, the basic description can be extended down to below 0.1 μm feature sizes.

Optimum circuit performance can only be achieved when the matched circuit elements are designed identical with respect to geometry, rotation, biasing and temperature. Moreover various environmental effects play a role for matching: distance[2], topography (resist crowding)[13], [14], metal coverage [15], implantation striping, packaging[16] and mechanical strain[17]. The prediction of the matching coefficient in Figure 3 sets a target for the process development: deviations as mentioned above, must be traced and corrected in an early phase of the development. For instance the high values for the PMOS transistors in the 0.8 and 1 μm processes are due to compensating implantations in an n-well process. Another effect that can have a devastating impact on matching is associated with gate depletion in deep sub-micron processes[18].

Matching energy

In analog circuit design the threshold voltage matching is generally treated as an error voltage over the gate capacitor of the MOS transistor. This means that an error energy can be defined as [19], [20]:

$$E_{match} = C_{gate}\sigma^2_{\Delta VT} = C_{ox}A^2_{VT} \qquad (2)$$

The energy of the signal to be processed by the electronic circuit must be significantly larger than this random matching energy. In digital circuits (e.g. flip-flops) a factor of 6-10$\times\sigma_{\Delta VT}$ overdrive is required, while in analog circuits the signal-to-noise ratio or spurious signal suppression must be met. For a comparison to thermal noise energy, E_{match} is plotted in figure 4 in kT units. This plot clearly shows that for relevant circuits the matching energy is two orders of magnitude more than thermal noise energy (1 kT), which was the basis for earlier performance limitation analysis[23].

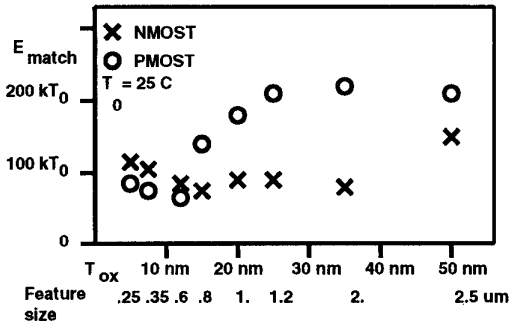

Fig. 4. Evolution of matching energy $C_{ox}A^2_{VT}$.

Power supply

Many analog circuits are limited by signal voltage amplitude. Figure 5 gives the power supply voltage development according to the SIA roadmap[21]. The crosses in the graph represent the matching coefficients for the relevant process generations, while the lower line indicates the matching of a pair of minimum size transistors. The graph clearly shows that the signal swing reduction due to the lower supply voltage becomes a limiting factor for analog CMOS designs. Since matching energy remains constant over

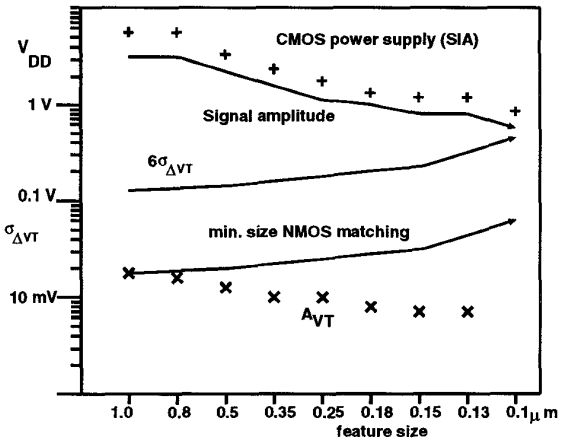

Fig. 5. Development of power supply voltage and the measured NMOS threshold matching factor A_{VT} through various process generations. The available signal swing (upper solid line) is derived by taking 90% from the nominal power supply and subtracting a threshold voltage and $4kT/q$ gate overdrive.

process generations (Figure 4), signal amplitude reduction must be counteracted by higher currents to assure the same signal-to-matching ratio. The effective signal voltage amplitude can be increased by low V_T transistors[22] or local V_{dd} boost. Alternative routes in design are repartitioning of systems into pure digital CMOS ICs and peripheral BiCMOS ICs where the inherently better matching of bipolar transistors (A_{Vbe}=0.35 mVμm [14]) can be exploited.
The $6\sigma_{\Delta VT}$ line in Figure 5 indicates that for 0.1 μm processes threshold voltage matching will also eliminate noise margins in basic digital circuits for multi-million transistor ICs.

Application of mismatch statistics in circuit design

In circuit design CAD the modeling[24], [25], [26], [?] of matching parameters allows to analyse and predict critical performance. Figure 6 shows how the extraction and model description of a standard design flow is adapted to simulate the impact of transistor mismatch. A standard flow will simulate variations of the global transistor parameters to account for process/lot variations: all transistors in a circuit will experience the same variation. The introduction of transistor mismatch parameters causes variations between transistors in a circuit. A Monte-Carlo analysis allows the evaluation of the variations of desired circuit performance, which subsequently allows yield predictions. A comparison of predicted behaviour and measured performance is shown in the example of a bandgap

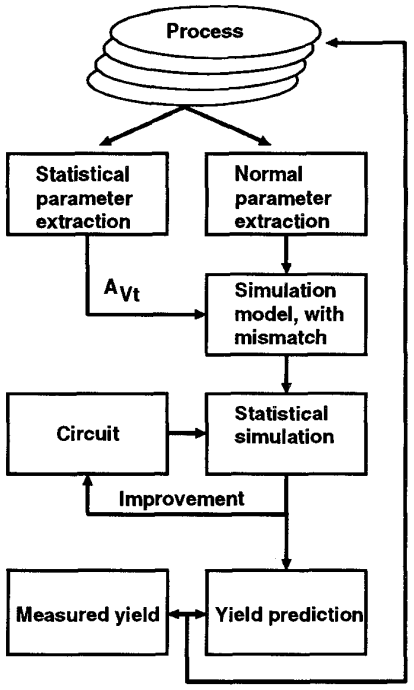

Fig. 6. The effect of the introduction of matching parameters on the design flow.

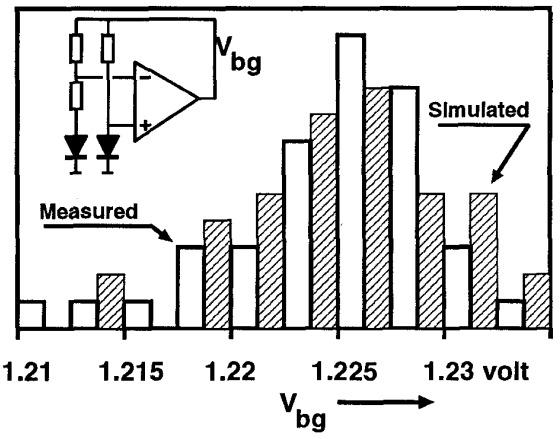

Fig. 7. Comparison of simulated bandgap spread and measured spread.

circuit in Figure 7. In this example the NMOS transistors in the input stage of the amplifier suffer from mismatch, which translates into output voltage variations in V_{bg}. The good agreement between the measured and simulated distributions shows, that when characterized and modeled properly, matching effects can be taken into account during the design phase. As indicated before, also in digital designs matching can be important. Various digital circuit blocks are in fact analog: sense amps in memories, clock trees etc.

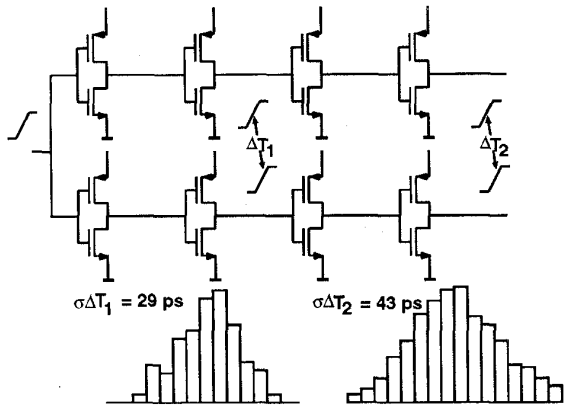

Fig. 8. Due to MOS matching the clock signal propagates differently over both inverter chains. The histograms shows the simulated distribution over 200 trials.

Another example is the study of Mizuno [4], which relates RAM cell threshold variation to dopant fluctuations. Figure 8 shows as an example the random part of clock skew between two branches in a clock tree, which was built in a 0.25 μm CMOS process with 1/0.25 μm and 2/0.25 μm transistors. In GigaHertz digital circuits the magnitude of the skew variations will be comparable to the clock cycle.

Conclusion

Matching performance is a key parameter for analog CMOS process development. In circuit design, extensions in modelling and CAD allow prediction of yield or performance loss. Even digital circuit design will be affected.

Matching effects gain importance as process dimensions decrease and power supply lowers. MOS transistor matching has proven to be a key factor for improving analog and digital circuit performance and for optimizing CMOS technology.

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