Ultra low power four-quadrant multiplier/two-quadrant divider circuit using FGMOS

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Abstract

This paper presents a novel ultra low power wide-range four-quadrant multiplier/two-quadrant divider circuit. The proposed circuit is implemented using Floating Gate MOS (FGMOS) devices operating in weak inversion. The wide range is achieved by means of a predistortion technique based on having different input capacitances in the FGMOS transistors. The circuit compares favourably to other ultra low power multiplier/divider circuits. The multiplier/divider can operate under a 0.9V supply voltage with a power consumption of 87nW in a 0.35μm AMS technology.

1. Introduction

Low-power consumption circuit design techniques have become more and more important in modern VLSI technologies. This has been mainly motivated by the demand for portable equipments which must consume as little power as possible to extend the battery life.

Weak inversion mode is suitable for the design of continuous time micropower systems. The use of FGMOS transistors in weak inversion has proven to be specially promising under low power and low voltage constraints [1]-[2]. FGMOS transistors biased in the weak inversion region exhibit an exponential behaviour which can be used to implement various current mode circuits such as multipliers and dividers [3]. In this paper, we propose a circuit that implements four-quadrant multiplication and two-quadrant division. The performance of the circuit is compared to other state of the art implementations. The performance of an equivalent circuit designed with MOS transistors instead is also shown to verify the theoretical analysis and the advantages of the proposed technique.

2. Floating Gate MOS Transistors

A FGMOS transistor is a MOS transistor with capacitive connections to the gate. The device has the same drain, source and bulk terminals; however, the capacitive connections result in an effectively "floating" gate in DC. These connections correspond to extra inputs for the device, whereas the gate is not accessible anymore. In practice, the FGMOS transistor is implemented by extending the polysilicon layer of the gate outside the active area and capacitively coupling it to pieces of a second polysilicon layer placed on top [4].

The voltages connected to the input capacitors control the voltage at the floating gate (FG) and modulate the channel current flowing through the MOS transistor. The equivalent circuit of an N-input FGMOS transistor is shown in Fig.1(a). The voltage at the floating gate (FG) is given by:

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GD}}{C_T} V_D + \frac{C_{GS}}{C_T} V_S + \frac{C_{GB}}{C_T} V_B + \frac{Q_{FG}}{C_T} \quad (1)$$

where V_{FG}, V_D, V_S and V_B are the voltages at the FG, drain, source and bulk respectively; N is the number of inputs; C_i are their corresponding input capacitances; C_{GB}, C_{GS} and C_{GD} are the parasitic capacitances to bulk, source and drain respectively; and C_T is the sum of all the capacitances connected to the FG:

$$C_T = C_{GD} + C_{GS} + C_{GB} + \sum_{i=1}^{N} C_i \quad (2)$$

Q_{FG} is the residual charge that stays trapped in the oxide-silicon interface during the fabrication process.

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If the input capacitances are much larger than the parasitics and also the technique in [4] is used the last four terms can be neglected and the voltage at the gate is just a weighted summation of the voltages at the inputs. Figure 1(b) shows the symbol for an *N*-input n-channel FGMOS.

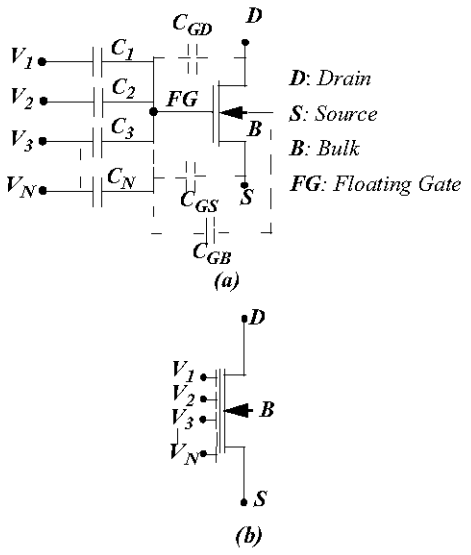


Fig.1: (a) Equivalent circuit for an *N*-input FGMOS transistor. b) Symbol

It has been demonstrated that using FGMOS in weak inversion, as an alternative to conventional MOS, relaxes voltage supply constraints. Moreover, the topologies required to realize a certain mathematical function can be simplified due to the increased number of terminals in the device. This results in a reduction of the power consumption as well as the noise floor [1].

A very popular technique to reduce the power consumption and the power supply voltage consists of designing topologies using the so called "Translinear Principle". It has been shown how the latter is particularly easy to implement if FGMOS in weak inversion are used, instead of normal MOS. In the former, the exponents of non-linear functions can be realized just by choosing adequate capacitances ratios [3]. This has proven to reduce the voltage requirements. It also improves the frequency response (due to the lack of internal nodes) and eliminates instabilities in the circuits [1].

The drain current of an n-channel FGMOS transistor in the weak inversion saturation region with its source and bulk grounded, under the assumptions that $C_i >> (C_{GB}, C_{GS}, C_{GD})$, and $Q_{FG}=0$ is:

$$I_D = I_s e^{\sum_{i=1}^{\left(\frac{C_i}{C_T} \frac{V_i}{n U_T}\right)}} \tag{3}$$

where I_s is the weak inversion specific current, n is the slope factor and U_T is the thermal voltage.

3. Circuit Description

The proposed one-quadrant multiplier/divider circuit is shown in Figure 2(a). Assuming that all the transistors operate in the weak inversion saturation region, all of them are equally sized, and using the translinear principle [1]-[3] the following result is obtained:

$$I_{out} I_b = I_{in1} I_{in2} \tag{4}$$

where all the currents are strictly positive.

Figure 2(b) shows the proposed four-quadrant multiplier/two-quadrant divider circuit. The core elements are M2, M4, M5 and M6. Transistors M1, M3 and M7 duplicate the currents of M2, M4 and M6, respectively, to be I_b, $I_{in1}+I_b$ and $I_{in2}+I_b$. Both, I_{in1} and I_{in2}, can be positive or negative. Currents in the core transistors (named I_{Mi} for transistor Mi) are given as:

$$I_{M2} = I_{M1} = I_b \tag{5}$$

$$I_{M4} = I_{M3} = I_{in1} + I_b \tag{6}$$

$$I_{M5} = \frac{I_{M4} \times I_{M6}}{I_{M2}} = \frac{(I_{in1} + I_b)(I_{in2} + I_b)}{I_b} \tag{7}$$

$$I_{M6} = I_{M7} = I_{in2} + I_b \tag{8}$$

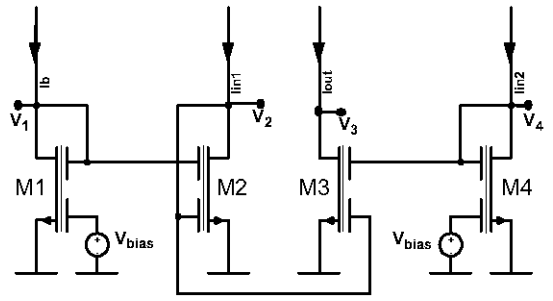
If $|I_{in1}|$, $|I_{in2}| < I_b$, then the output currents are given as:

$$I_{out1} = I_{M1} + I_{M5} = I_b + \frac{(I_{in1} + I_b)(I_{in2} + I_b)}{I_b} \tag{9}$$

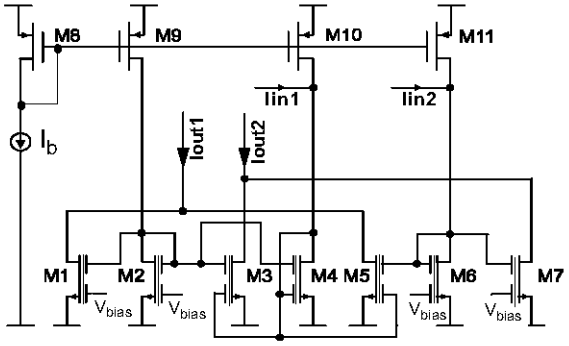
$$I_{out2} = I_{M3} + I_{M7} = (I_{in1} + I_b) + (I_{in2} + I_b) \tag{10}$$

And if a differential output current is defined, then the following result is obtained:

$$I_{out} = I_{out1} - I_{out2} = \frac{I_{in1} \times I_{in2}}{I_b} \tag{11}$$



(a)



(b)

Figure 2: (a) One quadrant multiplier/divider. (b) Four quadrant multiplier/two quadrant divider

4. Parasitic Capacitances, Distortion and Output resistance

One of the main disadvantages of FGMOS-based designs is related to the reduction of the transistor output resistance (when compared to a normal MOS device) caused by the $(C_{GD}/C_T)V_D$ term in the FG voltage equation (eq.(1)). In the case of FGMOS translinear circuits this has a detrimental effect on the circuit linearity. An "easy" way to deal with it is to design the input capacitors big enough so that the term $(C_{GD}/C_T)V_D$ can be neglected from eq.(1). However, this is bad for the frequency response, due to the increased capacitive loads in internal nodes; and also the area. Hence, strategies to deal with distortion should be devised which do not involve having very large input capacitors.

The output current for an n-channel FGMOS transistor with V_S=V_B=0 and not neglecting any parasitic term in the equation of V_{FG} is given by:

$$I_D = I_s e^{\sum_{i=1}^{\left(\frac{C_i}{C_T}\frac{V_i}{nU_T}\right)}} \cdot e^{\frac{C_{GD}}{C_T}\frac{V_D}{nU_T}} \tag{12}$$

Using this expression the currents for the different transistors in Figure 2(a) are given by:

$$I_b = I_s e^{\frac{C_{in}}{C_T}\frac{V_{bias}}{nU_T}} e^{\frac{C_{in}}{C_T}\frac{V_1}{nU_T}} e^{\frac{C_{GD}}{C_T}\frac{V_1}{nU_T}} \tag{13}$$

$$I_{in1} = I_s e^{\frac{C_{in}}{C_T}\frac{V_2}{nU_T}} e^{\frac{C_{in}}{C_T}\frac{V_1}{nU_T}} e^{\frac{C_{GD}}{C_T}\frac{V_2}{nU_T}} \tag{14}$$

$$I_{out} = I_s e^{\frac{C_{in}}{C_T}\frac{V_4}{nU_T}} e^{\frac{C_{in}}{C_T}\frac{V_2}{nU_T}} e^{\frac{C_{GD}}{C_T}\frac{V_3}{nU_T}} \tag{15}$$

$$I_{in2} = I_s e^{\frac{C_{in}}{C_T}\frac{V_{bias}}{nU_T}} e^{\frac{C_{in}}{C_T}\frac{V_4}{nU_T}} e^{\frac{C_{GD}}{C_T}\frac{V_4}{nU_T}} \tag{16}$$

where C_{in} is the value of the FGMOS input capacitances. From eq.(13)-(16) the equation for the output current can be obtained which, as shown below, is a nonlinear function of I_{in1} and I_{in2}.

$$I_{out} = I_s^{(x-1)^2}(I_{in1}I_{in2})^x I_b^{-x^2} e^{\frac{C_{GD}}{C_T}(V_3 - x^2 V_{Bias})} \tag{17}$$
$$x = C_{in}/(C_{in} + C_{GD})$$

In order to compensate for the nonlinearities the input capacitances design values can be predistorted to account for this in the following way:

1- C_{in} in all the FGMOS transistors with one diode connected input (M1, M2 and M4) is designed to have a value C_{in}-C_{GD} instead.

2- In the diode connected transistors an extra input is added with associated capacitance value C_{GD}, and connected to ground.

The resulting output current with these new design values is:

$$I_{out} = \frac{I_{in1} \times I_{in2}}{I_b} \cdot e^{\frac{C_{GD}}{C_T}\frac{V_3}{nU_T}} \tag{18}$$

Equation (18) shows how the exponents of the input currents are equal to one, as wanted, and the only second order remaining term corresponds to the output resistance of the circuit which is reduced as expected

due to the parasitic coupling between the output node and the FG of the output transistor. Should this effect be critical it can be compensated for by adding a cascode transistor at the output (only). Although in general this strategy is not recommended since it increases the minimum power supply voltage demand for the circuit, in this case it would not be a problem. If properly biased, the cascode transistor should not increase the minimum power supply voltage constraint since the latter is mostly going to be determined by the diode-connected devices.

An alternative method to completely eliminate the effect of the output parasitic capacitances would be to design the circuit as follows:

1-C_{in} in all the FGMOS transistors with one diode connected input (M1, M2 and M4) is designed to have a value C_{in}-C_{GD} instead.

2- An extra input is added to all the diode connected transistors, except for the bias one, M1, with associated capacitance value C_{GD}, and connected to ground.

3- An extra input is added to the bias device, M1, with associated capacitance value C_{GD}, which is connected to the output of the circuit.

In this case the output current will be given by:

$$I_{out} = \frac{I_{in1} \times I_{in2}}{I_b} \tag{19}$$

The same principle, explained for the one quadrant multiplier/divider can be applied to the four quadrant multiplier/two quadrant divider in Figure 2(b) with slight modifications:

1-The core transistors, M2, M4, M5 and M6 are designed as explained before.

2- The current mirrors have to be designed as shown in Figure 3, this is sharing the FG and inputs.

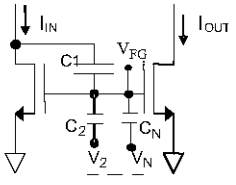


Figure 3: Implementation of FGMOS current mirrors with improved output resistance

It can be proven that the output resistance of this kind of implementation is given by:

$$R_{out} = \left[\left(1 + \frac{C_{GD}}{\sum_{i=[1,N]} C_i} \right) g_{ds} \right]^{-1} \tag{20}$$

as opposed to:

$$R_{out} = \left(g_{ds} + g_m \frac{C_{GD}}{C_T} \right)^{-1} \tag{21}$$

for a FGMOS current mirror with FGs disconnected. g_{ds} is the conductance of the MOS transistor used to design the FGMOS and g_m is its transconductance. Equation (21) shows how the output resistance seriously decreases with respect to the output resistance of a normal MOS current mirror since g_m is much larger than g_{ds}. On the contrary, eq.(20) predicts a very small degradation since in general even for small values of input capacitances, $C_{GD} << \sum_{i=[1,N]} C_i$.

5. Results

The circuit in Fig.2(a) was designed in a 0.35μm AMS technology. The aspect ratio of the n-channel FGMOS transistors was 5μm/5μm, whereas the p-channel MOS devices were 5μm/10μm. The values of the input capacitances were 67.5fF (for the diode connected inputs) and 70fF for the rest. The performance is summarized in Table I. The values of distortion have been obtained for a modulation index (ratio between the peak amplitude of the input signal and bias signal) of 0.9. The bias current was set to 10nA and the voltage supply to 0.9V. Figure 4 shows the output current for the multiplier when I_{in1} ranges from -5nA to 5nA and I_{in2} from -4.5nA to 4.5nA. The output characteristic for the divider is shown in Fig.5. for I_{in1}=4.5nA and I_b ranging between 6nA and 10nA.

Table I: Summary of performance for the multiplier in Figure 2(b)

-3 dB point	80k Hz
THD @ 1 Hz	0.162%
THD @ 10 Hz	0.164
THD @ 100 Hz	0.19%
THD @ 1k Hz	0.313%
Power Consumption	87.2 nW
Noise (referred to input) 1Hz to 160k Hz	24.4pA
Dynamic Range	45.2 dB

The performance of this multiplier was compared by simulation to other very low power state of the art realizations found in literature. The best performing low power realization was the one presented in [5]. The results for the latter are shown in Table II. It can be seen how for the multiplier in Figure 2(b), designed using the predistortion technique in the FGMOS transistors, the maximum level of distortion is 0.3% measured at 1kHz whereas it is more than 1% for the multiplier in [5]; the equivalent noise level is around five time smaller; and the power consumption is in the order of three times lower.

Table II: Summary of performance for multiplier in [5]

	Input Iin1	Input Iin2
-3 dB point	45kHz	130kHz
THD@10 Hz	0.88%	0.43%
THD@100 Hz	1.03%	0.64%
THD@1KHz	1.12%	0.69%
Power Consumption	214.5nW	
Noise (referred to input) (1Hz to -3dB frequency)	126 pA	147 pA
Dynamic Range	37 dB	35.7 dB

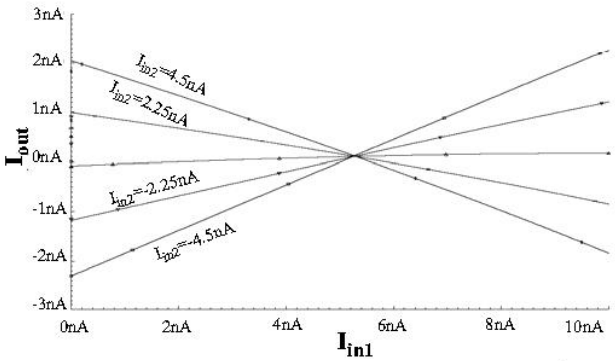


Figure 4: Output current for the multiplier in Figure 2(b)

Another comparative example is the Gilbert multiplier simulated an implemented in [6]. The power consumption required for this circuit to operate with the same Dynamic Range as the topology proposed here was 560nW, this is six times larger than the current work.

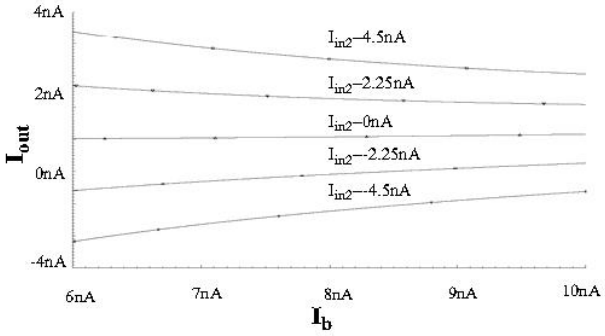


Figure 5: Output current for the integrator in Figure 2(b)

5. Conclusions

A low power and low voltage wide range four quadrant multiplier/two quadrant divider has been presented. The circuit is based on the use of FGMOS transistors implementing the translinear function. The circuit achieves a much larger input range for the same levels of power than other state of the art realizations. This is obtained by applying a predistortion technique consisting on having different value input capacitances in the diode connected transistors, and improved output resistance FGMOS current mirrors. This technique also avoids the use of cascode transistors in the most voltage demanding circuit branches.

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