Consumer Microcircuits Limited

M-I-X-E-D S-I-G-N-A-L S-O-L-U-T-I-O-N-S

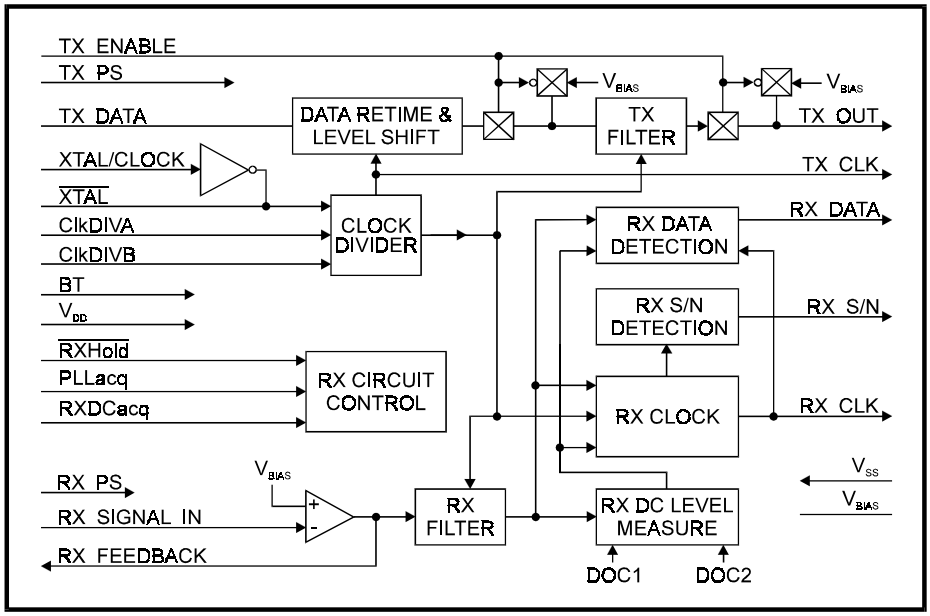
CMX589A

GMSK Modem

D/589A/3 September 1998 Provisional Information

Features and Applications

- **Data Rates from 4kbps to 200kbps**
- **Full or Half Duplex Gaussian Filter and Data Recovery for Minimum Shift Keying (GMSK) Designs**
- **Selectable BT: (0.3 or 0.5)**
- **Low Power**
  - **3.0V, 20kbps, 1.5mA typ.**
  - **5.0V, 64kbps, 4.0mA typ.**
- **Low Current Non-DSP Solution**
- **Small TSSOP Packs fit PCMCIA/PC Cards**
- **Portable Wireless Data Applications**
  - **Cellular Digital Packet Data (CDPD)**
  - **Mobitex™ Mobile Data System**
- **Spread Spectrum Data Links**
- **GPS/Differential GPS Wireless Links**
- **Point-of-Sale Terminals**
- **Low Power Wireless Data Link for PCs, Laptops, and Printers**



Brief Description

The CMX589A is a single-chip synchronous data pump/modem designed for Wireless Data Applications. Employing Gaussian filtering for Minimum shift Keying (GMSK) baseband modulation applications, the CMX589A features a wide range of available data rates from 4k to 200k bps. Data Rates and the choice of BT (0.3 or 0.5) are pin programmable to provide for different system requirements.

The Tx and Rx digital data interfaces are bit serial, synchronized to generated Tx and Rx data clocks. Separate Tx and Rx Powersave inputs allow full or half-duplex operation. Rx input levels can be set by suitable AC and DC level adjusting circuitry built with external components around an on-chip Rx Input Amplifier.

Acquisition, Lock, and Hold of Rx data signals are made easier and faster by the use of Rx Control Inputs to clamp, detect, and /or hold input data levels and can be set by the µProcessor as required. The Rx S/N output provides an indication of the quality of the received signal.

The CMX589A may be used with a 3.0V to 5.5V power supply and is available in the following packages: 24-pin TSSOP (CMX589AE2), 24-pin SSOP (CMX589AD5), 24-pin SOIC (CMX589AD2), and 24-pin PDIP (CMX589AP4).

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Block Diagram

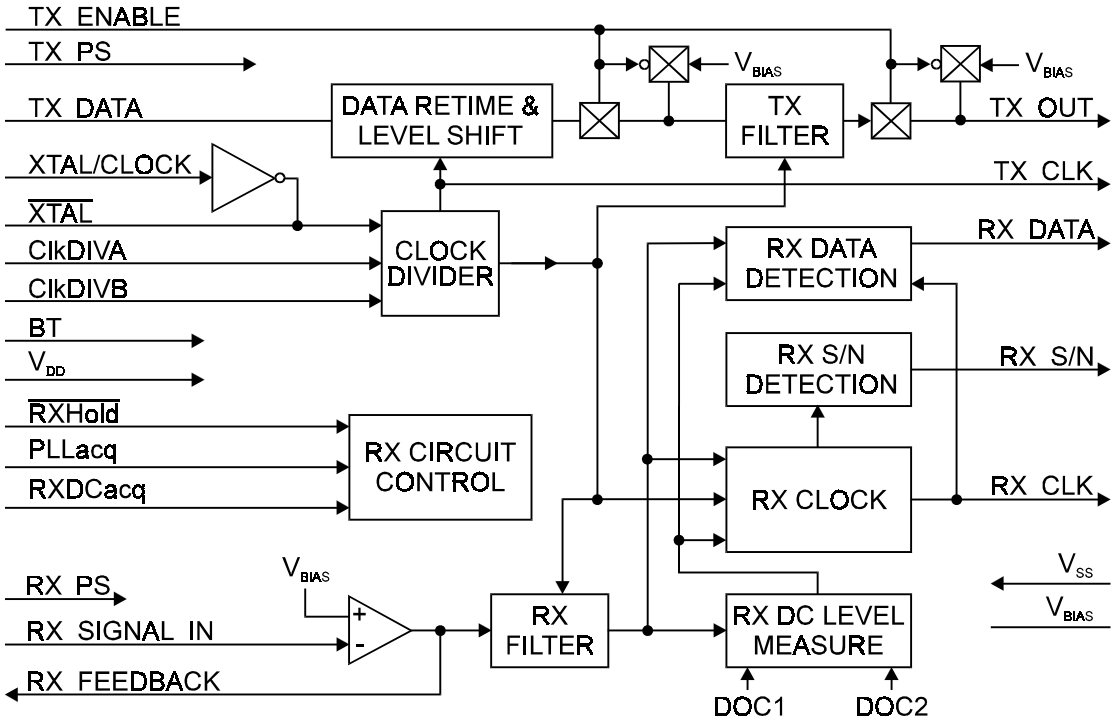

Figure 1: Block Diagram

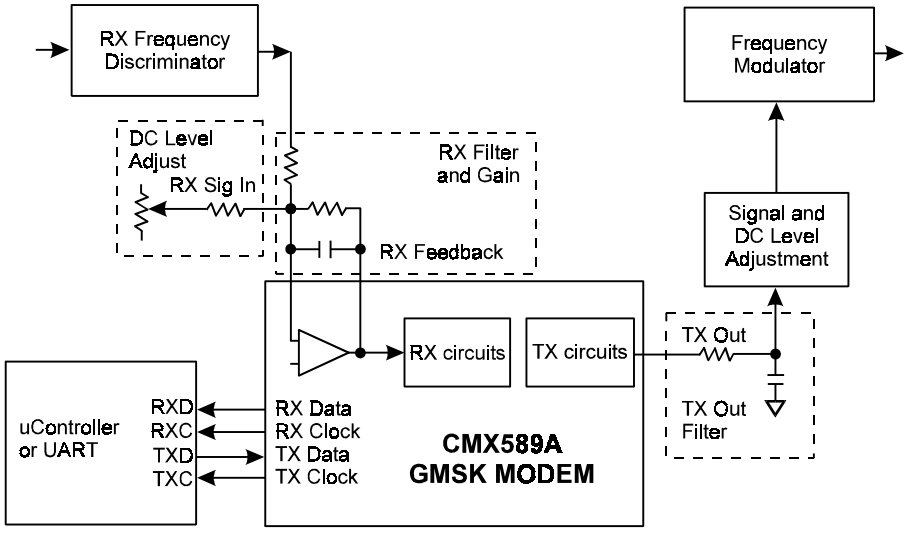

Figure 2: System Block Diagram

2 Signal List

Pin No. E2/D5/ D2/P4	Signal	Type	Description
1	XTALN	O/P	The output of the on-chip clock oscillator.
2	XTAL/CLOCK	I/P	The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock (f_{XTAL}) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the XTALN pin left unconnected. Note: Operation without a suitable Xtal or clock input may cause device damage.
3	ClkDivA	I/P	Logic level inputs control the internal clock divider and therefore the transmit and receive data rate. See Table 4.
4	ClkDivB	I/P	Logic level inputs control the internal clock divider and therefore the transmit and receive data rate. See Table 4.
5	RxHOLDN	I/P	A logic ‘0’ applied to this input will freeze the Clock Extraction and Level Measurement circuits unless they are in ‘Acquire’ mode.
6	RxDCacq	I/P	A logic ‘1’ applied to this input will set the Rx Level Measurement circuitry to the ‘Acquire’ mode. See Table 6.
7	PLLacq	I/P	A logic ‘1’ applied to this input will set the Rx Clock Extraction circuitry to the ‘Acquire’ mode. See Table 5.
8	Rx PSAVE	I/P	A logic ‘1’ applied to this input will powersave all receive circuits except for Rx CLK output (which will continue at the set bit-rate) and cause the Rx Data and Rx S/N outputs to go to a logic ‘0’.
9	V_{BIAS}		The internal circuitry bias line, held at $V_{DD}/2$. This pin must be bypassed to V_{SS} by a capacitor mounted close to the pin.
10	Rx FB	O/P	Output of the Rx Input Amplifier.
11	Rx Signal In	I/P	Input to Rx input amplifier.
12	V_{SS}	power	Negative supply (GND).
13	DOC1		Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from this pin to V_{SS}.
14	DOC2		Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from this pin to V_{SS}.
15	BT		A logic level to select the modem BT (the ratio of the Tx Filter's -3dB frequency to the Bit-Rate). A logic ‘1’ = BT of 0.5 and a logic ‘0’ = BT of 0.3.

Pin No. E2/D5/ D2/P4	Signal	Type	Description
16	Tx Out	I/P	Gaussian filtered Tx output signal. In powersave mode the Tx Out pin is high impedance.
17	Tx Enable	I/P	A logic '1' applied to this input, enables the transmit data path, through the Tx Filter to the Tx Out pin. A logic '0' will place the Tx Out pin to V_{BIAS} via a high impedance.
18	Tx PSAVE	I/P	A logic '1' applied to this input will powersave all transmit circuits except for the Tx Clock.
19	Tx Data	I/P	The logic level input for the data to be transmitted. This data should be synchronous with Tx CLK.
20	Rx Data	I/P	A logic level output carrying the received data, synchronous with Rx CLK.
21	Rx CLK	I/P	A logic level clock output at the received data bit-rate.
22	Tx CLK	I/P	A logic level clock output at the transmit data bit-rate.
23	Rx S/N	O/P	A logic level output which may be used as an indication of the quality of the received signal.
24	V_{DD}	power	Positive supply. Levels and voltages within the device are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the pin.

Table 1: Signal List

3 External Components

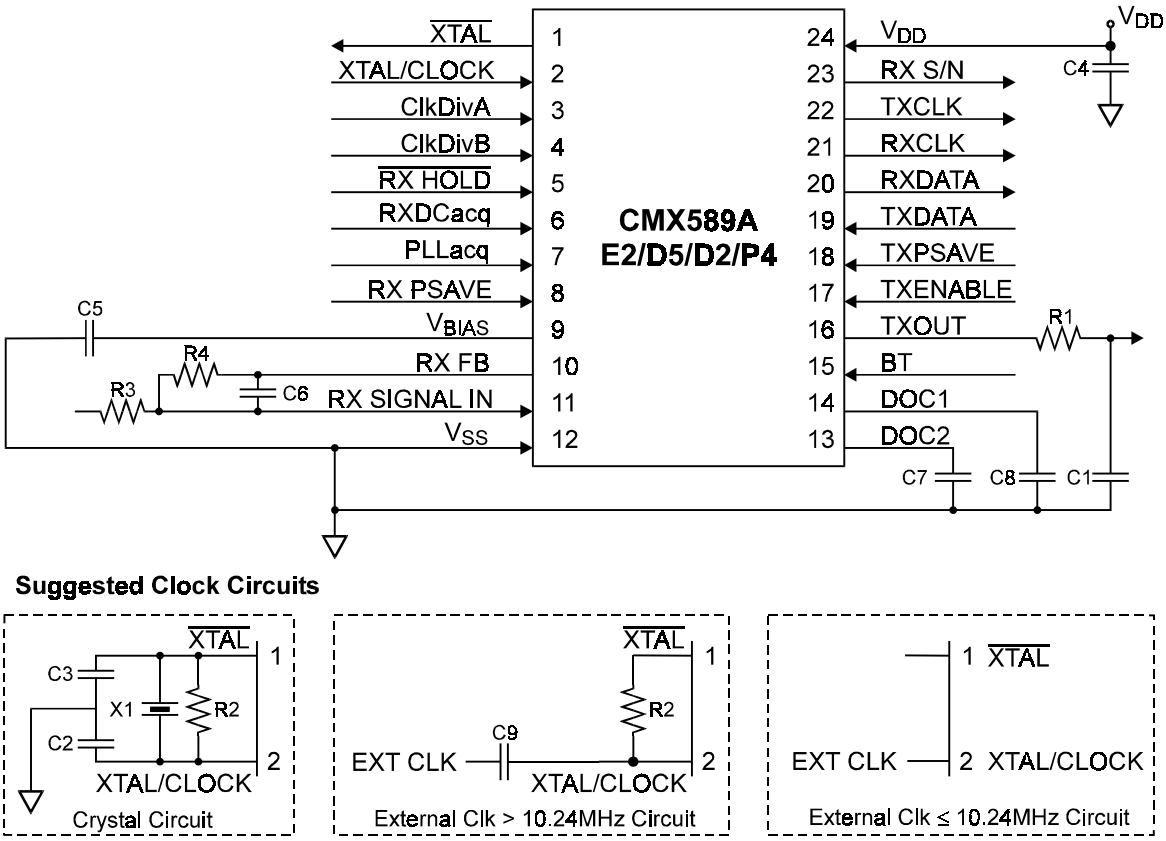

Figure 3: Recommended External Components

Component	Notes	Value	Tolerance
R1	1		±5%
R2		1.0MΩ	±10%
R3	2		±10%
R4	3		±10%
C1	1		±10%
C2	4		
C3	4		

Component	Notes	Value	Tolerance
C4		0.1µF	±20%
C5		1.0µF	±20%
C6	5		±20%
C7	6		
C8	6		
X1	8		

Table 2: Recommended External Components

Recommended External Component Notes:

1. The RC network formed by R1 and C1 is required between the Tx Out pin and the input to the modulator. This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.
   The component values should be chosen so that the product of the resistance and the capacitance is:

   For a BT of 0.3 R1C1 = 0.34/bit rate (bps)
   For a BT of 0.5 R1C1 = 0.22/bit rate (bps)

Data Rates (kbps)	BT = 0.3		BT = 0.5	
	R1	C1	R1	C1
4	120kΩ	680pF	120kΩ	470pF
4.8	100kΩ	680pF	100kΩ	470pF
8	91kΩ	470pF	120kΩ	220pF
9.6	91kΩ	390pF	47kΩ	470pF
16	47kΩ	470pF	91kΩ	150pF
19.2	100kΩ	180pF	91kΩ	120pF
32	47kΩ	220pF	47kΩ	150pF
38.4 *	47kΩ	180pF	47kΩ	120pF
64 *	56kΩ	100pF	51kΩ	68pF
80 *			39kΩ	68pF
128 *			82kΩ	22pF
144 *			68kΩ	22pF
160 *			62kΩ	22pF
176 *			56kΩ	22pF
192 *			51kΩ	22pF
* $V_{DD} \geq 4.5V$, external clock				

Table 3: Data Rate vs. BT and Selected External Component Values

Note: In all cases, the value of R1 should not be less than 20.0kΩ, and that the calculated value of C1 includes calculated parasitic capacitance.

2. R3, R4 and C6 form the gain components for the Rx Input signal. R3 should be chosen as required by the signal input level.
3. For bit rate ≤ 64kbps, R4 = 100kΩ. For bit rate > 64kbps, R4 = 10kΩ.
4. The values chosen for C2 and C3 (including stray capacitance), should be suitable for the applied V_{DD} and the frequency of X1.
   As a guide: C2 = C3 = 33pF at 1.0MHz falling to 18pF at the maximum frequency.
   At 3.0V, C2 = C3 = 33pF falling to 18pF at 5.0MHz the equivalent series resistance of X1 should be less than 2.0KΩ falling to 150Ω at the maximum frequency. Stray capacitance on the Xtal/Clock circuit pins must be minimized.
5. For bit rate ≤ 64kbps, C6 = 22pF. For bit rate > 64kbps, C6 = $\frac{1}{3 \times \text{bit rate} \times 2\pi \times 10\text{k}\Omega}$
   e.g. for 128kbps, C6 = 41.1pF.
6. C7 and C8 should both be .015µF for a data rate of 8kbps, and inversely proportional to the data rate for other data rates, e.g. 0.030µF at 4kbps, 1800pF at 64kbps, 680pF at 192kbps.
7. The tolerance of C9 is not very critical because it primarily serves as a dc blocking capacitor.
8. The CMX589A can operate correctly with the Xtal frequencies between 1.0MHz and 16.0MHz (V_{DD} = 5.0V) and 1.0MHz to 5.0MHz (V_{DD} = 3.0V). External clock frequencies up to 25.6MHz ($V_{DD} \geq 4.5V$) are also supported (See Table 4 for examples.) For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

4 General Description

4.1 Clock Oscillator Divider

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the XTALN pin as generated by the on-chip Xtal oscillator, with external components, or supplied from an external source.

The division ratio is controlled by the logic level inputs on ClkDivA and ClkDivB pins as shown in Table 4, together with an indication of how various standard data rates may be derived from common µP Xtal frequencies.

$$\text{Data Rate} = \frac{\text{Xtal/Clk Frequency}}{\text{Division Ratio (ClkDiv A/B)}}$$

			Xtal/Clock Frequency (MHz)					
			24.576*	8.192	4.9152	4.096	2.4576	2.048
Inputs						12.288/3	12.288/5	6.144/3
ClkDivA	ClkDivB	Xtal/Clk Freq / Data Rate	Data Rate (kbps)					
0	0	128	192*	64*	38.4*	32	19.2	16
0	1	256	96*	32	19.2	16	9.6	8
1	0	512	48*	16	9.6	8	4.8	4
1	1	1024	24*	8	4.8	4		

* $V_{DD} \geq 4.5V$, external clock

Table 4: Example Clock/Data Rates

Note: The device operation is not guaranteed above 200kbps or below 4kbps at the relevant supply voltage.

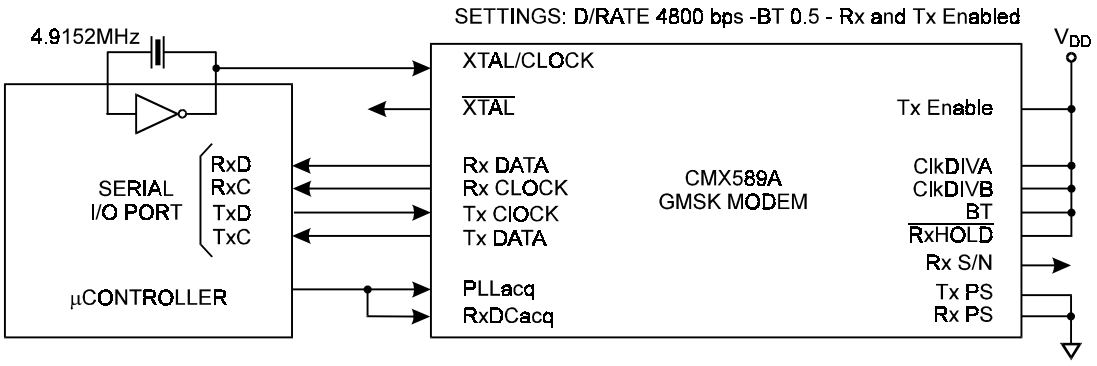

Figure 4: Minimum µController System Connections

4.2 Receive

4.2.1 Rx Signal Path Description

The function of the Rx circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide dc level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide Rx data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the CMX589A's Rx Filter by a suitable gain and DC level adjusting circuit. This circuit can be built with external components around the on-chip Rx Input Amplifier. The gain should be set so that the signal level at the Rx Feedback pin is nominally 1V peak to peak (for V_{DD}=5.0V) centered around V_{BIAS} when receiving a continuous 1111000011110000.. data pattern.

Positive going signal excursions at Rx Feedback pin will produce a logic ‘0’ at the Rx Data Output. Negative going excursions will produce a logic ‘1’.

The received signal is fed through the lowpass Rx Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors, one of which measures the amplitude of the positive parts of the received signal. The other measures the amplitude of the negative portions. (Positive refers to signal levels higher than V_{DD}/2, and negative to levels lower than V_{DD}/2.) External capacitors are used by these detectors, via the Doc1 and Doc2 pins, to form voltage ‘hold’ or ‘integrator’ circuits. These two levels are then used to establish the optimum DC level decision-thresholds for the Clock and Data extraction, depending upon the Rx signal amplitude and any DC offset.

4.2.2 Rx Circuit Control Modes

The operating characteristics of the Rx Level Measurement and Clock Extraction circuits are controlled, as shown in Table 6, by logic level inputs applied to the PLLacq, Rx HOLDN and RxDCacq pins to suit a particular application, or to cope with changing reception conditions, reference Figure 5.

In general, a data transmission will begin with a preamble, for example, 1100110011001100, to allow the receive modem to establish timing and level-lock as quickly as possible. After the Rx carrier has been detected, and during the time that the preamble is expected, the RxDCacq and PLLacq Inputs should be switched from a logic ‘0’ to a logic ‘1’ so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The Rx HOLDN input should normally be held at a logic ‘1’ while data is being received, but may be driven to a logic ‘0’ to freeze the Level Measuring Clock Extraction circuits during a fade. If a fade lasts for less than 200 bit periods, normal operation can be resumed by returning the Rx HOLDN input to a logic ‘1’ at the end of the fade. For longer fades, it may be better to reset the Level Measuring circuits by placing the RxDCacq to a logic ‘1’ for 10 to 20 bit periods.

Rx HOLDN has no effect on the Level Measuring circuits while RxDCacq is at a logic ‘1’, and has no effect on the PLL while PLLacq is at a logic ‘1’.

A logic ‘0’ on Rx HOLDN does not disable the Rx Clock output, and the Rx Data Extraction and S/N Detector circuits will continue to operate.

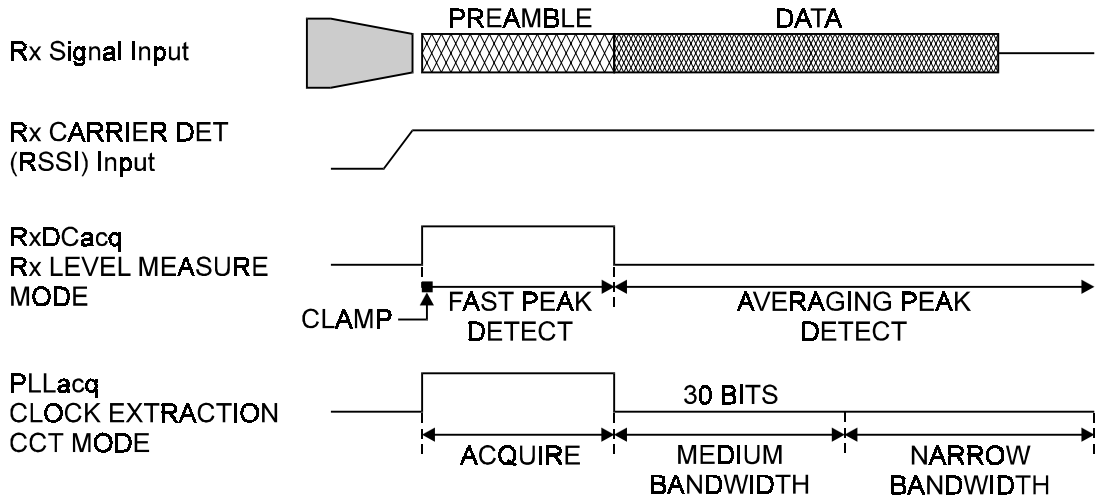

Figure 5: Rx Mode Control Diagram

PLLacq	Rx HOLDN	PLL Action	
1	1	Acquire	Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. This mode will operate as long as PLLacq is a logic “1”.
1 to 0	1	Medium Bandwidth	The correction applied to the extracted clock is limited to a maximum of ±1/16th bit-period for every two received zero-crossings. The PLL operates in this mode for a period of about 30 bits immediately following a 1 to 0 transition of the PLLacq input, provided that the Rx HOLDN input is a logic ‘1’.
0	1	Narrow Bandwidth	The correction applied to the extracted clock is limited to a maximum of ±1/64th bit-period for every two received zero-crossings. The PLL operates in this mode whenever the Rx HOLDN Input is a logic ‘1’ and PLLacq has been a logic ‘0’ for at least 30 bit periods (after Medium Bandwidth operation for instance).
0	0	Hold	The PLL feedback loop is broken, allowing the Rx Clock to freewheel during signal fade periods.

Table 5: PLL Action Measurement Operational Modes

RxDCacq	Rx HOLDN	Rx Level Measure Action	
0 to 1	X	Clamp	Operates for one bit-time after a 0 to 1 transition of the RXDCacq input. The external capacitors are rapidly charged towards a voltage mid-way between the received signal input level and V_{BIAS}, with the charge time-constant being of the order of 0.5 bit-time.
1	X	Fast Peak Detect	The voltage detectors act as peak-detectors, one capacitor is used to capture the positive-going signal peaks of the Rx Filter output signal and the other capturing the negative-going peaks. The detectors operate in this mode whenever the RXDCacq input is at a logic ‘1’, except for the initial 1-bit Clamp-mode time.
0	1	Averaging Peak Detect	Provides a slower but more accurate measurement of the signal peak amplitudes.
0	0	Hold	The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000 bits] towards V_{BIAS}).

X = Do not care

Table 6: Rx Level Measurement Operational Modes

4.2.3 Rx Clock Extraction

Synchronized by a PLL circuit to zero-crossings of the incoming data, the Rx Clock Extraction circuitry controls the Rx Clock output. The Rx Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the Rx Circuit Control inputs PLLacq and Rx HOLDN to operate in one of four PLL modes as described in Table 5 and Table 6.

4.2.4 Rx Data Extraction

The Rx Data Extraction circuit decides whether each received bit is a 1 or 0 by sampling the received signal, after filtering, and comparing the sample values to an adaptive threshold derived from the Level Measuring circuit. This threshold is adapted from bit to bit to compensate for intersymbol interference caused by the and limiting of the overall transmission path and the Gaussian premodulation filter. Extracted data is output from the Rx Data pin, and should be sampled externally on the rising edge of the Rx CLK.

4.2.5 Rx S/N Detection

The Rx S/N Detector system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the Rx S/N pin. A high level indicates a series of GOOD crossings; a low level indicates a BAD crossing.

By averaging this output, it is possible to derive a measure of the Signal-to-Noise-Ratio and hence the Bit-Error-Rate of the received signal.

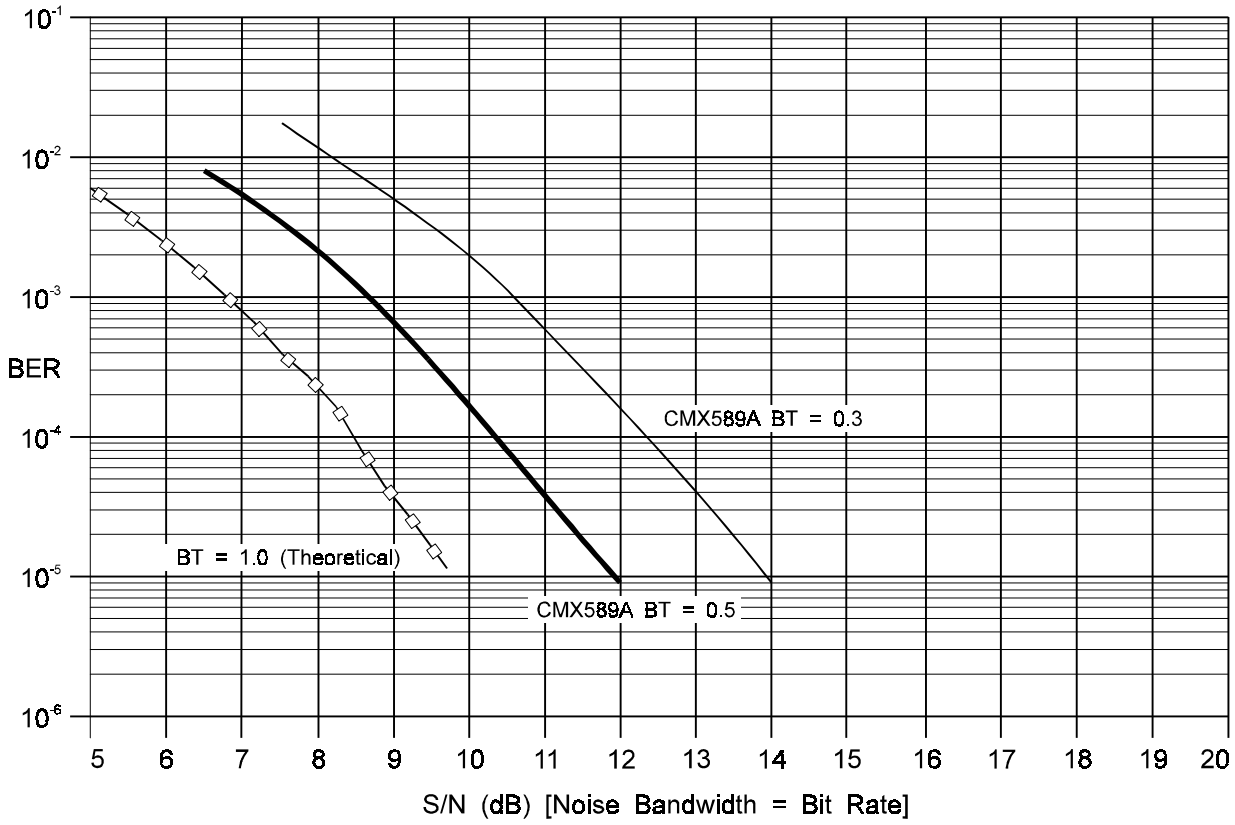

Figure 6: Typical Bit-Error-Rate Performance at V_{DD} = 5.0V

Note: Figure 6 indicates typical performance, independent of bit rate (although the applied noise bandwidth is considered to match the bit rate used), radio performance (e.g. IF filter distortion), supply voltage (higher bit rates require $V_{DD} \geq 4.5V$), and other 'real world' factors.

4.2.6 Rx Signal Quality

The effect of input Rx Signal quality on the Rx S/N output is shown in Figure 7.

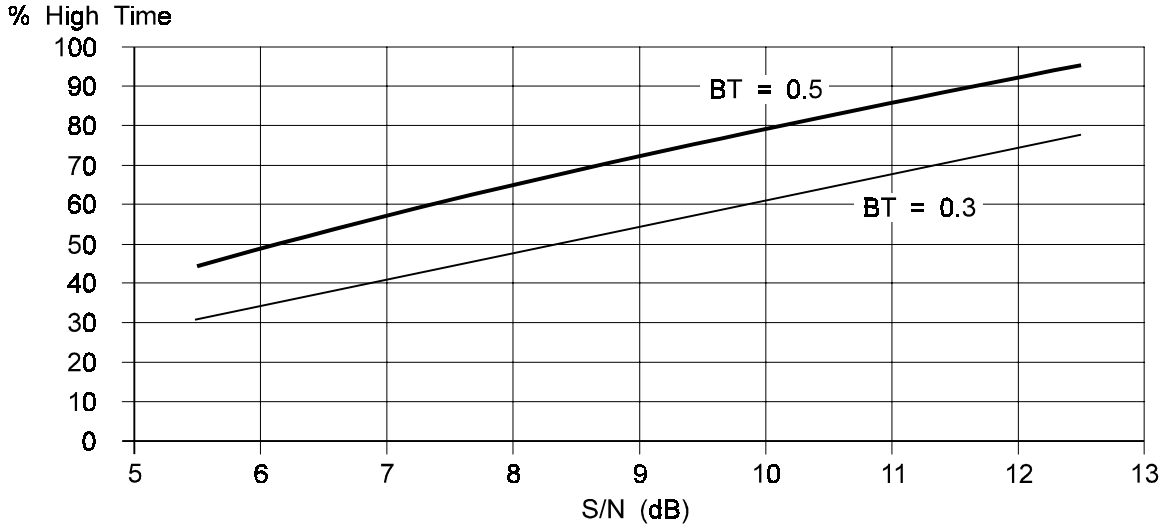

Figure 7: Typical Rx S/N Output High Time (%) vs. Input S/N

4.3 Transmit

4.3.1 Tx Signal Path Description

The binary data applied to the Tx Data input is retimed within the chip on each rising edge of the Tx Clock and then converted to a 1-volt peak-to-peak binary signal centred at V_{BIAS} (for V_{DD}= 5.0V)

If the Tx Enable input is high, then this internal binary signal will be connected to the input of the Lowpass Tx Filter, and the output of the filter connected to the Tx Out pin.

Tx Enable	Tx Filter Input	Tx Out Pin
1	Data @ $\frac{V_{DD}}{5}$ V_{P-P} e.g. 1V_{P-P} for V_{DD}=5V	Filtered 'Tx Filter Input'
0	V_{BIAS}	V_{BIAS} via 500kΩ

A 'low' input to the Tx Enable will connect the input of the Tx Filter to V_{BIAS}, and disconnect the Tx Out pin from the filter, connecting it instead to V_{BIAS} through a high resistance (nominally 500kΩ).

The Tx Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimize amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs.-frequency response of the transmit filtering provided by the CMX589A has been designed to meet the specifications for most GMSK modem systems that are -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

Note: An external RC network is required between the Tx Out pin and the input to the Frequency Modulator (see Figure 2 and Figure 3). This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.