The signal at Tx Out is centered around V_{BIAS}, going positive for logic '1' (high) level inputs to the Tx Data input and negative for logic '0' (low) inputs.

When the transmit circuits are put into a powersave mode (by a logic '1' to the Tx PS pin) the output voltage of the Tx Filter will go to high impedance. When power is subsequently restored to the Tx filter, its output will take several bit-times to settle. The Tx Enable input can be used to prevent these abnormal voltages from appearing at the Tx Out pin.

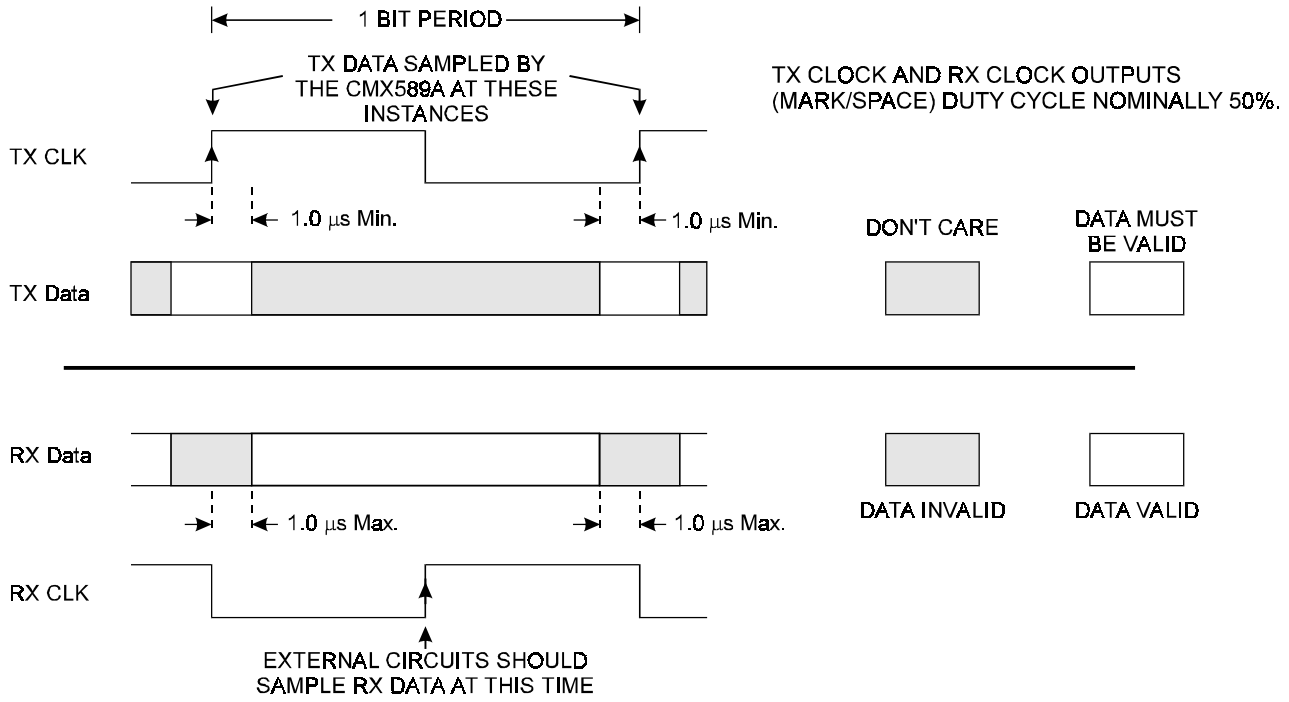


Figure 8: Rx and Tx Clock Data Timings

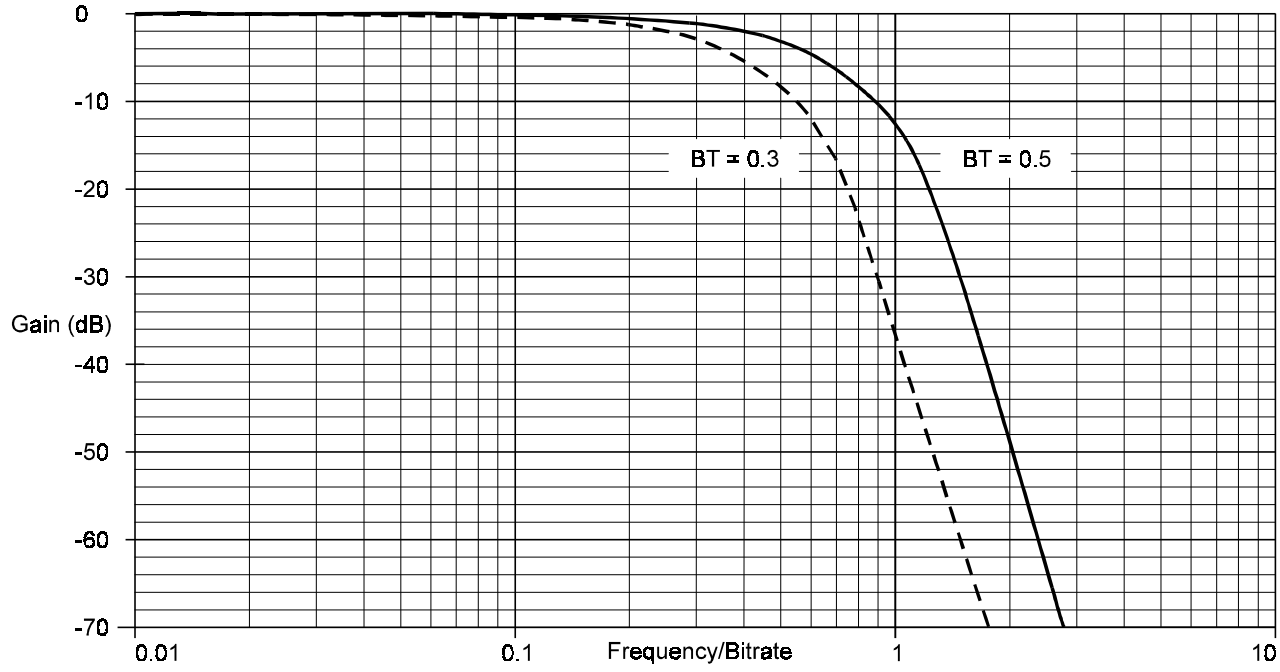


Figure 9: Tx Filter Response

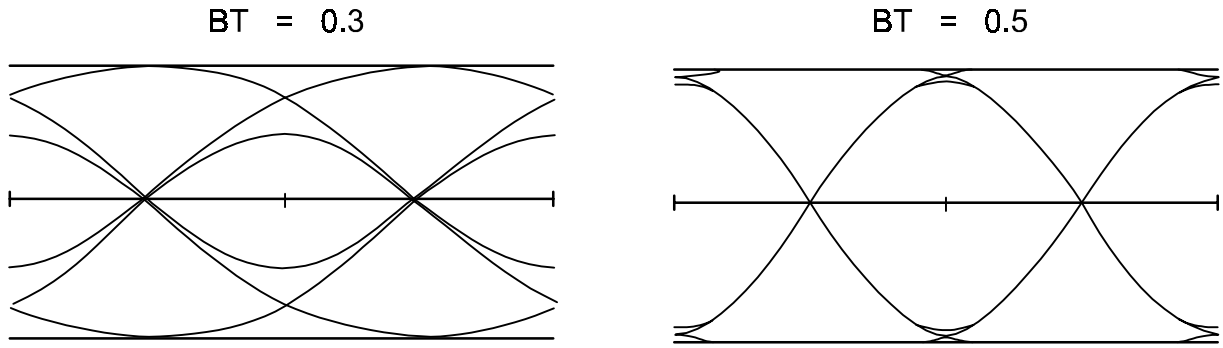


Figure 10: Typical Transmit Eye Patterns

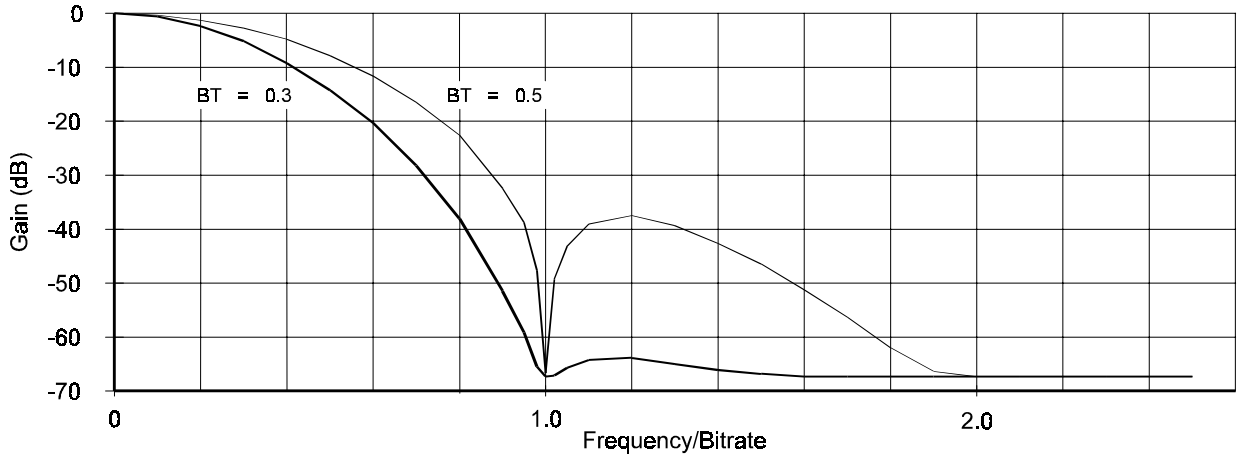


Figure 11: Tx Output Spectrum (Random Data)

4.4 Data Formats

The receive section of the CMX589A works best with data which has a reasonably random structure --the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences (>100 bits) of consecutive ones or zeroes. Also, long sequences (>100 bits) of 10101010 ... patterns should be avoided.

For this reason, it is recommended that data be made random in some manner before transmission, for example by exclusive-ORing it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble for BT=0.3 should be at least 16 bits long, and should preferably consist of alternating pairs of ones and zeros i.e. 110011001100....; the eye of pattern 10101010 .... has the most gradual slope and will yield poor peak levels for the Rx circuits. For BT=0.5 the eye pattern of 10101010... has reduced intersymbol interference and may be used as the preamble (DC Acq pin should be held high during preamble). See Figure 5.

4.5 Acquisition and Hold Modes

The RXDCacq and PLLacq inputs must be pulsed High for about 16 bits at the start of reception to ensure that the DC measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, the above inputs should be taken Low again.

In most applications, there will be a DC step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the remote transmitter is turned on.

The CMX589A can tolerate DC offsets in the received signal of at least ±10% of V_{DD} with respect to V_{BIAS}, (measured at the Rx Feedback pin). However, to ensure that the DC offset compensation circuit operates correctly and with minimum delay, the Low to High transition of the RXDCacq and PLLacq inputs should occur after the mean input voltage to the CMX589A has settled to within about 0.1V of its final value.

Note: This can place restrictions on the value of any series signal coupling capacitor.

As well as using the Rx Hold input to freeze the Level Measuring and Clock Extraction circuits during a signal fade, it may also be used in systems which use a continuously transmitting control channel to freeze the Rx circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the CMX589A Xtal clock needs to be accurate enough that the derived RxClock output does not drift by more than about 0.1 bit time from the actual received data-rate during the time that the RxHold input is 'Low'.

However; the RXDCacq input may need to be pulsed High for 2 bit durations to re-establish the level measurements if the RxHold input is Low for more that a few hundred bit-times (exact number depends on system crystal tolerances).

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.

Note: These pins are driven from very high-impedance circuits, so that the DC load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

5 Application

5.1 Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index is required. For optimum channel utilization, (e.g. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

5.1.1 Bit Rate, BT, and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on the following:

Channel spacing
Allowable adjacent channel interference
Tx filter bandwidth
Peak carrier deviation (Modulation Index)
Tx and Rx carrier frequency accuracies
Modulator and Demodulator linearity
Rx IF filter frequency and phase characteristics
Use of error correction techniques
Acceptable error-rate

As a guide to MOBITEX operation, a raw data-rate of 8kbps at 12.5kHz channel spacing may be achievable - depending on local regulatory requirements- using a ±2kHz maximum deviation, a BT of 0.3, and no more than 1.5kHz discrepancy between Tx and Rx carrier frequencies. Forward error correction (FEC) could then be used with interleaving to reduce the effect of burst errors.

Reducing the data-rate to 4.8kbps would allow the BT to be increased to 0.5, improving the error-rate performance.

5.1.2 FM Modulator, Demodulator and IF

For optimum performance, the eye pattern of the received signal (when receiving random data) applied to the CMX589A should be as close as possible to the Transmit eye pattern examples shown in Figure 10.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to:

Linearity and frequency/phase response of the Tx frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few hertz. This is because two-point modulation is necessary for synthesized radios.

Bandwidth and phase response of the Rx IF filters.

Accuracy of the Tx and Rx carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the Rx demodulator should be DC coupled to the CMX589A Rx Signal In pin (with a DC bias added to center the signal at the Rx Feedback pin at $V_{DD}/2$ [V_{BIAS}]). However, AC coupling can be used provided that:

The 3dB cut-off frequency is 20Hz or below (i.e. a 0.1µF capacitor in series with 100kΩ).

The data does not contain long sequences of consecutive ones or zeroes.

Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of a RF carrier) for the voltage into the CMX589A to settle before the RXDCacq line is strobed.

5.1.3 Two-Point Modulation

When designing the CMX589A into a radio that uses a frequency synthesizer, a two-point modulation technique is recommended. This is both to prevent the radio's PLL circuitry from counteracting the modulation process, and to provide a clean flat modulation response down to DC.

Figure 12 shows a suggested basic configuration to provide a two-point modulation drive from the CMX589A Tx Output using MX-COM's MX019 Digitally Controlled Quad Amplifier Array. The MX019 elements provide individual set-up, calibration and dynamic control of modulation levels. Level setting control of the amplifiers/attenuators of the MX019 is via an 8-bit data word. Note that the MX019 frequency response only supports data rates as high as 8kbps.

With reference to Figure 12:

The buffer amplifier is required to prevent loading of the CMX589A external RC circuit.

Stage B, with R1/R2, provides suitable signal and DC levels for the VCO varactor; C1 is RF decoupling. The drive level should be adjusted (digitally) to provide the desired deviation.

Stage C, with R3/R4, provides the Reference Oscillator drive (application dependent). This parameter is set by adjusting for minimum AC signal on the PLL control voltage with a low-frequency modulating signal (inside the PLL bandwidth) applied.

Stage D could be used with the components shown if a negative reference drive is required.

Stage A provides buffering and overall level control.

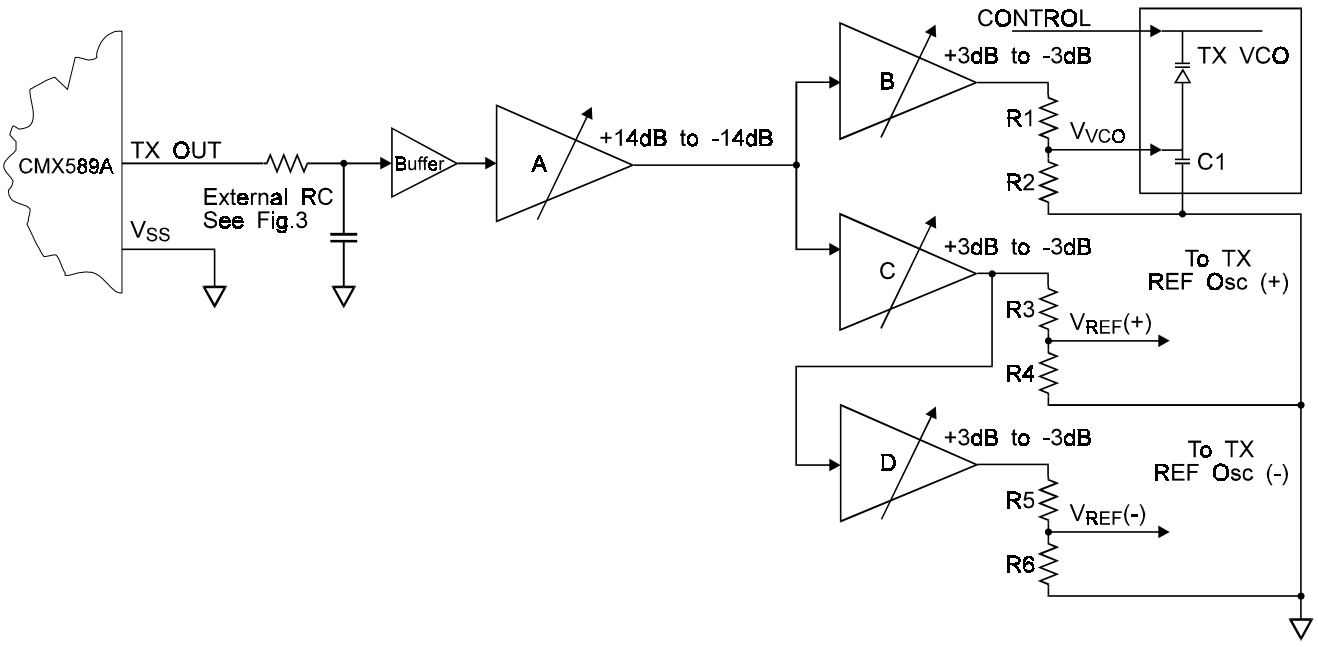


Figure 12: An Example of Two-Point Modulation Drive with Individual Adjustment Using the FX019

5.2 AC Coupling of Tx and Rx Signals

In practical applications, it is possible to arrange AC coupling between the CMX589A Tx Output and the frequency modulator to cut-off at a very low frequency, such as 5.0Hz. AC coupling between the receive discriminator and the input of the CMX589A may need a shorter time-constant to avoid problems from voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.

For these reasons, as well as to maintain reasonable BER, the optimum –3dB cut-off frequencies are around 5.0Hz in the Tx path and 20.0Hz in the Rx path.

Figure 13 shows the typical static Bit-Error-Rate performance of the CMX589A operating under nominal conditions for various degrees of AC coupling at the Rx input and the Tx output.

Data Rate = 8kbps V_{DD} = 5.0V T_{AMB} = 25°C Tx BT = 0.3

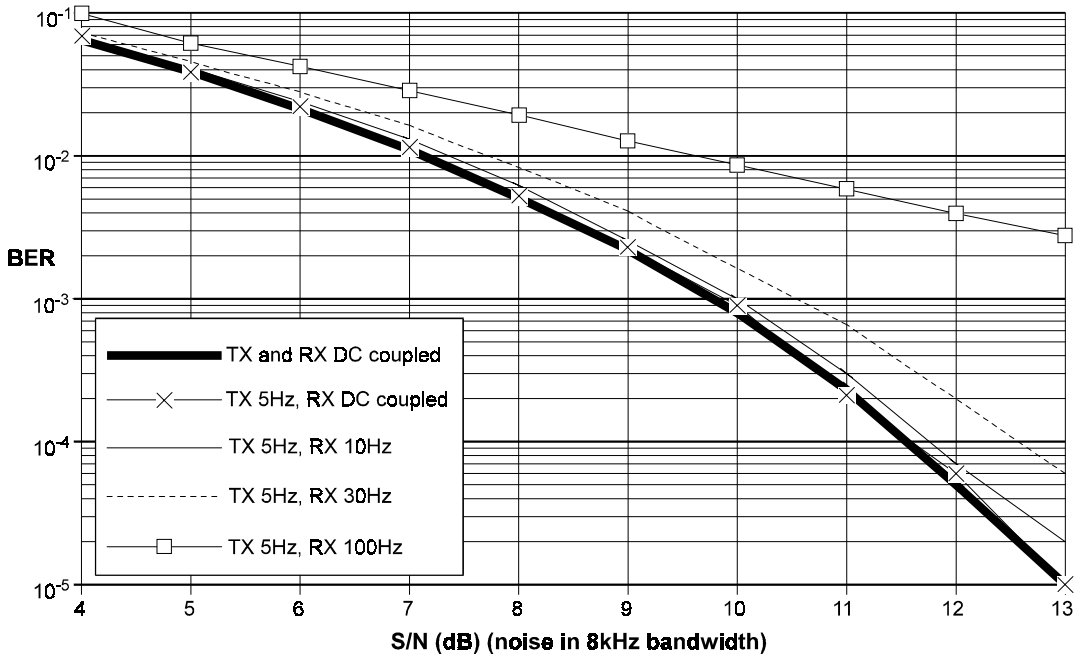


Figure 13: Effect of AC Coupling on Typical Bit-Error Rate

Any AC Coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated in Figure 14, the time for this step to decay to 37% of its original value is 'RC' where:

$$RC = \frac{1}{2\pi(\text{the 3dB cutoff frequency of the RC network})}$$

which is 32ms, or 256 bit times at 8kbps, for a 5Hz network.

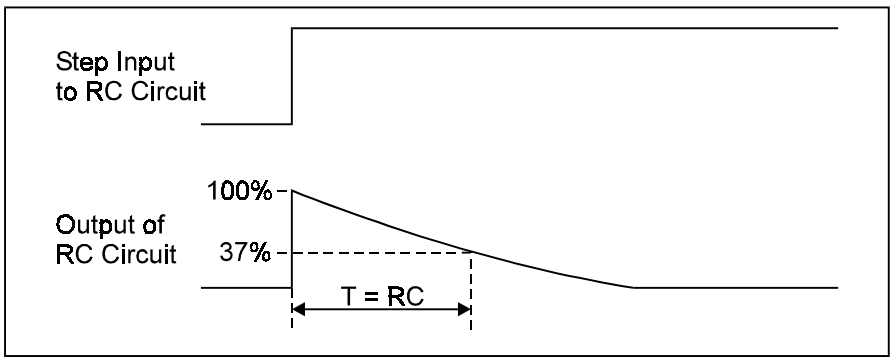


Figure 14: Decay time-AC Coupling

6 Performance Specifications

6.1 Electrical Specifications

6.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
D2 / P4 Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			13		mW/°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C
D5 Package					
Total allowable Power dissipation at T_{AMB} = 25°C				550	mW
Derating above 25°C			9		mW/°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C
E2 Package					
Total allowable Power dissipation at T_{AMB} = 25°C				320	mW
Derating above 25°C			5.3		mW/°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

Table 7: Absolute Maximum Ratings

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		3.0	3.3/5.0	5.5	V
Operating Temperature		-40		85	°C
Rx and Tx Data Rate					
$V_{DD} \geq 3.0V$		4		32	kbps
$V_{DD} \geq 4.5V$		4		200	kbps
Xtal Frequency					
$V_{DD} \geq 3.0V$		1.0		5.0	MHz
$V_{DD} \geq 4.5V$		1.0		16.0	MHz
External Clock Frequency					
$V_{DD} \geq 3.0V$	1	1.0		5.0	MHz
$V_{DD} \geq 4.5V$	1	1.0		25.6	MHz
High Pulse Width	1	15			ns
Low Pulse Width	1	15			ns

Table 8: Operating Limits

Operating Limits Notes

1. Timing for an external clock input to the Xtal/Clock pin.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.
V_{DD} = 5.0V @ T_{AMB} = 25°C
Xtal/Clock Frequency = 4.096MHz, Data Rate = 8kbps, Noise Bandwidth = Bit Rate

Static Values			**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Supply Current	Tx PS	Rx PS	1				
I_{DD} (V_{DD} = 3.0V)							
	1	1		-	0.5	-	mA
	0	1		-	1.0	-	mA
	1	0		-	1.0	-	mA
	0	0		-	1.5	-	mA
I_{DD} (V_{DD} = 5.0V)							
	1	1		-	1.0	-	mA
	0	1		-	2.0	-	mA
	1	0		-	3.0	-	mA
	0	0		-	4.0	-	mA
Input Logic Level							
Logic 1 Input Level				3.5	-	-	V
Logic 0 Input Level				-	-	1.5	V
Logic Input Current			2	-5.0	-	5.0	µA
Output Logic Level							
Logic 1 Output Level (I_{OH} = 120µA)				4.6	-	-	V
Logic 0 Output Level (I_{OL} = -120µA)				-	-	0.4	V
Transmit Parameters				-			
Tx OUT pin DC bias shift caused by change from Tx Enable = 0 to Tx Enable = 1 while Tx PSAVE = 0 at 25°C				-85.0	-	85.0	mV
Tx OUT, Output Impedance			3	-	1.0	-	kΩ
Tx Out, Level			4, 10	0.8	1.0	1.2	V_{P-P}
Output DC Offset			12	-0.125	-	0.125	V
Tx Data Delay							
BT = 0.3			5	-	2.0	2.5	bit-periods
BT = 0.5			5	-	1.5	2.0	bit-periods
Tx PS to Output-Stable time			6	-	4.0	-	bit-periods
Receive Parameters							
Rx Amplifier							
Input Impedance				1.0	-	-	MΩ
Output Impedance			7	-	10.0	-	KΩ
Voltage Gain				-	50.0	-	dB
Rx Filter Signal Input Level			8, 10	0.7	1.0	1.3	V_{P-P}
Rx Time Delay			9	-	-	3.0	bit-

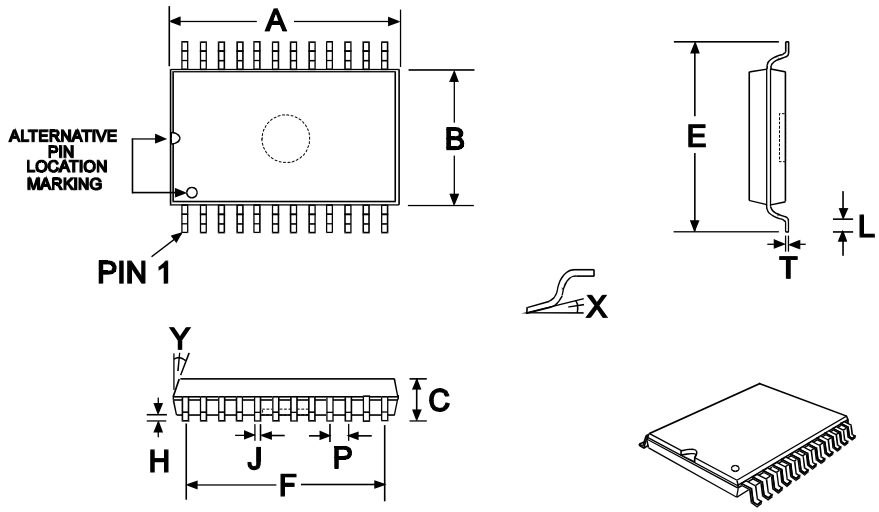
Static Values	Notes	Min.	Typ.	Max.	Units
					periods
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}	11	-	50.0	-	kΩ
Voltage Gain	11	-	25.0	-	dB

Table 9: Operating Characteristics

Operating Characteristics Notes:

1. Not including current drawn from the CMX589A pins by external circuitry. See Absolute Maximum Ratings.
2. For V_{IN} in the range V_{SS} to V_{DD}.
3. For a load of 10KΩ or greater. Tx PS input at logic '0'; Tx Enable = '1'.
4. Data pattern of 1111000011110000…
5. Measured between the rising edge of Tx Clock and the centre of the corresponding bit at Tx Out.
6. Time between the falling edge of the Tx PS and the Tx Out voltage stabilizing to normal output levels.
7. For a load of 10kΩ or greater. Rx PS input at logic '0'.
8. For optimum performance, Measured at the Rx Feedback pin for an 1111000011110000… pattern.
9. Measured between the center of bit at Rx Signal In and corresponding rising edge of the Rx Clock.
10. Levels are proportional to applied V_{DD}
11. Small signal measurement at 1.0kHz with no load on Xtal output.
12. (Tx OUT enabled DC level) – (Tx Out disabled DC level) when transmitting a repeating 11110000 bit pattern.

6.2 Packages



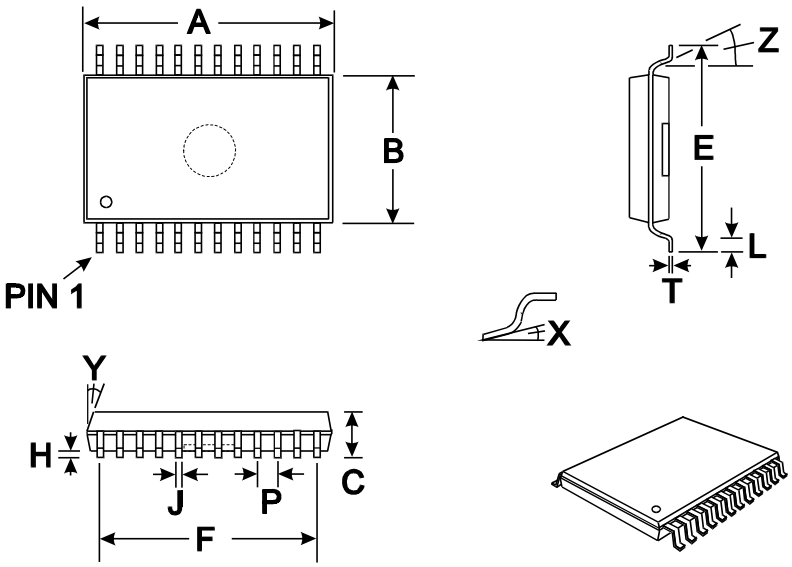
DIM.	MIN.	TYP.	MAX.
* A	0.303 (7.70)		0.311 (7.90)
* B	0.169 (4.30)		0.177 (4.50)
C	------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
F		0.286 (7.15)	
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.026 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
X	0°		7°
Y		12°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 24-pin TSSOP Mechanical Outline: ***Order as part no. CMX589AE2***



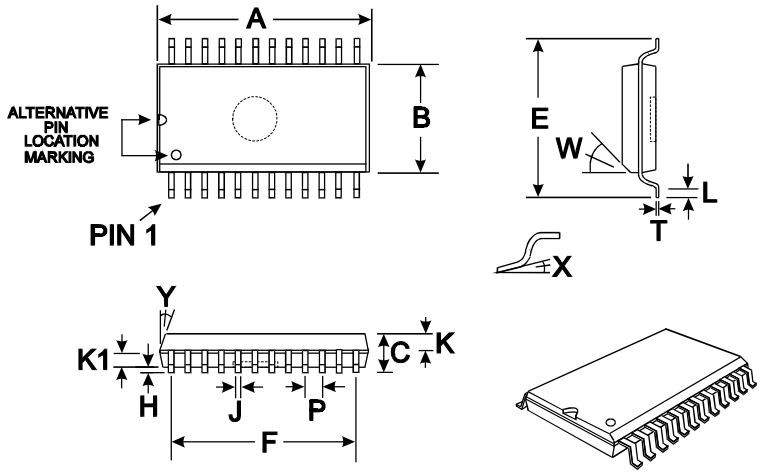
DIM.	MIN.	TYP.	MAX.
* A	0.318 (8.08)		0.328 (8.33)
* B	0.205 (5.21)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
F		0.281 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.56)		0.037 (0.94)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.23)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 24-pin SSOP Mechanical Outline: ***Order as part no. CMX589AD5***



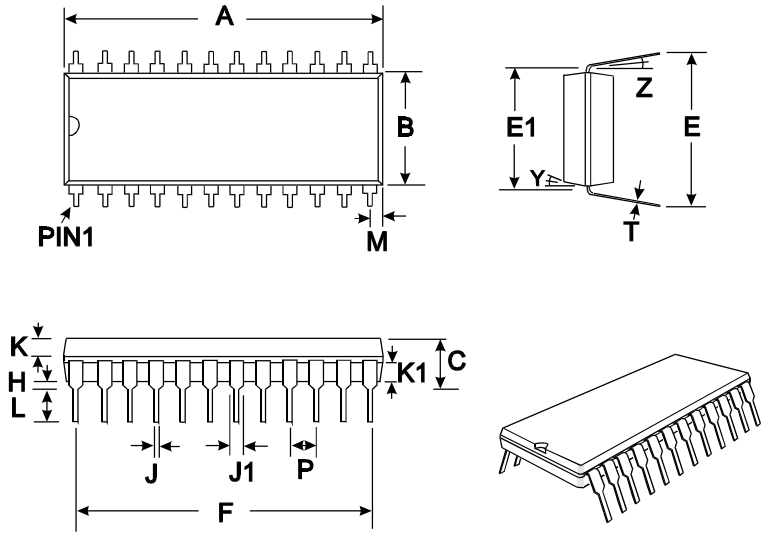
DIM.	MIN.	TYP.	MAX.
* A	0.597 (15.16)		0.613 (15.57)
* B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
F		0.550 (14.1)	
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 17: 24-pin SOIC Mechanical Outline: *Order as part no. CMX589AD2*



DIM.	MIN.	TYP.	MAX.
* A	1.200 (30.48)		1.270 (32.26)
* B	0.500 (12.70)		0.555 (14.10)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.06)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 18: 24-pin PDIP Mechanical Outline: *Order as part no. CMX589AP4*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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