DUO-MODE NON-LINEAR STATE SPACE AVERAGED SPICE MODEL OF A CURRENT MODE BUCK CONVERTER

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ABSTRACT

Although most current-programmed converters are designed for steady state continuous mode operation, transient and fault analysis require duo-mode (continuous/discontinuous) models. The popularity of SPICE (Simulation Program with Integrated Circuits Emphasis) has created a demand for non-linear state space averaged SPICE converter models because execution times of brute-force SPICE models are impractical. Fast non-linear models have been developed for duo-mode duty-ratio-programmed converters and for sinlge-mode current-programmed converters but not for duo-mode simulation of the latter. This report desribes the theory, evolution, and use of a fast, non-linear, duo-mode SPICE model of a current-programmed buck converter. A slow brute-force SPICE simulation confirmed results obtained from the fast model.

INTRODUCTION

The predominant use of current-programmed converters in the continuous mode does not preclude the need for a practical duo-mode SPICE model of current-programmed converters. Load changes, source changes, and faults could temporarily force the converter to into the discontinuous mode, and SPICE is the standard simulation program availabe on workbenches. Brute-force (pulse-by-pulse) SPICE models change modes "on the fly" but execute too slow (2-5 hours) for most applications. Such long execution times erode the workbench's analytic power. Based on the state-space-averaged models developed at Cal Tech [1], Dr. Bello of Norden Systems developed fast non-linear SPICE models for duo-mode duty-ratio-programmed converters [2] and for single-mode current-programmed converters [3]. This paper describes two methods of combining the Bello models. The first method uses double-valued gain stages to join the continuous mode current-programmed controller to its discontin uous mode counterpart. The second method replaces the double-valued gain stages with a mode-invariant control law. In either case, node-slowing circuits, buffers, zero-valued voltages sources, and soft diodes strengthen convergence and accelerate execution. We extended the composite Bello model to check loop gain Bode plots of a multiple output current-programmed buck converter. The remainder of this paper reviews the Bello models, explains how the composite Bello model evolved, states critical SPICE options, compares a composite Bello simulation to a brute-force simulation, then compares predicted and measured Bode plots of the multiple output converter.

REVIEW OF THE DUO-MODE POWER STAGE MODEL

The key to dynamic mode changing is a fictitious feedback loop that determines the inductor discharge time. For a buck converter in the discontinuous mode, the following equation relates "almost" average inductor current, i, to

input voltage, vg,
output voltage, v,
switching period, T,
inductor charge time, d*T, and
inductance, L.

$$i=(vg-v)*d*T/(2*L).$$

True average inductor current equals (d+d2)*i, where d2*T=inductor discharge time. The feedback loop nulls the difference between quantities on either side of this equation by adjusting d2. In the model, d2+d is the turns ratio of a DC transformer and

$$d2=10e6*(i-(vg-v)*d*T/(2*L))=10e6*(\text{sensed i - computed i}). \quad (1)$$

Figure 1 shows a simple schematic of the power stage model. Note that

$$i=vg*d/(R*(d+d2)^2). \quad (2)$$

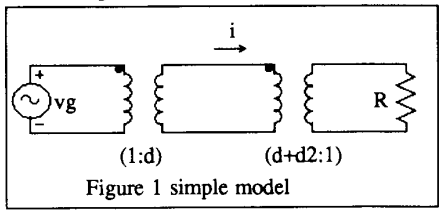

Figure 1 simple model

An increase in i causes an increase in d2 via (1), which in turn drives i back to its equilibrium point via (2). The equilibrium error equals d2/10e6. The two DC transformers enforce equations relating averaged terminal voltages. The feedback loop enforces the equation relating averaged inductor current to terminal voltages. Figure 2a shows the two transformers and the feedback loop. The circuit "sees" true averaged inductor current because the i-sensor lies between the DC transformers; the current flowing from the (d+d2) transformer towards the load equals (d+d2)*i. The feedback loop saturates at 0+ to maintain validity and convergence. To cross the mode boundary, the loop also saturates at 1-d. When d2 equals 1-d, the (d+d2) transformer's turns ratio becomes unity and therefore stops affecting the circuit. The (d) transformer continues affecting the circuit to enforce the continuous mode relationships between averaged voltages and currents. The diodes and sources in the loop impose the limits on d2. The DC supply and rightmost battery offset the diode voltage drops. Unlike the original DC supply of 1 volt, this source supplies 2 volts to keep d2 greater than zero. A negative d2 sabotages convergence.

Two more components complete the basic model: a voltage dependent resistor shorts the inductor in the discontinuous mode, and a saturation circuit keeps the duty ratio between 0 and 1. Figure 2b shows the basic power stage model.

Node C monitors error in the d2 feedback loop and indicates the conduction mode. In the discontinuous mode, the d2 feedback loop is unsaturated and consequently nulls node C's voltage. Continuous mode operation saturates the loop and releases control of node C, rendering node C's voltage non-negligible. The variable resistor circuit shunts the inductor with a resistance equal to the volage at node C in Megohms. Thus, the inductor is shunted by a small resistance in the discontinuous mode and a large resistance in the continuous mode. As discussed in the next section, node C also keeps controller gains consistent with the conduction mode.

MODEL EVOLUTION

The power stage model required minor but critical changes to strenghen convergence. The controller model required fundamental changes. The first controller model used double-valued gain stages to switch between discontinuous and continuous mode control laws. Figure 3 shows the simplest double-valued gain stage. It has either negligible or unity gain. A high control voltage creates a voltage follower whereas a low control voltage drops the output to a small fraction of the input. Two simple stages and a divider block allow arbitrary gains. The combination shown in Figure 4 has a gain of .5 for large control voltages and a gain of 1 for small control voltages. The divider, expanded in Figure 5, gives the reciprocal of the control voltage. The circuit in Figure 6 combines the circuits in Figures 3 through 5 to construct a differrent d for each conduction mode. In the continuous mode (large node C voltage),

$d = f^* (Vc-Vi) / (m+m_1/2)$.

In the discontinuous mode (small node C voltage),
$d = f^*Vc/(m+m_1)$.

Here, Vc is the control voltage, Vi is the inductor current sensor output voltgage, m_1 is the stabilizing slope, and $m=(Vg-V)/L$ in the proper units. The additional divider replaces the feedback loop in Bello's current-programmed

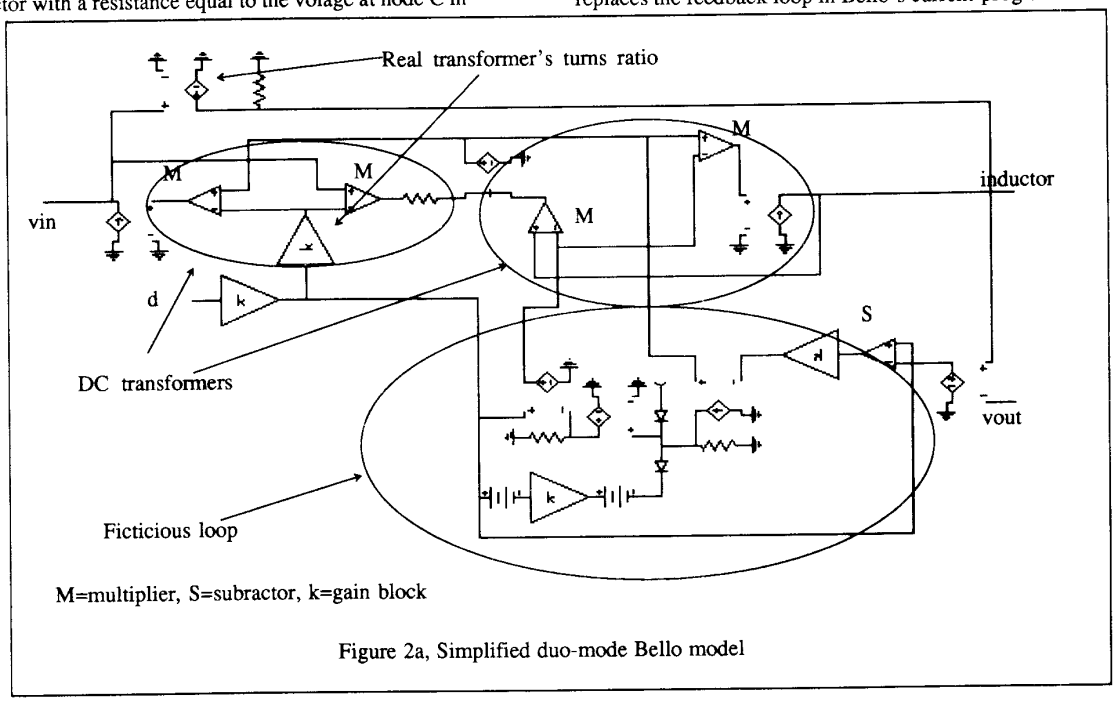

Figure 2a, Simplified duo-mode Bello model

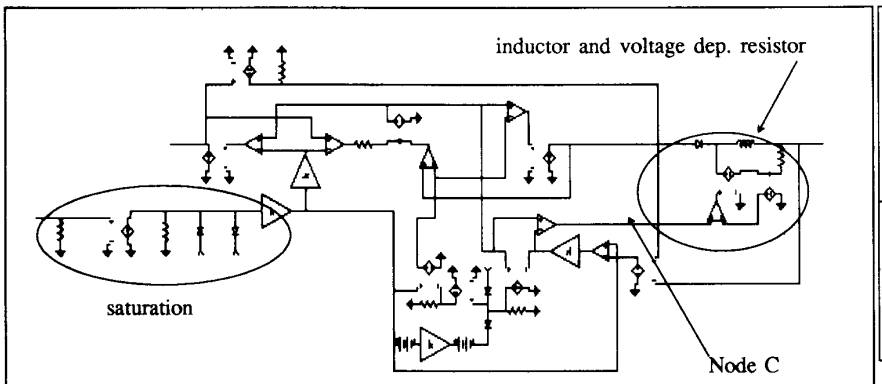

Figure 2b, Additional circuitry

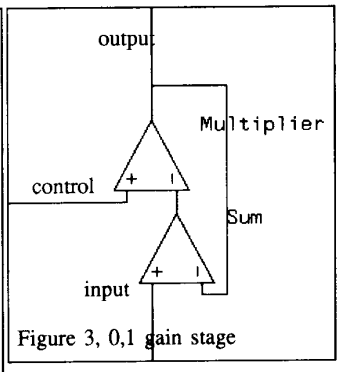

Figure 3, 0,1 gain stage

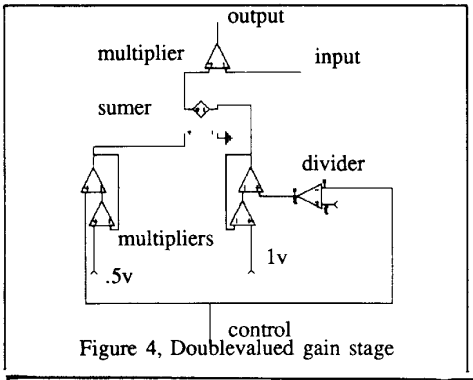

Figure 4, Doublevalued gain stage

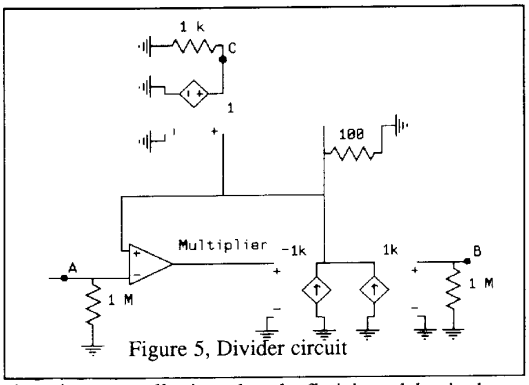

Figure 5, Divider circuit

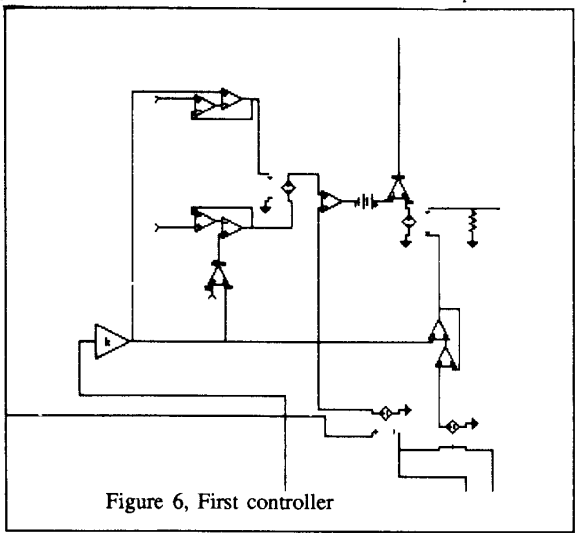

Figure 6, First controller

controller.

In the second version of the controller model, a mode-invariant form of the duty ratio equation eliminated the double-valued gain stages. Although this controller reduced fatal convergence errors, it did not accelerate execution. The mode-invariant controller introduced a ficticious delay in the state variable waveforms. A smaller RELTOL removed the delay but slowed execution to the previous rate. Figure 7 shows the mode-invariant model. By replacing Vi with its almost average value (sensed between the transformers),

$$d = f^* (Vc-Vi) / (m+m_1/2)$$

reqardless of mode. The need to change formulas amid simulation dissappeared and the controller model lossed its troublesome dependence on node C. The encircled elements keep the controller from processing a non-negative di/dt.

Although the subcircuits worked well by themselves, together they created convergence nightmares. Fortunately, circuit remedies removed most aggravations. The finite input impedances of the workbench's function blocks hindered convergence by creating bidirectional signal paths. Buffers constructed from ideal voltage-controlled-voltage sources ensured unidirectional coupling. Node C played a crucial role in convergence of the first controller because several feedback loops depended on it. Without the parasitic RC network in Figure 7, SPICE had difficulty determining the conduction mode and sometimes failed to converge. Negative voltages on node C created positive feedback in the double-valued gain stages and negative resistance across the inductor. Both effects caused divergence. Since the circuit

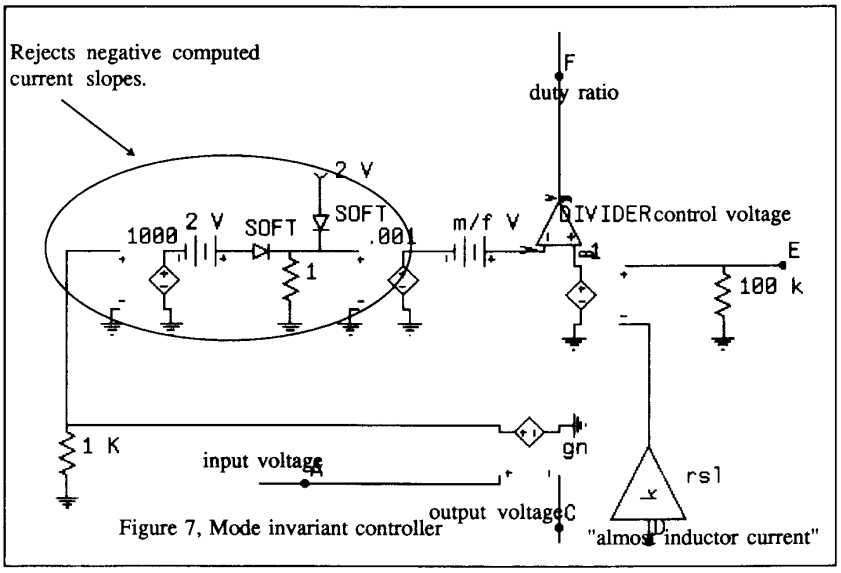

Figure 7, Mode invariant controller

depends only on the order of magnitude of node C's voltage, the multiplier in Figure 7 solved the problem by squaring the voltage. Analog Design Tools Inc. suggested using "softer" diodes and zero volt batteries to eliminate convergence errors. Sharp transfer curves and instantaneous reactions of ideal (i.e. "hard") diodes frequently inhibit convergence. A saturation current of 1e-8 A, an emission coefficient of .4, an ohmic resistance of .0001 ohm, a parallel 100k resistor, and a junction capacitance of 100pf softened the diode and improved convergence. Although zero volt batteries in series with ground connections do not electrically alter the circuit, they "magically" improve convergence. Some non-default analysis options proved unavoidable. The following non-default settings reduced convergence errors :

RELTOL=	.01
ABSTOL=	.0001
CHGTOL=	1E-8
ITL1=	500

COMPARISON WITH BRUTE-FORCE SIMULATION

A brute-force SPICE simulation validated the model. The brute-force model, shown in Figure 8, included a transistor and diode to toggle the inductor. Figure 9 compares brute-force and composite Bello state variable responses to a step in load current. The brute-force model executed in 15 minutes, the composite Bello executed in 9.

We extended the model to a four winding forward converter to check a frequency domain response against lab measurements. Since SPICE freezes the switch during the inevitable DC analysis, one can not use brute-force models in the frequency domain. SPICE has no difficulty linearizing the Bello model because state space averaged models have no switch. Figure 10 shows the extended composite Bello model. Figure 11 expands the main controller block. Figure 12 shows predicted phase and magnitude plots of the voltage loop gain while Figure 13 shows the corresponding lab measurements.

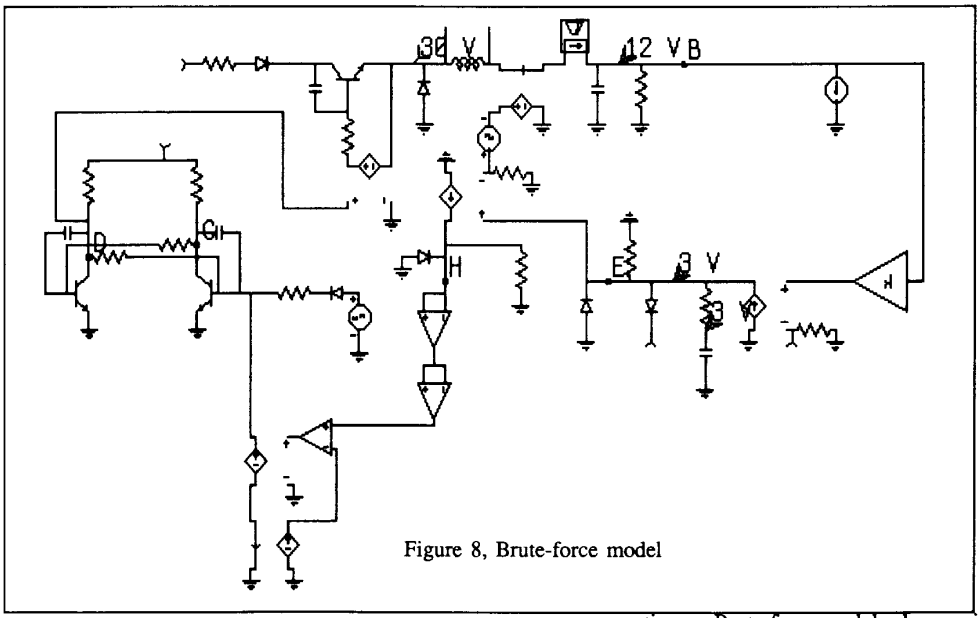

Figure 8, Brute-force model

CONCLUSIONS

With the right models, the workbench increases power system reliability by putting design engineers in direct and efficient contact with SPICE. Until now, the right duo-mode SPICE model of current-programmed converters did not exist; fast models operated in only one mode and duo-mode models taxed the engineers patience. Brute-force models also require modification for frequency domain analysis because SPICE freezes the switch to

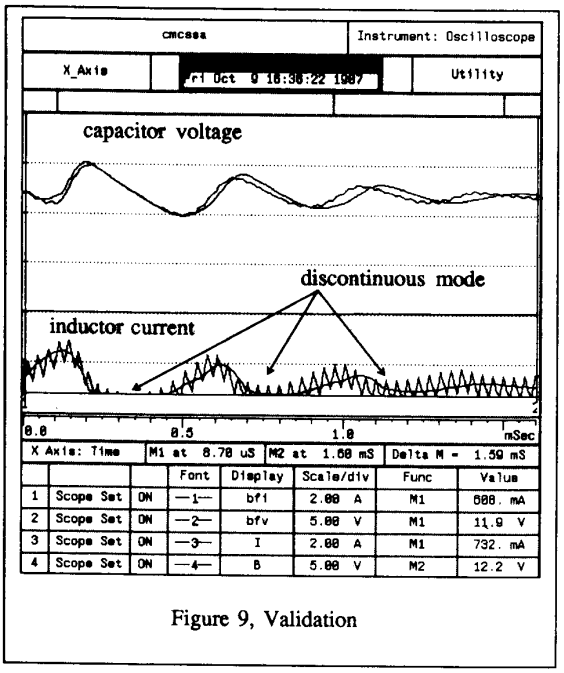

Figure 9, Validation

compute operating points and consequently removes all feedback. The duo-mode current-programmed converter model presented in this paper accelerates time domain SPICE simulations and requires no modification for frequency domain analysis. The interrelated feedback loops created several convergence problems but none proved insurmountable, and the results matched those of a brute-force simulation.

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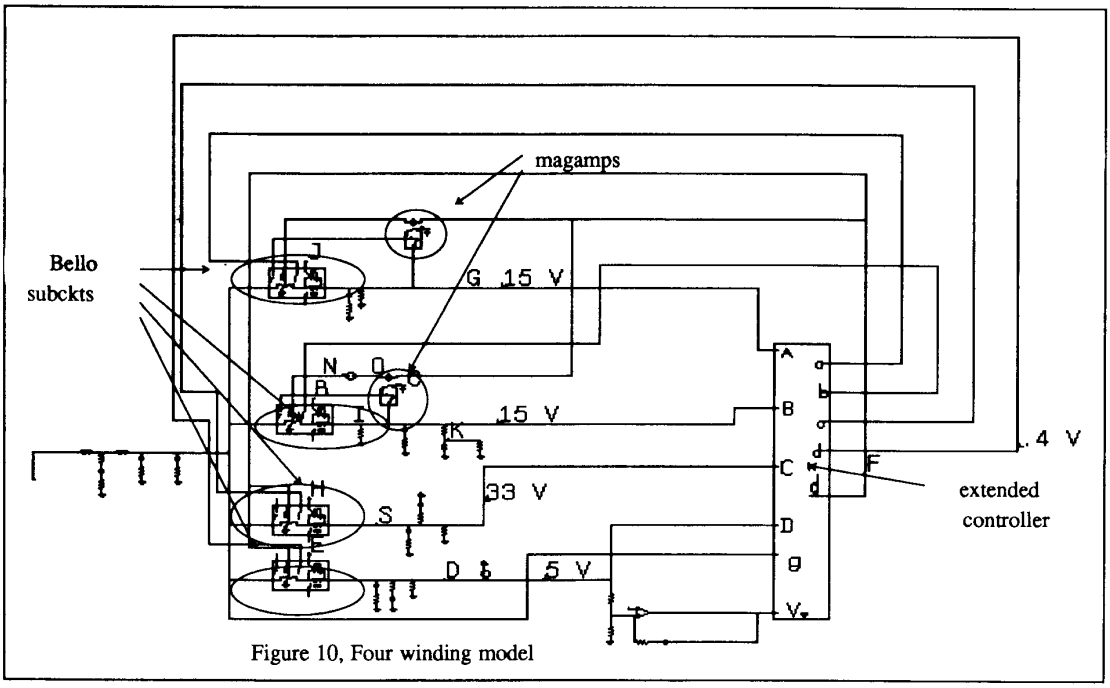

Figure 10, Four winding model

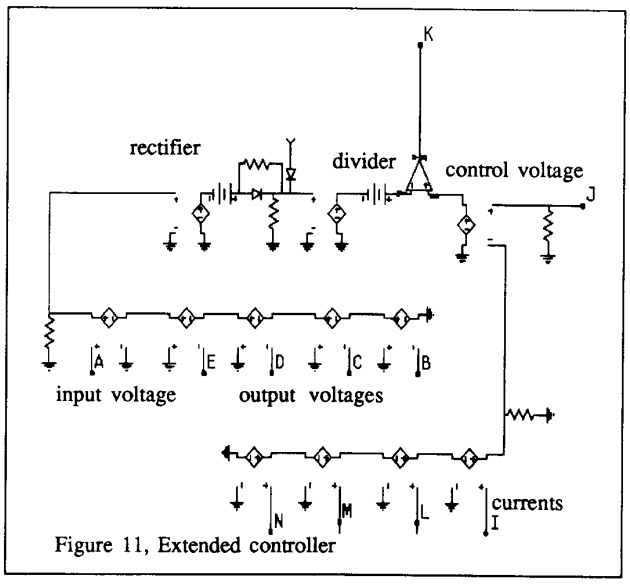

Figure 11, Extended controller

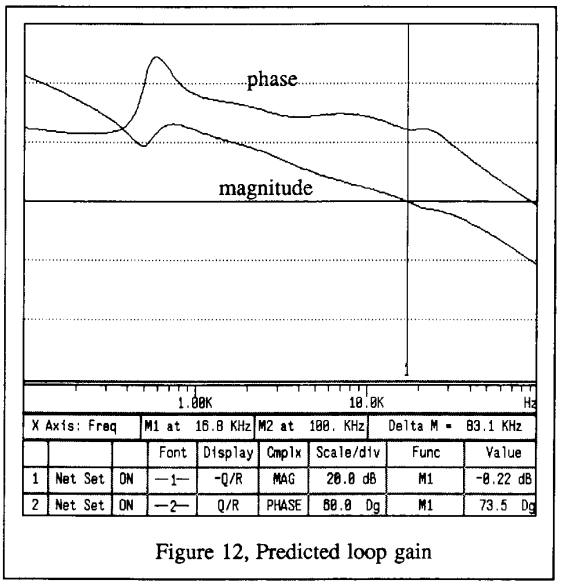

Figure 12, Predicted loop gain