the DC operating point by annulling the capacitances. This creates an open circuit at the gate. As no current is flowing through the resistance R_G, the FG DC operating point is given by the sum of the VCVS voltages. In AC analysis, the VCVSs do not have any influence on the simulation because the resistance connected to the gate is very large and thus behaves as an open circuit even for very low frequencies.

Although very commonly used, this approach has several important limitations. On one hand, the parasitic capacitances have to be known from the beginning. The only way to obtain their values is to, prior to application of the proposed method, carry out a set of simulations with an estimated operating point at the FG. This is not completely correct since the voltage at the FG does depend on these parasitic capacitances. Besides, once their values are obtained this method assumes that they are constant for the whole operating range, which is not always true. In fact the deviations from these values can be quite significant if the transistor has to operate in more than one region. Also, the final values of the parasitics connected to the FG increase once the circuit has been laid out and this can be difficult to model in the schematics [125]. All these facts increase the risk of failure in certain topologies, and is critical in those analog cells that have to work with reduced voltage margins, such as, for example, the low voltage circuits described along this book. Circuits operating in the subthreshold region are also very much affected by the variation of the parasitic capacitances since this variation will have an exponential effect.

A very important consequence of an incorrect estimation of C_{GD} is the miscalculation of the output resistance (see eq. (2.11)), which can cause a number of undesired effects such as unexpected losses in a bandpass filter, large variations in a quality factor and cutoff frequency, instability and so on.

All these problems could be minimised by oversizing the transistors in such a way that the parasitic capacitance which varies the most is much smaller than the minimum input capacitance (how much smaller would depend on the value of the expected variation and how it could affect the circuit performance). However, it is not easy to know a priori how much bigger the input capacitors need to be. Previous assumptions need to be made that are often not trivial and could even give rise to undesired consequences such as instability in circuits with feedback. Besides, oversizing the input capacitors might be unnecessary and therefore a waste in terms of area.

Yin *et al.* suggest a different model to simulate FGMOS transistors [122]. The model is based on connecting resistors in parallel with the input capacitors as shown in Fig. 2.6. The equation for the operating point is the same one as in Ramírez-Angulo's approach. The problems of this model are also the same.

Another technique proposed in literature [123] is based on iterative simulations which are directly performed by the simulator with the help of a program that has to be previously implemented. This can be done using the SKILL language functions in Cadence [123,125]. This technique is a more accurate, but still not exact enough, version of the method in [121].

A reliable technique to simulate FGMOS transistors is illustrated in Fig. 2.7 [124]. It is based on the use of an initial transient analysis (ITA). At the beginning of this analysis supply voltages and circuit inputs are set to 0 V. Under these conditions,

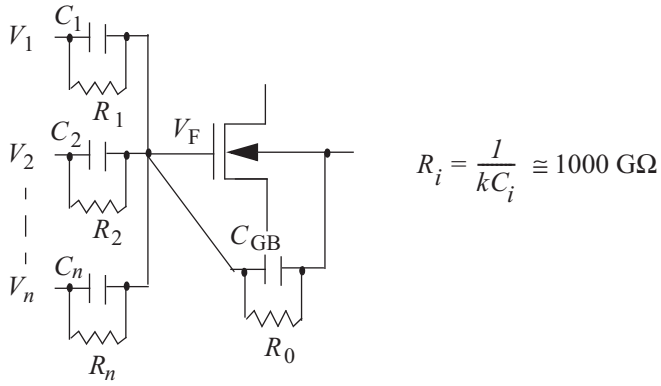

Figure 2.6 Model in [122] for the FGMOS

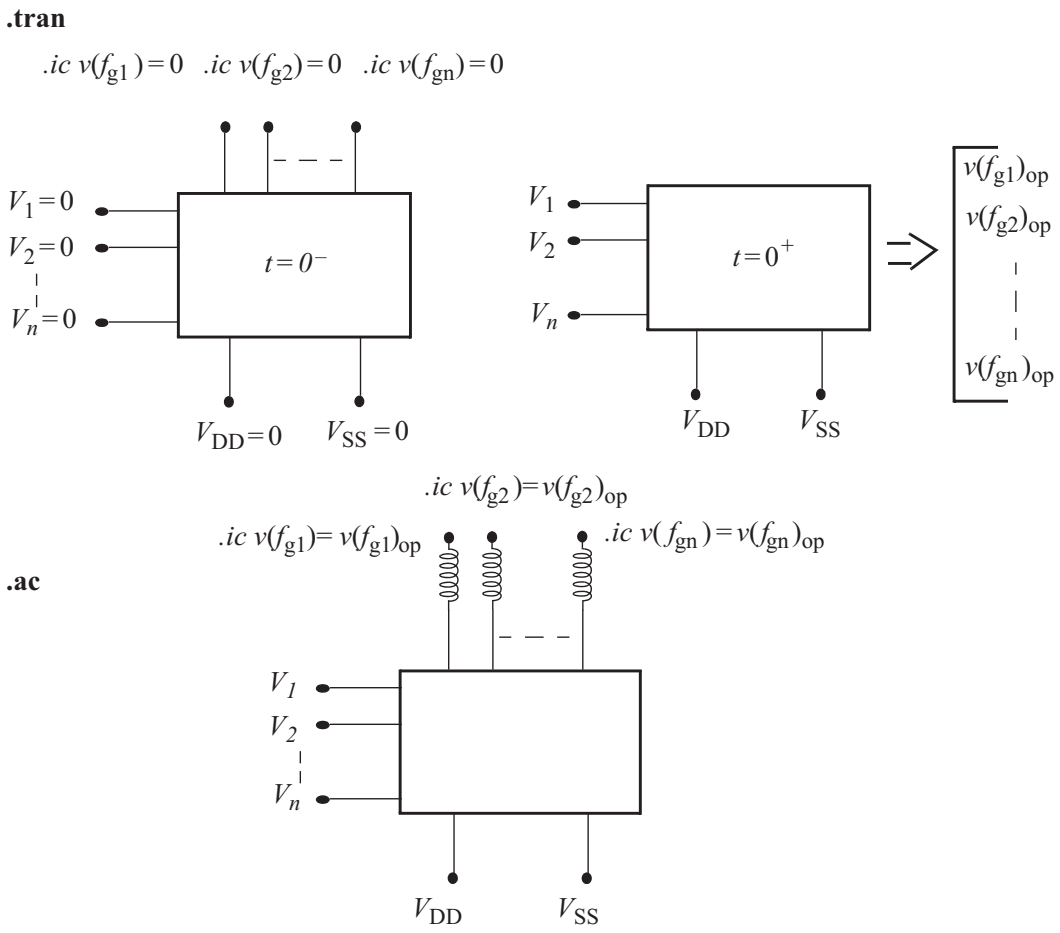

Figure 2.7 Simulation technique based on an initial transient analysis (ITA)

it can be guaranteed that the initial voltages at the FGs are also zero, unless that, as it happens in some technological processes or under certain conditions, some residual charge (Q_{FG}) remains trapped at the FG after fabrication. If this is the case, the initial condition at the FGs would be Q_{FG}/C_T. In any case, this is an unpredictable term common to all models and will be discussed in more detail in the next section. The transient analysis starts with these initial conditions. If, for example, HSpice is

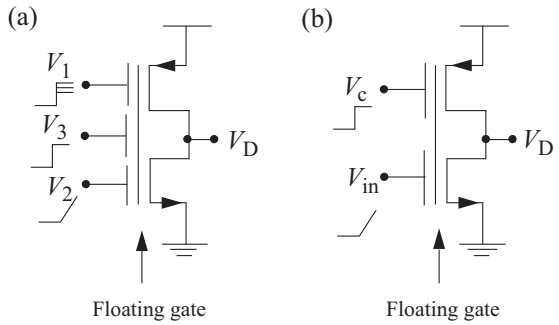

Figure 2.8 *(a) Circuit used to illustrate the simulation technique in Fig. 2.7 (b) Circuit used to compare the techniques in Figs. 2.5 and 2.7*

used, the initial conditions can be imposed with the command .ic [120]. Subsequently, the supply voltages are set to their final values and the inputs evolve normally. Small signal simulations can be performed extracting the operating point $(v(f_{gi})_{op}$ for $i = [1, n])$ from the transient analysis and forcing it to the FGs with the help of very high value inductances. The inductances behave as wires in DC and fix the operating point. Besides, if they are big enough, their effect is negligible for any other operating frequency. In the case of Hspice, for example, after completing a transient simulation, the operating point can be found in the file input_file_name.ic (where input_file_name is the name of the input file). In order to force the initial conditions the command .nodeset at the beginning of the file needs to be changed to .ic.

An example of how to use this simulation technique is provided below. The netlist describes the FGMOS inverter shown in Fig.2.8(a). First of all, the subcircuits for generic n-channel and p-channel transistors are defined. The external nodes for these subcircuits are the FGs, drains, effective inputs and sources. The parameters are the values of the input capacitances and the dimensions of transistors. The reason for adding the FG to the list of external nodes, despite the fact that it has to be completely isolated, is that it gives the freedom to change the number of capacitive inputs without having to define a new device. The simulation shows how to perform a parametric DC analysis. As it was previously explained, voltage supplies and inputs are initially set to 0 V and a zero initial condition is forced at the FG with the option .ic. When the circuit is 'powered up' [vdd vdd 0 pulse(0 2 0.01 0.01 1 2 4)] , the inputs that are going to be constant in the steady state change quickly [v1 v1 0 pulse(0 a 0.01 0.01 1 2 4), v3 v3 0 pulse(0 2 0.01 0.01 1 2 4)], whereas the input which is supposed to be swept in DC rises very slowly [v2 v2 0 pulse (0 2 0.01 1 1 2 4)]. In subsequent simulations the final value of the DC bias ('*a*' parameter in v1) is set to different values thus performing the parametric variations. The input–output characteristics obtained with these simulations are shown in Fig. 2.9.

Netlist for the circuit in Fig. 2.8(a)

```
Inverter

.include 'c:\simulation\modelos\NC\Typical\NC.sp'
```

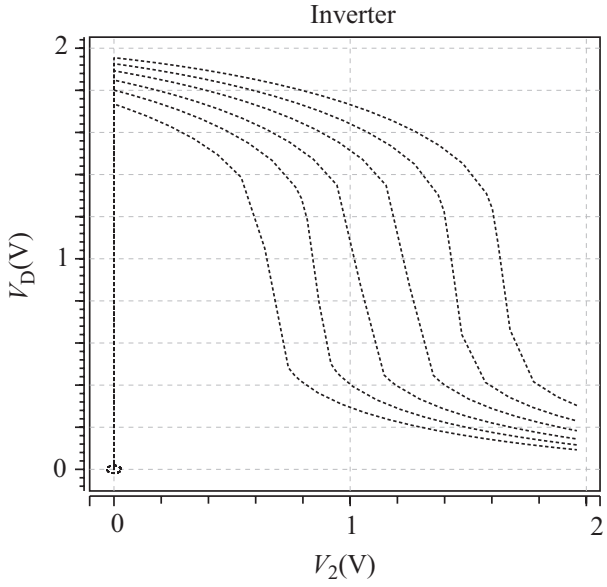

Figure 2.9 Input–output characteristic for the FGMOS inverter in Fig. 2.8(a)

```
.include 'c:\simulation\modelos\PC\Typical\PC.sp'


.subckt transistorn vg vd v1 v2 v3 vs w=20u l=20u
   c1=210f c2=210f c3=210f


m1 vd vg vs 0 nc w='w' l='l'

c1 v1 vg c1

c2 v2 vg c2

c3 v3 vg c3

.ic vg=0


.ends


.subckt transistorp vg vd v1 v2 v3 vs w=20u l=20u
   c1=210f c2=210f c3=210f


m1 vd vg vs 0 pc w='w' l='l'
```

```
c1 v1 vg c1

c2 v2 vg c2

c3 v3 vg c3

.ic vg=0


.ends

x1 vg vd v1 v2 v3 0 transistorn w=20u l=20u c1=210f
   c2=210f c3=210f

x2 vg vd v1 v2 v3 vdd transistorp w=20u l=20u c1=210f
   c2=210f c3=210f


v1 v1 0 pulse(0 a 0.01 0.01 1 2 4)

v2 v2 0 pulse(0 2 0.02 1 1 2 4)

v3 v3 0 pulse(0 2 0.01 0.01 1 2 4)

vdd vdd 0 0 pulse(0 2 0.01 0.01 1 2 4)


.tran 0.01 1 sweep a 0 10 2

.op t=1

.options post


.end
```

The ITA technique is even easier to apply if the Spectre simulator is used in Cadence to design the circuit [125]. In this case the input file does not need to be modified to perform an AC simulation. The latter can be realised just by choosing the simulation options adequately in a transient simulation, followed by an AC analysis. In the initial transient analysis all the sources will be automatically set to zero by the simulator. They will then rise to their final value between the 'starttime' and the time zero. At the final time the operating point will be saved in a file. The AC analysis will then be run using this initial operating point from the file.