The objective is to implement an analog buffer in order to drive an input reference voltage, see Figure 1. Table 1 specifies characteristics parameters.

The topology selected for the OTA implementation is a 'Simple OTA' with Nmos transistors at the input.

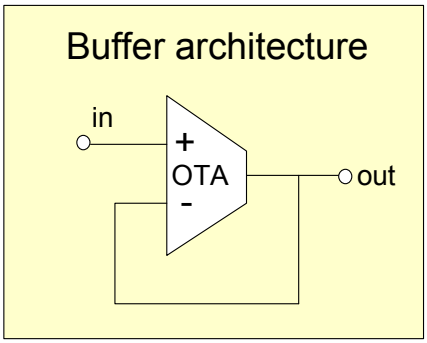

Figure 1. Buffer architecture

Table 1 - OTA parameters

FOM	Target
Open loop gain (dB)	A
Phase margin (º)	ph
Settling time 5mV (ns)	ts
Output noise (uVrms)	von_{rms}
Power cons. (mW)	P
Load capacitor (pF)	Cl

In following sections, several characteristic parameters of analog buffer and OTA must be calculated by the designer.

1.1.1. Schematic

Draw in Figure 2 the schematic of simple OTA (Differential Pair with MOS Loads, single-ended).

Figure 2. OTA architecture

1.1.2. Input and output range of buffer

Determine the input and output range of buffer in function of transistor parameters.

1.1.3. Offset

Explain the offset contributions.

1.1.4. Poles calculation

Calculate theoretically the poles of OTA in open loop.

Study the stability of buffer.

Calculate the poles of buffer (OTA in closed loop).

Maybe several assumptions and approximations should be account in order to simplify the final results as much as possible.

1.1.5. Settling time

Obtain the mathematical expression associated to the settling time of buffer.

1.1.6. Verification

Describe in detail the verification plan associated to the analog buffer.