VDD

node

VSS

VDD

vssstk

vpstk vsstk 0 0.0

+
- vpstk

signal goes from
0.0V to VDD

.measure tran avgleakagestk AVG i(vpstk) FROM='ckper+(cktr/2)' TO='ckper+(cktr/2)+(ckper/2)'

when i(vpstk) is plotted the plot shows negative current. But I expect it to be positive
(because current is flowing in to the source). Why do I see different from what I expected?

Initially "node"is high there is a leakage current flowing in to the source and PMOS is
turned off also the the "node" voltage decreases and still the current is flowing in to the
source.