

A GENERAL DESCRIPTION OF COMMON-MODE FEEDBACK IN FULLY-DIFFERENTIAL AMPLIFIERS.

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Abstract

One of the standard techniques to extend the signal swing of analog IC's is to use fully-differential circuits. However, the common-mode feedback (CMFB) loops that are used to stabilize the DC output level also affect the differential-mode signal processing. In this paper, a general description is given of fully-differential amplifiers with their CMFB loops, and the impact of CMFB loop mismatching on CMRR, noise and distortion is discussed.

1. Introduction

Many analog IC's must operate with low total supply voltages, as dictated by system requirements or limitations in the IC process. This implies that the total signal swing can be very limited, and that achieving high signal-to-noise ratios becomes a difficult design problem. Fully-differential signal processing can result in a significant improvement in performance, for the following reasons:

- 1°: In a perfect fully-differential or balanced circuit implementation, all even harmonics are effectively cancelled. Even when there is a slight mismatch between the left and right side of the circuit, the partial cancellation of the even harmonics can be sufficient to reduce THD with an order of magnitude.
- 2°: Fully-differential signal processing is to first order insensitive to error, noise and interference sources which appear as Common-Mode (CM) error sources. This is particularly important for analog circuits on a predominantly digital IC, where high-frequency switching transients are superimposed on the supply and substrate bias voltages.

One of the basic problems of fully-differential operation is that the feedback around the amplifiers does only provide a Differential-Mode (DM) feedback, and therefore a stabilization of the quiescent DM signal levels. The same feedback does however not provide any stabilization of the CM voltage levels. As a result, an extra CMFB loop must be added to each operational amplifier, to maintain the output CM voltage at a preset DC level, which is most often the analog reference or ground voltage.

In most textbooks [1] or papers on analog IC design, DM feedback loops are treated with much more depth than CMFB loops. In particular, the following issues are seldomly covered in a general way:

- 1°: What is the CMFB loop gain and bandwidth?
- 2°: What is the impact of the CMFB loop on the DM signal processing?
- 3°: How does the CM output level depend on DM signals?

In this paper, we will present a general description of fully-differential amplifiers with a CMFB loop included. A set of gain parameters is defined which are suitable for predicting the actual performance of such a balanced amplifier. The presented formalism takes mismatching and non-linearity in the CMFB loop into account. The gain parameters which are defined here can easily be calculated or simulated for different circuit configurations. Hence, the authors expect that the presented formalism should be useful to compare different CMFB strategies, and to answer the questions stated above in a general way.

2. Description of Fully-Differential Amplifiers

It is common practice in CMFB circuits to sense the CM output voltage $V_{o,CM}$ by a circuit which is ideally insensitive to the DM output voltage $V_{o,DM}$. The output of such CM sense circuit can be either a voltage (Fig.1a) or a current (Fig.1b). For simplicity, we will in this paper always refer to the output of the CM sense circuit as a voltage, although the analysis is equivalent for current output CM sense circuits. In Fig.1a and 1b, the input voltages are represented by the CM input voltage $V_{i,CM}$ and the DM input voltage $V_{i,DM}$. The output CM and DM voltage components are $V_{o,CM}$ and $V_{o,DM}$. Realize that these four voltages do not exist as voltages on physical circuit nodes, but rather as linear combinations of the real input and output node voltages. The sensed voltage V_S however is a physical node voltage in the circuit. Unbalance in the CM sensing circuit will result in a (slight) dependency of V_S on $V_{o,DM}$. Therefore, the "CM Sense" block in Fig.1a and 1b has two inputs, $V_{o,CM}$ and $V_{o,DM}$. The sense signal V_S is applied as a secondary input to the main amplifier. This secondary input has a high gain between V_S to $V_{o,CM}$; unbalance in the main amplifier circuit will also create a non-zero gain between V_S and $V_{o,DM}$.

a) The linearized case

The classical textbook description of the different gain paths in a fully-differential circuit, which typically neglects the CMFB loop completely, is as follows:

$$\begin{bmatrix} V_{o,DM} \\ V_{o,CM} \end{bmatrix} = \begin{bmatrix} A_{DD} & A_{CD} \\ A_{DC} & A_{CC} \end{bmatrix} \begin{bmatrix} V_{i,DM} \\ V_{i,CM} \end{bmatrix}$$

where all four gains A_{DD} , A_{DC} , A_{CD} and A_{CC} can be functions of frequency. The ratio of A_{DD} over A_{DC} is known as the open-loop Common-Mode Rejection Ratio (CMRR) of the amplifier. The gains A_{DC} and A_{CC} typically do not play an important role in predicting the performance of the fully-differential circuit in which this amplifier is applied, as long as the CMRR of all blocks is high. However, if the CMFB loop is taken into account, we get a much more complicated representation of the circuit:

$$\begin{bmatrix} V_{o,DM} \\ V_{o,CM} \end{bmatrix} = \begin{bmatrix} A_{DD} & A_{CD} & A_{SD} \\ A_{DC} & A_{CC} & A_{SC} \end{bmatrix} \begin{bmatrix} V_{i,DM} \\ V_{i,CM} \\ V_S \end{bmatrix}$$

$$[V_S] = [A_{DS} \quad A_{CS}] \cdot \begin{bmatrix} V_{o,DM} \\ V_{o,CM} \end{bmatrix}$$

which, after elimination of the sense node voltage V_S , which is after all just an internal node of the circuit, can be rewritten as:

$$\begin{bmatrix} V_{o,DM} \\ V_{o,CM} \end{bmatrix} = \begin{bmatrix} A_{DD}^* & A_{CD}^* \\ A_{DC}^* & A_{CC}^* \end{bmatrix} \begin{bmatrix} V_{i,DM} \\ V_{i,CM} \end{bmatrix}$$

where the new DM and CM gains are given by:

$$A_{DD}^* = \frac{A_{DD}(1 - A_{SC}A_{CS}) + A_{DC}A_{CS}A_{SD}}{1 - A_{SC}A_{CS} - A_{SD}A_{DS}}$$

$$A_{CD}^* = \frac{A_{CD}(1-A_{SC}A_{CS}) + A_{CC}A_{CS}A_{SD}}{1-A_{SC}A_{CS}-A_{SD}A_{DS}}$$

$$A_{DC}^* = \frac{A_{DC}(1-A_{SD}A_{DS}) + A_{DD}A_{DS}A_{SC}}{1-A_{SC}A_{CS}-A_{SD}A_{DS}}$$

$$A_{CC}^* = \frac{A_{CC}(1-A_{SD}A_{DS}) + A_{CD}A_{DS}A_{SC}}{1-A_{SC}A_{CS}-A_{SD}A_{DS}}$$

It is important to realize that the gains A_{SD} and A_{DS} are only due to mismatches; therefore:

$$A_{SC}A_{CS} \gg A_{SD}A_{DS}$$

It is also important to realize that what is commonly called the loop gain T_{CM} of the CMFB loop is effectively:

$$T_{CM} = A_{SC}A_{CS}$$

T_{CM} should be made as high as possible at DC, and its bandwidth should be as high as the differential-mode bandwidth, which depends on A_{DD} and the external DM feedback network. The major design problem here is that the gain A_{SC} is the gain through the secondary input stage which has in many cases considerably lower transconductance than the primary input stage which realizes A_{DD} . Hence, it is rather difficult to reach the same bandwidth for CM and DM feedback loops.

Another very important parameter to describe the interaction between CM and DM signals, is the loop gain ΔT_{CM} , which is defined here as:

$$\Delta T_{CM} = A_{SD}A_{CS}$$

For a perfectly balanced amplifier circuit, A_{SD} and therefore also ΔT_{CM} are both equal to zero. The physical interpretation of ΔT_{CM} is the following. T_{CM} is the CMFB loop gain. For a perfectly balanced amplifier circuit, the gain from node V_S to each of the amplifier output nodes V_{O+} and V_{O-} is equal; this gain has been called A_{SC} before. If the amplifier circuit is unbalanced or mismatched, then the gain between V_S to V_{O+} and between V_S and V_{O-} is not equal, and the difference between these gains is the gain A_{SD} . Therefore, ΔT_{CM} represents the unbalance between the CMFB loop gain through V_{O+} and through V_{O-} , as is indicated in Fig.1c.

We can now simplify the four effective gains of the amplifier to the following equivalent forms:

$$A_{DD}^* = \frac{A_{DD}(1-T_{CM}) + A_{DC}\Delta T_{CM}}{1-T_{CM}} \approx A_{DD}$$

$$A_{CD}^* = \frac{A_{CD}(1-T_{CM}) + A_{CC}\Delta T_{CM}}{1-T_{CM}}$$

$$A_{DC}^* = \frac{A_{DC}(1-A_{SD}A_{DS}) + A_{DD}A_{DS}A_{SC}}{1-T_{CM}}$$

$$A_{CC}^* = \frac{A_{CC}(1-A_{SD}A_{DS}) + A_{CD}A_{DS}A_{SC}}{1-T_{CM}}$$

It is important to realize that the open-loop DM gain A_{DD}^* is almost equal to A_{DD} , i.e. it is not significantly affected by the non-idealities of the CMFB loop. As will be shown later, this conclusion is only true as long as the complete amplifier system is linear.

The CMRR of the amplifier, after the inclusion of the CMFB loop, now becomes equal to:

$$CMRR^* = \frac{A_{DD}(1-T_{CM}) + A_{DC}\Delta T_{CM}}{A_{CD}(1-T_{CM}) + A_{CC}\Delta T_{CM}}$$

or:

$$CMRR^* = CMRR \cdot \frac{A_{DD}(1-T_{CM}) + A_{DC}\Delta T_{CM}}{A_{DD}(1-T_{CM}) + CMRR \cdot A_{CC}\Delta T_{CM}}$$

Two important conclusions can be made here. First of all, all four gains of the original amplifier (A_{DD} , A_{CD} , A_{DC} and A_{CC}), together with the CMFB loop gains T_{CM} and ΔT_{CM} , all can have a major impact on the effective CMRR of the amplifier. It is also clear that the CMRR will be degraded if the common-to-common gain A_{CC} is large, if the CMRR before inclusion of the CMFB loop

was high, and if the CMFB loop gain T_{CM} is low, but has an appreciable unbalance. In the limiting case, the CMRR* can be reduced to:

$$CMRR^* = \frac{A_{DD}(1-T_{CM})}{A_{CC}\Delta T_{CM}}$$

As a result, CMRR* may reduce to only 50 to 60 dB.

b) The impact of noise in the CMFB loop

Using the same matrix equations as before, we can analyze the noise performance of the amplifier. For simplicity, we assume here that the noise performance of the main amplifier can be represented by an input-referred (differential-mode) noise voltage e_{NA} . We will model the noise performance of the CMFB sense circuit by an output referred noise source with value e_{NS} . This means that this noise source e_{NS} is also the input referred noise of the secondary input of the main amplifier, where the CM sense signal V_S is fed back into the main amplifier. The effective input referred noise voltage of the total amplifier can now be approximated by:

$$e_{NA}^* = e_{NA} + \frac{\Delta T_{CM}}{1-T_{CM}} \cdot \frac{e_{NS}}{A_{DD}}$$

which implies that the noise level in the DM signal path will not be affected significantly by noise generated in the CMFB loop circuitry.

c) The non-linear case

Obviously, any practical amplifier circuit will be non-linear, due to the non-linearity of the I-V characteristic of the MOS transistors. However, in a fully-differential amplifier, it is not only sufficient to linearize the gain A_{DD} [2]. Let us assume that the sense voltage V_S contains a component F_{DM} which is a non-linear function of the DM voltage $V_{O,DM}$:

$$V_S = A_{CS}(V_{O,CM} + F_{DM})$$

In Fig.2 to 4, three previously published CM sense circuits are shown. In Fig.2, the common-source voltage of a differential pair V_S is used to estimate the CM voltage [3,4]. In Fig.3, a current mirror is degenerated by resistors (MOSFET's in the linear range) that are sensitive to the CM voltage; the output is a current [1,4]. Both circuits have very high F_{DM} values, as is indicated in Fig.5. A generic version of a family of improved current-output CM sensing circuits [5,6] is shown in Fig.4; this circuit has a very small F_{DM} value over the whole $V_{O,DM}$ range. For most CM sense circuits, F_{DM} can be approximated by:

$$F_{DM} = \alpha \cdot V_{O,DM}^2$$

Let us further, to simplify the calculations, assume that all other gains in this amplifier (as defined before) are linear, and that a purely linear DM feedback is applied around the amplifier, which yields a closed-loop gain A_{CL} . Then we can derive the following equations for the second and third order harmonic distortion of the output DM signal:

$$HD_2 = \sqrt{2} \cdot A_{CL} \cdot \frac{\alpha \cdot \Delta T_{CM}}{T_{CM}} \cdot V_{in,RMS}$$

$$HD_3 = 4 \cdot A_{CL}^2 \cdot \frac{\alpha^2 \cdot \Delta T_{CM}^2}{T_{CM}^2} \cdot V_{in,RMS}^2$$

In Fig.6, the HD_2 distortion component is shown for the three circuits in Fig.2 to 4, due to a non-zero α , assuming a linear DM amplifier gain. On top of this, we will also see an appreciable shift in the CM output voltage, due to the DM signal:

$$V_{O,CM} = \alpha \cdot A_{CL}^2 \cdot V_{i,DM}^2$$

In Fig.7, the two output voltages V_{O+} and V_{O-} are shown for the three CM sense circuits in Fig.2 to 4. It can be observed that the CM output level shift results in a very asymmetrical signal swing. It can even cause

premature saturation of one of the output nodes, if α is too large. It is clear from Fig. 5 to 7 that the circuit in Fig.4 [5,6] are clearly superior over the other circuits.

3. Conclusions

The main conclusion of this paper is that the CM sense circuits can have a major impact on the accuracy of the DM signal processing. Major parameters that affect such DM signal processing are:

- 1°: The parameters F_{DM} (or α) which characterizes the non-linear relationship between the CM sense output V_S and the DM output signal.
- 2°: The unbalance in the CM loop gain ΔT_{CM} .

To optimize the performance of the fully-differential circuit, one should choose a CM sense circuit with a minimal non-linear (quadratic) sensitivity to $V_{o,DM}$, even when this means that a small linear sensitivity to $V_{o,DM}$ must be tolerated. The circuit in Fig.4 results in far better linearity and signal swing specifications than the circuits in Fig. 2 and 3.

4. Reference List

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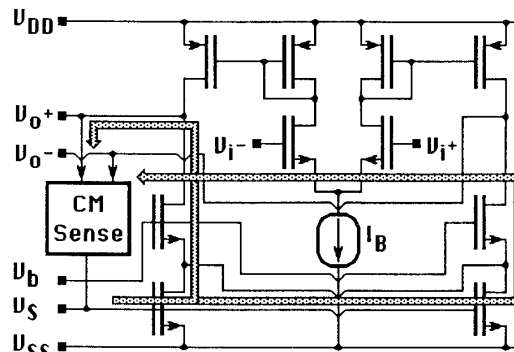
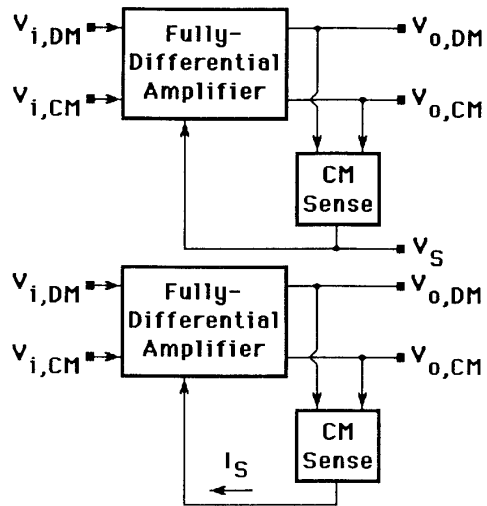


Fig.1: Simplified block diagrams of a fully-differential amplifier with Common-Mode feedback.
a) CM sense with voltage output V_S
b) CM sense with current output I_S
c) Definition of T_{CM} and ΔT_{CM} for simple OpAmp

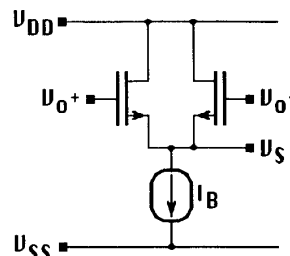


Fig.2: Commonly used CM sensing circuit with voltage output V_S (common source of diff. pair)

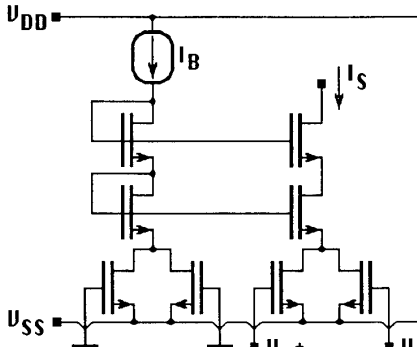


Fig.3: Commonly used CM sensing circuit with current output I_S (source degeneration of current mirror)

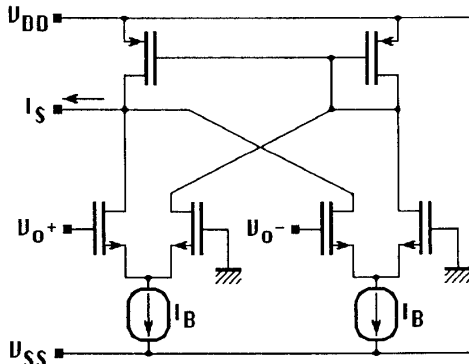


Fig.4: Improved version of CM sensing circuit with current output I_S with two differential pairs.

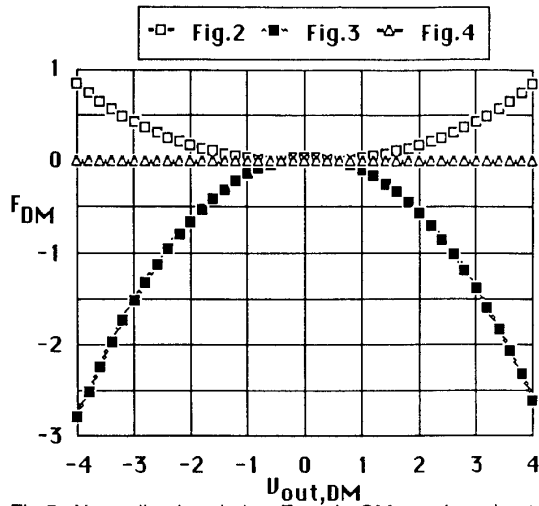


Fig.5: Normalized variation F_{DM} in CM sensing, due to DM output voltage, for the circuits in Fig.2 to 4.

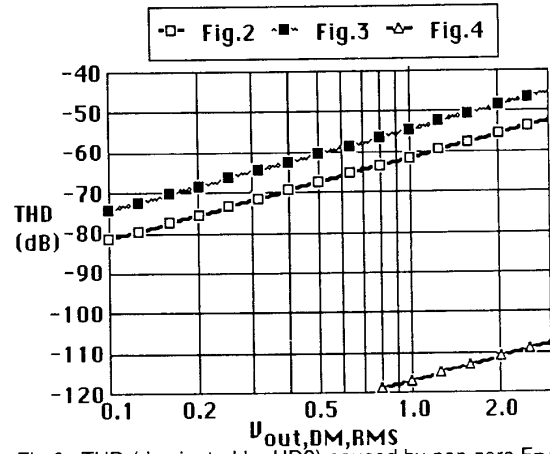


Fig.6: THD (dominated by HD2) caused by non-zero F_{DM} for the three circuits in Fig.2 to 4 (does not include possible distortion due to other non-linearities).

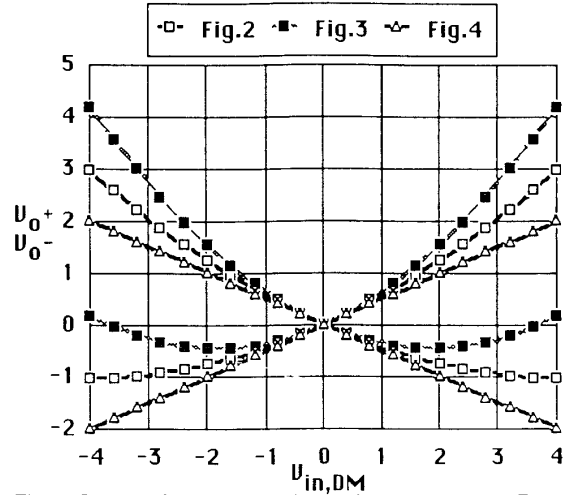


Fig.7: Shift in CM output voltage due to non-zero F_{DM} for the three circuits in Fig.2 to 4, for amplifier with unity-gain feedback. High values for F_{DM} lead to very asymmetrical signal swing.