```
////////////////////////////////////////////////////////////////////////
// PLEASE DO NOT EDIT OR COMPILE THIS FILE.
// IT IS MEANT FOR VIEWING PURPOSE ONLY.
//
// All files for configuration: (workDan sim_inh_conn_test config)
////////////////////////////////////////////////////////////////////////

`include "disciplines.vams"
`include "userDisciplines.vams"
// Library - amis500cxascm, Cell - inv1_m, View - schematic
// LAST TIME SAVED: Aug 14 11:18:00 2007
// NETLIST TIME: Jan 14 09:09:40 2009
`timescale 1ns / 1ns

(* cds_ams_schematic *)
module inv1_m1 ( Q, A );
output  Q;

input  A;
wire (*
integer inh_conn_prop_name = "LVDD";
integer inh_conn_def_value = "cds_globals.\\vdd! ";*)
cdsNet0;
wire (*
integer inh_conn_prop_name = "LVSS";
integer inh_conn_def_value = "cds_globals.\\vss! ";*)
cdsNet1;
wire (*
integer inh_conn_prop_name = "SUB";
integer inh_conn_def_value = "cds_globals.\\sub! ";*)
cdsNet2;


// List of primary aliased buses

wire (*
integer inh_conn_prop_name = "LVDD";
integer inh_conn_def_value = "cds_globals.\\vdd! ";
*)
\LVDD_vdd! ;
epm #(.w(2.4), .l(0.6), .as(2.165), .ad(2.165), .ps(7.2), .pd(7.2),
    .nrd(0.2957), .nrs(0.2957), .m(1), .mult("(1)"), .region(1),
    .matchingLevel("LOW"))
(* integer passed_mfactor = "m"; *)
PMOS_1 (Q, A, cdsNet0, \LVDD_vdd! );

wire (*
integer inh_conn_prop_name = "SUB";
integer inh_conn_def_value = "cds_globals.\\sub! ";
*)
\SUB_sub! ;
enm #(.w(2.6), .l(0.6), .as(2.295), .ad(2.295), .ps(7.6), .pd(7.6),
    .nrd(0.2981), .nrs(0.2974), .m(1), .mult("(1)"), .region(1),
    .matchingLevel("LOW"))
(* integer passed_mfactor = "m"; *)
NMOS_1 (Q, A, cdsNet1, \SUB_sub! );

endmodule
// Library - workDan, Cell - sim_inh_conn_test, View - schematic
// LAST TIME SAVED: Jan 14 09:09:37 2009
// NETLIST TIME: Jan 14 09:09:40 2009
`timescale 1ns / 1ns

(* cds_ams_schematic *)
module sim_inh_conn_test (  );


// List of primary aliased buses

capacitor #(.c(1p)) C0 (c, vss);

\inv1_m (* integer cds_net_set
[0:2] = { "LVDD","SUB","LVSS" };
integer LVDD = "vdd";
integer SUB = "vss";
integer LVSS = "vss";
*)  I6 ( .Q(b), .A(a));

inv1_m1 (* integer cds_net_set
[0:2] = { "SUB","LVSS","LVDD" };
integer SUB = "vss";
integer LVSS = "vss";
integer LVDD = "vdd";
*) I7 ( c, b);

inv1_m1 (* integer cds_net_set
[0:2] = { "SUB","LVSS","LVDD" };
integer SUB = "vss";
integer LVSS = "vss";
integer LVDD = "vdd";
*) I1 ( a, in);

vsource #(.dc(0), .type("pulse"), .val0(0), .val1(5), .period(2u),
    .delay(1u), .rise(500p), .fall(500p), .width(1u)) V1 (in, vss);

vsource #(.type("dc")) V2 (vss, cds_globals.\gnd! );

vsource #(.dc(5), .type("dc")) V0 (vdd, vss);
```

```
endmodule
// Verilog-AMS cds_globals module for top-level cell:
//    workDan/sim_inh_conn_test.
// Generated by ADE.
// Cadence Design Systems, Inc.

// This is an autoGenerated file, any changes done to this file may get lost.

`include "disciplines.vams"
`include "userDisciplines.vams"

module cds_globals;

// Global Signals
   electrical \sub! ;
   electrical \vdd! ;
   electrical \vss! ;
   electrical \gnd! ;
   ground \gnd! ;

// Design Variables

endmodule

// This is the Cadence AMS Designer(R) analog simulation control file.
// It specifies the options and analyses for the Spectre analog solver.

simulator lang=spectre

simulatorOptions options temp=27 tnom=27 scale=1.0 scalem=1.0 reltol=1e-3 \
vabstol=1e-6 iabstol=1e-12 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
digits=5 pivrel=1e-3

tran tran stop=20u save=none write="spectre.ic" writefinal="spectre.fc" \
errpreset=conservative maxiters=5 annotate=status

finalTimeOP info what=oppoint where=rawfile

modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile

saveUseProbes options currents=all useprobes=yes

# This is the NC-SIM(R) probe command file
# used in the AMS-ADE integration.


#
# Database settings
#
if { [info exists ::env(AMS_RESULTS_DIR) ] } { set AMS_RESULTS_DIR $env(AMS_RESULTS_DIR)} else {set AMS_RESULTS_DIR "/export/home/scratch/sims/sim_inh_co
nn_test/ams/config/psf"}
database -open ams_database -into $AMS_RESULTS_DIR -default

#
# Probe settings
#
probe -create -emptyok -database ams_database -all -depth all
probe -create -emptyok -database ams_database -all cds_globals
probe -create -emptyok -database ams_database {sim_inh_conn_test.c}
probe -create -emptyok -database ams_database {sim_inh_conn_test.b}
probe -create -emptyok -database ams_database {sim_inh_conn_test.a}
probe -create -emptyok -database ams_database {sim_inh_conn_test.in}
probe -create -emptyok -database ams_database -flow -ports -depth all
probe -create -emptyok -database ams_database -aicms -all -depth all
```

```
irun: 06.11-s011: (c) Copyright 1995-2008 Cadence Design Systems, Inc.
TOOL:   irun    06.11-s011: Started on Jan 14, 2009 at 09:09:40 MST
irun
        -clean
        -UNBUFFERED
        -noupdate
        -nowarn DLNOHV
        -v93
        -incdir .
        -propspath /projects/20348-900/RevA/local/lib/development/dfii/workDan/sim_inh_conn_test/config/prop.cfg
        -timescale 1ns/1ns
        -discipline logic
        -delay_mode None
        -novitalaccl
        -access r
        -amsmatlab
        -amspartinfo ../psf/partition.info
        -modelincdir /projects/20348-900/RevA/local/users/djclemen/
        -modelpath /projects/20348-900/RevA/local/lib/public/amis500cx/tech/spectre/amis500cxakxx/Rev2.16//dio-Default.scs(typ):/projects/20348-900/RevA/
local/lib/public/amis500cx/tech/spectre/amis500cxakxx/Rev2.16//res-Default.scs(typ):/projects/20348-900/RevA/local/lib/public/amis500cx/tech/spectre/amis
500cxakxx/Rev2.16//mos-Default.scs(typ):/projects/20348-900/RevA/local/lib/public/amis500cx/tech/spectre/amis500cxakxx/Rev2.16//cap-Default.scs(typ):/pro
jects/20348-900/RevA/local/lib/public/amis500cx/tech/spectre/amis500cxakxx/Rev2.16//bip-Default.scs(typ):/projects/20348-900/RevA/local/lib/public/amis50
0cx/tech/spectre/amis500cxakxx/Rev2.16//var-Default.scs(typ)
        -analogcontrol ./amsControlSpectre.scs
        -amslic
        -input ./probe.tcl
        -run
        -exit
        -ncsimargs "+amsrawdir ../psf"
        -simcompatible_ams spectre
        -name sim_inh_conn_test:config
        -amsconnrules ConnRules_inhconn_full
        -amsconnrules ConnRules_5V_full_fast1
        /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/ConnRules_inhconn_full/connect/verilog.va
ms
        /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/L2E_inhconn/module/verilog.vams
        /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/E2L_inhconn/module/verilog.vams
        /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/Bidir_inhconn/module/verilog.vams
        /export/home/scratch/sims/sim_inh_conn_test/ams/config/netlist/ihnl/connectLib/ConnRules_5V_full_fast1/connect/verilog.vams
        /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/L2E_2/module/verilog.vams
        /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/E2L_2/module/verilog.vams
        /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/Bidir_2/module/verilog.vams
        /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/E2R/module/verilog.vams
        /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/R2E/module/verilog.vams
        /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/ER_bidir/module/verilog.vams
        -v /projects/20348-900/RevA/local/lib/public/amis500cx/logic/verilog_generic/amis500cxascm/Rev3.6/amis500cxascm.v
        -v /projects/20348-900/RevA/local/lib/public/amis500cx/logic/verilog_generic/amis500cxapfx/Rev3.2/amis500cxapfx.v
        ./netlist.vams
        ./cds_globals.vams
        -l ../psf/irun.log
irun: *N,CLEAN: Removing existing directory ./INCA_libs.
file: /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/ConnRules_inhconn_full/connect/verilog.vams
        connect worklib.ConnRules_inhconn_full:vams
                errors: 0, warnings: 0
        connect worklib.ConnRules_inhconn_mid:vams
                errors: 0, warnings: 0
file: /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/L2E_inhconn/module/verilog.vams
        module worklib.L2E_inhconn:vams
                errors: 0, warnings: 0
file: /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/E2L_inhconn/module/verilog.vams
        module worklib.E2L_inhconn:vams
                errors: 0, warnings: 0
file: /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/Bidir_inhconn/module/verilog.vams
        module worklib.Bidir_inhconn:vams
                errors: 0, warnings: 0
file: /export/home/scratch/sims/sim_inh_conn_test/ams/config/netlist/ihnl/connectLib/ConnRules_5V_full_fast1/connect/verilog.vams
 'define Vthi  3.5
                |
ncvlog: *W,MACRDF (/export/home/scratch/sims/sim_inh_conn_test/ams/config/netlist/ihnl/connectLib/ConnRules_5V_full_fast1/connect/verilog.vams,11|18): te
xt macro 'Vthi' redefined - replaced with new definition.
 'define Vtlo  1.5
                |
ncvlog: *W,MACRDF (/export/home/scratch/sims/sim_inh_conn_test/ams/config/netlist/ihnl/connectLib/ConnRules_5V_full_fast1/connect/verilog.vams,12|18): te
xt macro 'Vtlo' redefined - replaced with new definition.
 'define Tr    1n
                |
ncvlog: *W,MACRDF (/export/home/scratch/sims/sim_inh_conn_test/ams/config/netlist/ihnl/connectLib/ConnRules_5V_full_fast1/connect/verilog.vams,13|17): te
xt macro 'Tr' redefined - replaced with new definition.
        connect worklib.ConnRules_5V_full_fast1:vams
                errors: 0, warnings: 0
file: /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/L2E_2/module/verilog.vams
        module worklib.L2E_2:vams
                errors: 0, warnings: 0
file: /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/E2L_2/module/verilog.vams
        module worklib.E2L_2:vams
                errors: 0, warnings: 0
file: /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/Bidir_2/module/verilog.vams
        module worklib.Bidir_2:vams
                errors: 0, warnings: 0
file: /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/E2R/module/verilog.vams
        module worklib.E2R:vams
                errors: 0, warnings: 0
file: /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/R2E/module/verilog.vams
        module worklib.R2E:vams
                errors: 0, warnings: 0
file: /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools.lnx86/affirma_ams/etc/connect_lib/connectLib/ER_bidir/module/verilog.vams
        module worklib.ER_bidir:vams
                errors: 0, warnings: 0
file: ./netlist.vams
```

```
        module worklib.inv1_m1:vams
                errors: 0, warnings: 0
        module worklib.sim_inh_conn_test:vams
                errors: 0, warnings: 0
file: ./cds_globals.vams
        module worklib.cds_globals:vams
                errors: 0, warnings: 0
file: /projects/20348-900/RevA/local/lib/public/amis500cx/logic/verilog_generic/amis500cxascm/Rev3.6/amis500cxascm.v
        module amis500cxascm.inv1_m:v
                errors: 0, warnings: 0
ncvlog: *W,LIBNOU: Library "/projects/20348-900/RevA/local/lib/public/amis500cx/logic/verilog_generic/amis500cxapfx/Rev3.2/amis500cxapfx.v" given but not
 used.
        Total errors/warnings found outside modules and primitives:
                errors: 0, warnings: 4
                Caching library 'amis500cxascm' ....... Done
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
ncelab: *N,SFEDPL: Deploying new SFE in analog engine.
        Top level design units:
                sim_inh_conn_test
                cds_globals
        Discipline resolution Pass...
        Doing auto-insertion of connection elements...
        Building instance overlay tables: ..................... Done
        Generating native compiled code:
                worklib.E2L_inhconn:vams <0x18fb3a7b>
                        streams:   8, words:  7354
                worklib.L2E_inhconn:vams <0x24407165>
                        streams:   9, words: 12483
                worklib.sim_inh_conn_test:vams <0x388ec292>
                        streams:   0, words:     0
        Loading native compiled code:     ..................... Done
        Building instance specific data structures.
        Design hierarchy summary:
                                 Instances  Unique
                Modules:                 8      13
                Primitives:              1       1
                Timing outputs:          1       1
                Registers:              20      45
                Scalar wires:            6       -
                Always blocks:          19      36
                Initial blocks:          3       8
                Cont. assignments:       3       9
                Interconnect:           10       -
                Simulation timescale:  10ps
        Writing initial simulation snapshot: worklib.sim_inh_conn_test:config
        Elaborating analog portion of the design hierarchy:
ncsim: *N,SFEDPL: Deploying new SFE in analog engine.
Loading snapshot worklib.sim_inh_conn_test:config ..................... Done
        Starting analog simulation engine...

Includes RSA BSAFE(R) Cryptographic or Security Protocol Software from RSA
        Security, Inc.

Analog Kernel using -ANALOGCONTROL  ./amsControlSpectre.scs.
ncsim> source /home/apps/cadence/ius/linux/ius6.1_usr4_isr20080223/tools/inca/files/ncsimrc
ncsim>
ncsim> # This is the NC-SIM(R) probe command file
ncsim> # used in the AMS-ADE integration.
ncsim>
ncsim>
ncsim> #
ncsim> # Database settings
ncsim> #
ncsim> if { [info exists ::env(AMS_RESULTS_DIR) ] } { set AMS_RESULTS_DIR $env(AMS_RESULTS_DIR)} else {set AMS_RESULTS_DIR "/export/home/scratch/sims/sim
_inh_conn_test/ams/config/psf"}
/export/home/scratch/sims/sim_inh_conn_test/ams/config/psf
ncsim> database -open ams_database -into $AMS_RESULTS_DIR -default
Created default SHM database ams_database
ncsim>
ncsim> #
ncsim> # Probe settings
ncsim> #
ncsim> probe -create -emptyok -database ams_database -all -depth all
Created probe 1
ncsim> probe -create -emptyok -database ams_database -all cds_globals
Created probe 2
ncsim> probe -create -emptyok -database ams_database {sim_inh_conn_test.c}
Created probe 3
ncsim> probe -create -emptyok -database ams_database {sim_inh_conn_test.b}
Created probe 4
ncsim> probe -create -emptyok -database ams_database {sim_inh_conn_test.a}
Created probe 5
ncsim> probe -create -emptyok -database ams_database {sim_inh_conn_test.in}
Created probe 6
ncsim> probe -create -emptyok -database ams_database -flow -ports -depth all
Created probe 7
ncsim> probe -create -emptyok -database ams_database -aicms -all -depth all
ncsim: *E,UNKOPT: unrecognized option for the probe [-create] command (-aicms).
ncsim> run

Warning from spectre during initial setup.
    sim_inh_conn_test.I7.NMOS_1.enm: 'A2' = 1.2 is larger than 1. Set A2 to 1
        and A1 to 0.
    sim_inh_conn_test.I7.NMOS_1.enm: 'Cdsc' = -400e-06 is negative.
    sim_inh_conn_test.I1.NMOS_1.enm: 'A2' = 1.2 is larger than 1. Set A2 to 1
        and A1 to 0.
    sim_inh_conn_test.I1.NMOS_1.enm: 'Cdsc' = -400e-06 is negative.
    sim_inh_conn_test.I7.PMOS_1.epm: 'A2' = 1.00801 is larger than 1. Set A2 to
```

```
        1 and A1 to 0.
    sim_inh_conn_test.I1.PMOS_1.epm: 'A2' = 1.00801 is larger than 1. Set A2 to
        1 and A1 to 0.
Notice from spectre during topology check.
    No connections to node 'cds_globals+sub!'.
    Only one connection to the following 3 nodes:
        0
        sim_inh_conn_test.I7.cdsNet0
        sim_inh_conn_test.I1.cdsNet0
    No DC path from node 'cds_globals+sub!' to ground, Gmin installed to
        provide path.
    No DC path from node 'sim_inh_conn_test.b__L2E_inhconn__logic.vdd!' to
        ground, Gmin installed to provide path.
    No DC path from node 'sim_inh_conn_test.b__L2E_inhconn__logic.vss!' to
        ground, Gmin installed to provide path.
    No DC path from node 'sim_inh_conn_test.b' to ground, Gmin installed to
        provide path.


Circuit inventory:
             nodes 11
         equations 54
            iprobe 16
     ahdl simulator 1
           bsim3v3 4
         capacitor 1
           vsource 3
worklib+E2L_inhconn+vams+0x10000001 behavioral 2
worklib+L2E_inhconn+vams+0x10000001 behavioral 1


Warning from spectre during initial setup.
    sim_inh_conn_test.I7.NMOS_1.enm: 'A2' = 1.2 is larger than 1. Set A2 to 1
        and A1 to 0.
        Further occurrences of this warning will be suppressed.
    sim_inh_conn_test.I7.NMOS_1.enm: 'Cdsc' = -400e-06 is negative.
    sim_inh_conn_test.I1.NMOS_1.enm: 'Cdsc' = -400e-06 is negative.
Warning from spectre during hierarchy flattening.
    3 warnings suppressed.


**********************************************
Transient Analysis 'tran': time = (0 s -> 20 us)
**********************************************

Notice from spectre during IC analysis, during transient analysis 'tran'.
    Gmin = 1 pS is large enough to noticeably affect the DC solution.
        dV(sim_inh_conn_test.I7.cdsNet0) = -38.1389 uV
        Use 'gmin_check' option to eliminate or expand this report.

Important parameter values:
    start = 0 s
    outputstart = 0 s
    stop = 20 us
    step = 20 ns
    maxstep = 200 ns
    ic = all
    skipdc = no
    reltol = 100e-06
    abstol(I) = 1 pA
    abstol(V) = 1 uV
    temp = 27 C
    tnom = 27 C
    tempeffects = all
    errpreset = conservative
    method = gear2only
    lteratio = 10
    relref = alllocal
    cmin = 0 F
    gmin = 1 pS
    maxrsd = 0 Ohm
    mos_method = s
    mos_vres = 50 mV

    tran: time = 500 ns       (2.5 %), step = 200 ns          (1 %)
    tran: time = 1.569 us    (7.85 %), step = 200 ns          (1 %)
    tran: time = 2.655 us    (13.3 %), step = 200 ns          (1 %)
    tran: time = 3.58 us     (17.9 %), step = 200 ns          (1 %)
    tran: time = 4.655 us    (23.3 %), step = 200 ns          (1 %)
    tran: time = 5.602 us      (28 %), step = 200 ns          (1 %)
    tran: time = 6.602 us      (33 %), step = 200 ns          (1 %)
    tran: time = 7.602 us      (38 %), step = 200 ns          (1 %)
    tran: time = 8.602 us      (43 %), step = 200 ns          (1 %)
    tran: time = 9.602 us      (48 %), step = 200 ns          (1 %)
    tran: time = 10.6 us       (53 %), step = 200 ns          (1 %)
    tran: time = 11.6 us       (58 %), step = 200 ns          (1 %)
    tran: time = 12.6 us       (63 %), step = 200 ns          (1 %)
    tran: time = 13.6 us       (68 %), step = 200 ns          (1 %)
    tran: time = 14.6 us       (73 %), step = 200 ns          (1 %)
    tran: time = 15.57 us    (77.9 %), step = 200 ns          (1 %)
    tran: time = 16.6 us       (83 %), step = 200 ns          (1 %)
    tran: time = 17.57 us    (87.9 %), step = 200 ns          (1 %)
    tran: time = 18.6 us       (93 %), step = 200 ns          (1 %)
    tran: time = 19.57 us    (97.9 %), step = 200 ns          (1 %)
Number of accepted tran steps = 1530.
Accumulated tran full load time = 180 ms.
    Accumulated tran full component evaluation time = 110 ms.
    Accumulated tran full preload time = 20 ms.
    Accumulated tran full merge time = 10 ms.
```

```
Accumulated tran residue-only load time = 70 ms.
    Accumulated tran residue-only component evaluation time = 50 ms.
    Accumulated tran residue-only preload time = 0 s.
    Accumulated tran residue-only merge time = 10 ms.
Accumulated tran factor time = 10 ms.
Accumulated tran solve time = 10 ms.
Accumulated tran output time = 200 ms.
Initial condition solution time = 0 s.

**** AMSD: Mixed-Signal Activity Statistics ****
Number of A-to-D events:                      61
  Number of A-to-D events in IEs:             61
Number of D-to-A events:                      27
  Number of D-to-A events in IEs:             27
Number of VHDL-AMS Breaks:                     0

Intrinsic tran analysis time = 600 ms.
Total time required for tran analysis 'tran' was 600 ms.

finalTimeOP: writing operating point information to rawfile.
modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
Simulation complete via transient analysis stoptime at time 20 US
Memory Usage - 15.2M program + 291.8M data = 307.1M total
CPU Usage - 0.8s system + 1.0s user = 1.9s total (16.9% cpu)
ncsim> exit
TOOL:   irun    06.11-s011: Exiting on Jan 14, 2009 at 09:09:53 MST  (total: 00:00:13)
```