Low power, small die-size PLL using semi-digital storage instead of big loop filter capacitance

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Abstract—Conventional low bandwidth Phase lock loop use an external Capacitor together with a big on chip ripple capacitor. A new architecture of a Phase lock loop is proposed which eliminates the need for an external capacitor. Also the value of the on chip capacitor is reduced to about one fifth, reducing the chip size. The PLL architecture proposed uses very low power.

Index Terms—**Phase lock loop, Low power, Real time clock**

I. INTRODUCTION

The architecture of the PLL   is shown in Fig 1. In conventional low bandwidth PLL's[1,2,4,5], the value of the Capacitance in the loop filter gets so big, that use of an external capacitance is mandatory. In addition to cost, off chip capacitors have the disadvantage of piezoelectric effects disturbing the PLL performance. Together with an off chip capacitor, a big on chip capacitor is needed (Ripple cap)[2]. In order to reduce cost, there is a need to remove the off chip cap and also reduce the chip size.

The architecture is not limited to low bandwidth PLL, it can be used to design high bandwidth PLL's as well. The architecture uses two charge pumps CP1 & CP2 (Fig 1). CP1 is used to provide proportional damping. CP2 is used for delay control block (DELCONT), which determines the loop bandwidth (the proportional part has to be set accordingly).
The big capacitor in the loop filter, storage cap, is replaced by a semi-digital storage here in DELCONT block. PVT compensation is achieved using the information stored digitally in DELCONT block.

II. DESCRIPTION OF THE BLOCKS

A. *DELCONT block & storage cells*

Storage cell is the most important part of this PLL architecture. The purpose of the storage cell is to store the information for VCO's running frequency in a semi-digital form. The VCO's tuning range is divided into N small steps and N storage cells are used. The storage cell has two functions:
a) Store the VCO tuning information digitally when being non active
b) Provide analog tuning when being active, to provide a smooth transition from one digital step to the next by analog tuning.
One of the implementation to achieve this is described below (fig 2):
S1, S2…SN are the storage cells. Their number depends on the VCO tuning range. By using this concept, a large tuning range can be achieved. The circuit diagram of the storage cell is shown in S1. It uses a small capacitance to store the analog voltage. The analog storage is active only for the cells which are active during VCO tuning, to achieve a smooth transition, minimum of two cells needs to be active. For all other cells, the information will be stored digitally with the help of two switches SW1(formed with P2 & P3) & SW2(formed with N1 & N3).

CP2 mirrors the current to pmos P1 & nmos N2. This current flows only if there is an UP or a DOWN Pulse from the PFD. If CP2 sees an UP pulse, VCO frequency (controlled by voltage B) should increase. In this case current through N2 is switched on and C1 will discharge. If a DOWN pulse is coming, pmos P1 will be active and C1 will charge. The time needed to charge/discharge can be controlled by choosing appropriate current mirror ratios. These currents should match to achieve low static phase offset. Pmos P6 initializes the capacitor at power up. Output A will depend on the voltage B at C1. If the voltage is above the threshold of the inverter (P5/N5) then the output is high otherwise it is low.

Referring to the interconnection of S1, S2…SN in fig 2, inputs L&H of Storage cell S2 can have three possible combinations, low-low, high-low, high-high. When low-low the voltage B at C1 will be pulled to high level and the storage cell is inactive. When high-low, C1 will keep its voltage and the storage cell is active. When both are at high level, then capacitor voltage will be pulled down to low level and the storage cell is inactive

In the beginning, all the storage cells (caps) are initialized to high level. That means VCO is getting no current from PN and it is running at lowest frequency, B<1: N> are set to VDD.

$$B < 1..N >_i = VDD \qquad (1)$$

PLL loop will try to increase the VCO frequency, so PFD will give wide UP pulses. These will discharge C1 inside S1. For S2 to SN, H and L terminals are at low level. So corresponding storage capacitors will be kept at high level with P2 & P3.Only S1 is active in this case. As soon as voltage B in S1 goes below the threshold voltage (VDD/2) of IV1 , A in S1 will go high (from low) which disables the pulling of C1 in S2 by turning off P3 . Capacitor C1 in S2 gets enabled for analog tuning. From this moment on, two caps of two consecutive storage cells are active and get affected by UP/DOWN generated by PFD. As soon as the OUT of S2 crosses the threshold voltage of IV1 in S2, S3 will be activated. As soon as this happens, H of S1 will get high level and then N1 & N3 inside S1 are activated and voltage B at C1 is pulled to low level and is kept. S1 is now inactive. The PLL loop is filling 0`s starting from B<1>.

The storage cells whose neighboring cells (A) are at same level (high or low) are disabled to high or low. Only the

storage cells (two in this case) whose neighboring cells (A) are at different level are enabled for analog tuning. At lock (i^{th} update cycle) m-1 storage cells are inactive and are LOW and N-(m+1) are inactive and HIGH.

$$B < 1 : (M - 1)_i >= 0 \qquad (2)$$

$$B < (M + 2)_i : N >= VDD \qquad (3)$$

Storage cells with the Voltage B<m:m+1> are active, this means for the length of Δt_i of the ith UP or DOWN pulse charge will be dumped at C1 (fig2). It would take a pulse of the length of *dt* to charge the voltage from VDD to GND.

$$B<m>_i = vdd \cdot (\sum_{i\_whileB<m>\_active\,\&\,DOWN} \frac{\Delta t_i}{dt} - \sum_{i\_whileB<m>\_active\,\&\,UP} \frac{\Delta t_i}{dt})$$
$$\dots(4)$$

$$B<m+1>_i = vdd \cdot (\sum_{i\_whileB<m+1>\_active\,\&\,DOWN} \frac{\Delta t_i}{dt} - \sum_{i\_whileB<m+1>\_active\,\&\,UP} \frac{\Delta t_i}{dt})$$
$$\dots(5)$$

$$f(i) = K_{prop} \cdot V_{prop}(i) + \sum_{j=1}^{m-1} K_{step} + K_{step} \cdot \frac{vdd - B<m>_i}{vdd} + K_{step} \cdot \frac{vdd - B<m+1>_i}{vdd}$$
$$---(6)$$

f(i) - average VCO frequency during i^{th} update
K_{prop} - proportional VCO gain(fig 3),
$V_{prop}(i)$ - is average voltage at PROP during i^{th} update pulse
K_{step} is - Frequency change per digital step

B. *Charge pumps & PFD*

There are two charge pumps used in this PLL architecture. CP1 in fig 3 and CP2 in fig 2. Referring to CP1(fig 3), Here the reference current is generated by using a programmable resistance SR1. The programming bits are derived from Storage cells for PVT compensation (will be described later). This current is mirrored to N2 & N3. When UP/UPB comes, P4 will supply a reference current to capacitor. On the other hand, when DOWN/DOWNB are generated, N3 through N7 will sink the reference current from the cap. This charge pump is used only for Damping.

In fig 2, is described second charge pump CP2. This has two matched branches with exactly same sizes and resistance values. Here also programmable resistances SR1 & SR2 are used to generate the reference current. When Up comes, current mirror formed with N12 are enabled and when DOWN is coming, then mirror of P11 are enabled.

PFD implementations can be referenced to [3] & [4].

C. *Voltage controlled oscillator*

The voltage controlled oscillator is shown in fig 3. A five stage single ended VCO is used here. The frequency of the oscillator depends on the current flowing through P11 & PN transistors. P11 pmos provides a proportional gain (proportional damping). PN is a special pmos which consists of N pmos connected in parallel. The voltage at PROP is biased to a reference voltage using two resistors R1 & R2. Here it is biased at VDD/2 (by choosing R1=R2). VCO frequency is controlled with B<1:N> signals. When all B<1:N> are at high level, VCO will output the lowest frequency. While all are at low level, VCO will give highest frequency. So VCO here can have a very wide range depending on the number of programming bits chosen here (B<1:N>). Fig 4 shows a simulation of the VCO frequency while CP2 is active continually(when UP is kept high). In this case B<1:N>(and A<1:N>) will start changing one by one. Between A<30> & A<40> there are ten A's(not plotted here). The VCO frequency change with respect to A(or B) is very linear and smooth.

III. PROCESS COMPENSATION

Process compensation is achieved using information in B<1:N> bits. Suppose VCO achieves target frequency at B<m> in nominal conditions. That means B<1:(m)> are at low level and B<(m+1):N> are at high level. From this point, as we move towards right or left, the VCO gain (frequency step from one B to the next B will change). The effect will be more if we move further away from B<m> and will be worse at the left and right extreme. To have a equal frequency steps from one B to the next over all B<1: N>, we can scale the sizes of the pmos's PN. So all N pmos will not have same size but a scaled one with respect to the pmos connected to B<m>.

Similarly the change in current through CP1 & CP2 can also be controlled using the same information (either B<1:N> or A<1:N>) to keep it constant across corners. Using this approach, we can compensate the PLL parameters over PVT.

IV. PROPORTIONAL DAMPING

In a traditional PLL the frequency of the VCO is only controlled by the Control Voltage. According to the phase difference of the reference signal and the divided VCO output, the charge pump will put a charge proportional to Ip*delta T on the loop capacitance. This Part of the Control Voltage is the storage part. In addition it will create a proportional component proportional to Ip*delta T* R. So the Control Voltage will be

$$V_{control} = storage + proportional = I_p \cdot \Delta T \cdot \tfrac{1}{s} \cdot C + I_p \cdot \Delta T \cdot R \qquad (7)$$

In this Semi digital PLL the Oscillator is not controlled by one voltage but by a proportional voltage and many storage voltages. Proportional voltage will be controlled like in a traditional analog PLL. To generate this Voltage, a voltage divider is used. As soon as the Charge Pump is switched off the current is turned off and the voltage settles at VDD/2.
Proportional voltage at the ith update(referring to VDD/2):

$$V_{prop}(i) = Icp \cdot \frac{R \cdot \Delta t_i}{T_{update}} \qquad (8)$$

Icp - charge pump current (CP1)
R - Effective damping resistor
Δt_i - phase difference at the ith update at the PFD inputs
T_{update} - Update period at the PFD input

V. SILICON IMPLMENTATION

The PLL is designed for real time clock (32.867 KHz) as input & 38.4MHz output frequency in 180nm technology. PLL bandwidth is set to 1KHz. PLL path has 32.867 KHz input

stage, PLL & 38.4MHz output stage. VCO is set to operate at double frequency (76.8MHz). Propotiona1 gain is set to 15MHz/V & Step gain is 400kHz/step. CP1 current is 15uA. Time to do one digital step if CP2 current is always flowing is dt=63us. Fig 5 shows phase noise LAB measurement on the chip. The layout of the chip is shown in Fig 6. The PLL together with input/output stages consume 700uA current. The total Die area of the chip is 0.95mm^2

VI. CONCLUSION

Using the PLL architecture described in this paper, very low bandwidth PLL can be designed without using any external components. The chip size used is also very small. The architecture uses very low power. This architecture is not limited to low Bandwidth PLL's only, High bandwidth PLL can also be designed with very small die size. The design is also proven by implementing in silicon.

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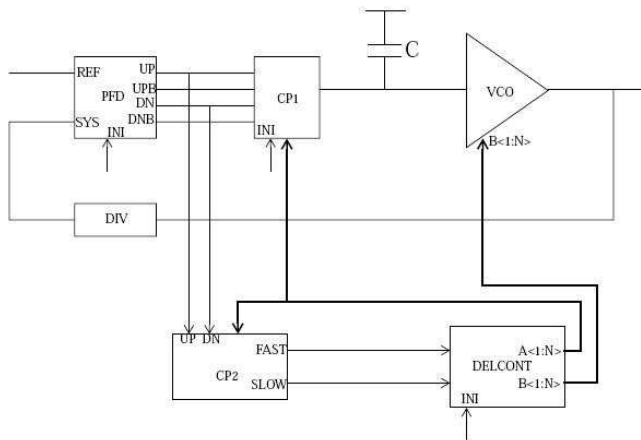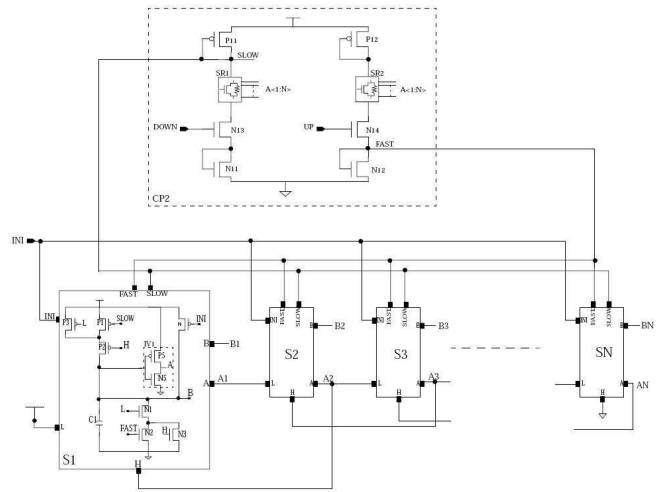
Fig 1: Block diagram of the PLL
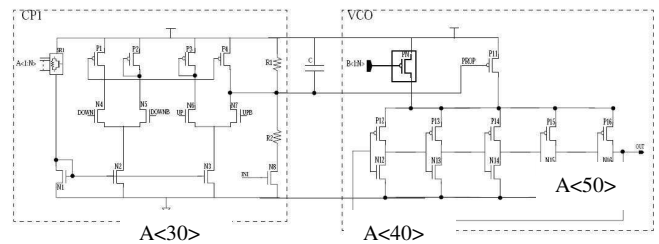

Fig 2: Storage cell & charge pump 2

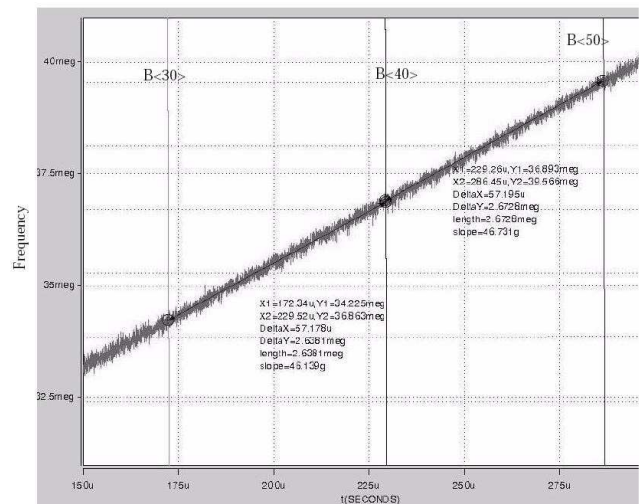Fig 3: Voltage control Oscillator & charge pump 1

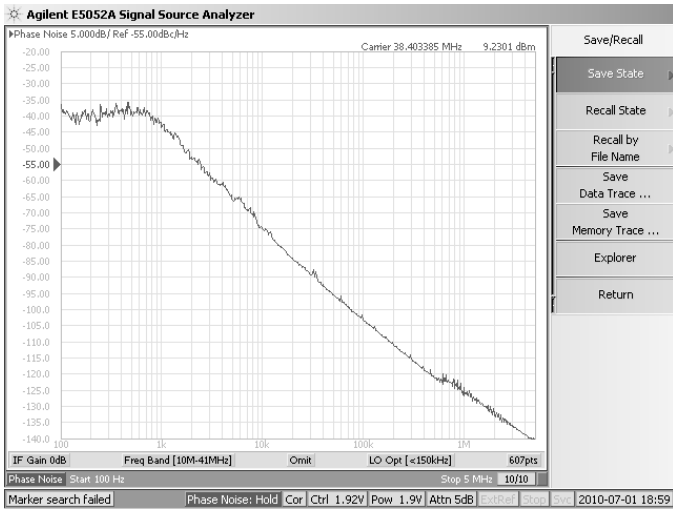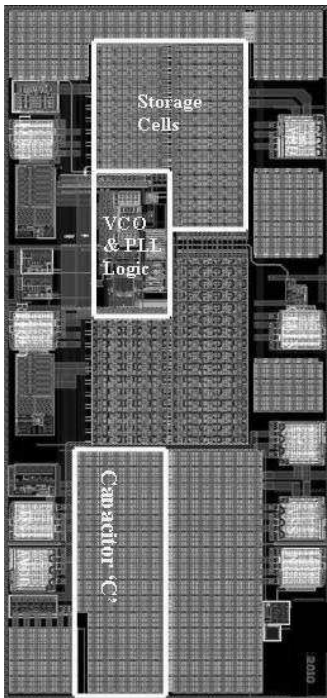Fig 4: VCO output frequency versus digital steps

Fig 5: Phase noise plot on the fabricated chip

Fig 6: Layout snapshot of the chip