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Analysis and design of amplifiers and comparators in CMOS 0.35 μm technology

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Abstract

Design techniques and CAD tools for digital systems are advancing rapidly at decreasing cost, while CMOS analog circuit design is related mostly with the individual experience and background of the designer. Therefore, the design of an analog circuit depends on several factors such as a reliable design methodology, good modeling and technology characterization. Most of this work focuses on the analysis of several analog circuits, including their functionality, using different design methodologies. Initially the determination of two key design parameters (slope factor n and early voltage VA) and the g_m/I_D characteristics were derived from simulations. Then, the analysis and design of three diferent analog circuits are presented. A comparison is made between two design methodology applied to an analog amplifier design. The first one is a conventional approach where transistors are in saturation. The second one is based on the g_m/I_D characteristic, that allows a unified synthesis methodology in all regions of operation of the transistor. The analog modules for comparison and continuous filtering, that find vast applications today, are then analyzed and designed with the parameters and methodology proposed.

1. Introduction

The development of very large scale integration (VLSI) technology, coupled with the demand for more signal processing integrated in a single chip, has resulted in a tremendous potential for design of analog circuits. Most VLSI systems require analog sub-systems such as amplifiers, comparators, filters, digital-analog and analog-digital converters, and so on.

The objective of analog circuit design is to map signal conditioning constrains into electronic circuit blocks that meet those specifications. This task is a challenging activity because the analog design procedure is based on several variables like noise, offset voltages, gain, drifts, etc., that are closely related to transistor sizing (technology dependency). So, the design process imposes to designers to make some choices based on their experience to achieve a successful design.

This work focuses on the analysis and design of several analog basic circuit blocks. Initially the characterization of two key design parameters (the slope factor and early voltage) is addressed. Then, a design methodology based on the g_m/I_D curve is used for the analysis and design of three different analog circuits: Miller amplifier, track-and-latch comparator and analog filter. This approach allows a unified synthesis methodology in all regions of operation of the transistor ranging from strong inversion to weak inversion.

This paper is organized as follows: Section 2 discusses the analog circuit design. Section 3 presents a brief review of analog circuit modeling, the characterization of two key design parameters is also presented. In Section 4, the design methodology based on the g_m/I_D curve and its main features are presented, where a quick comparison with a conventional design methodology of a Miller amplifier design is demonstrated. The application of the methodology to the design of analog modules for

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comparison and continuous filtering are then presented in Section 5. Finally, Section 6 presents our conclusions.

2. Analog circuit design

The objective of analog circuit design is to transform specifications into circuits that satisfy those specifications (schematics, netlists and layout). The designer must understand the process deeply enough to be able to model, layout, and test his chips, considering factors such as a reliable design methodology, good modeling and technology characterization.

Fig. 1 illustrates the steps of the design process of CMOS analog integrated circuits based on [1]. The designer is responsible for all these steps except fabrication.

First, an extensive characterization of the technology must be developed, where all the parameters that describe the electrical properties of the device are obtained. When this task is complete, an extensive analysis and modeling is made, transforming specifications into circuits with the transistor dimensions calculated. This leads to another important task—using electrical simulation to predict the performance of the circuit. Once the performance goals are satisfied, the designer is faced with the task of geometrical description (layout) of the circuit. Once the layout is finished, it is necessary to include the geometrical effects in a post-extraction simulation. If the results are satisfactory, the circuit is ready for fabrication. In case the specifications are not met, new design iteration must be undertaken.

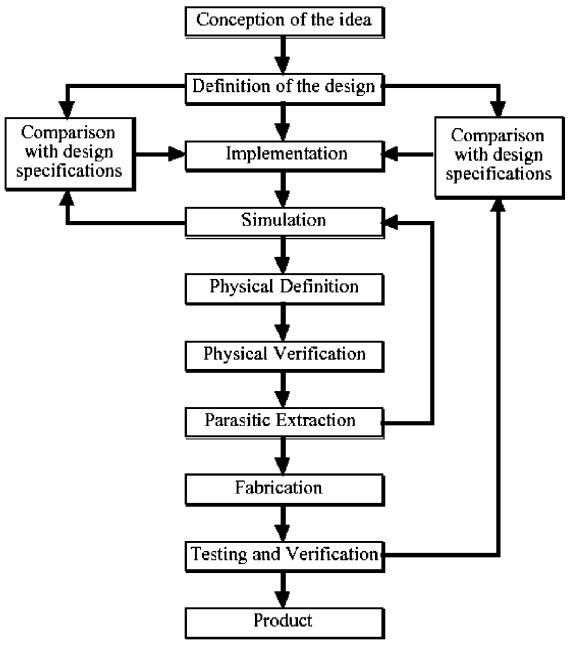

Fig. 1. Steps of the design process of CMOS analog integrated circuits [1].

3. Analog circuit modeling and device characterization

In order to develop a reliable design methodology for CMOS analog circuit design, an extensive study must be made aiming good device modeling and accurate technology characterization.

The first step is to characterize the technology about to be used in order to extract design parameters needed to the design. Several technology parameters that are supplied by the foundry are determined from the MOSFET BSIM3v3 model for the AMS 0.35 μm technology (Table 1).

Based on a conventional design methodology developed in [1,2], a zero-order model for the current I_D and the output resistance r_o can be obtained, considering that the transistors are in saturation:

$$I_D = \frac{\mu_0 \cdot C_{ox}}{2 \cdot n} \cdot \frac{W}{L} \cdot (V_{GS} - V_t)^2 \quad (1)$$

where $0 < V_{GS} - V_t < V_{DS}$,

$$r_o = \frac{VA}{I_D} \quad (2)$$

This simple model is suitable to hand calculations or computer analysis. The primary application of the model is to simulate or solve the behavior of the circuit. The behavior includes the biasing of the active devices, including capacitances, and small-signal analysis (AC analysis). Observing equations (1) and (2), it becomes clear the necessity of the characterization of two key design parameters: n (slope factor), in order to calculate the bias current, and VA (early voltage), in order to calculate the output impedance of the transistor.

3.1. Slope factor (n) parameter extraction

In order to calculate the bias current by means of a simple equation (Eq. (1)), the parameter n (slope factor) must be considered. The slope n can be translated as the inclination of the $\log(I_D)$ versus V_{GS} curve in weak inversion [3].

Table 1
Main parameters of the AMS 0.35 μm technology

	NMOS	PMOS
Nch	2.31e+17	1.03e+17 1/cm
μ_0	403.5	129.6 cm^2/V s
T_{ox}	7.7e−07	7.7e−07 cm
V_t0	0.465	−0.617 V
CGDO	2.1e−10	1.9e−10 F/m
CGBO	2.1e−10	1.9e−10 F/m

The extraction method based on [4], consider that the slope n can be obtained as the inverse of the derivative of V_P and V_{GB}. The pinch-off voltage (V_P) is defined as the channel voltage in the edge between the weak and strong inversion [5]. The relation of I_D with $V_P = V_{SB}$ can be obtained through electrical simulation (using the BSIM3v3 model) as shown in Fig. 2. The Is point (normalized current) is chosen to find the V_P correspondent. The relation of V_P with V_{GB} can be as shown in Fig. 3. The value of n can be obtained as the inverse of the derivative of V_P and V_{GB}. The obtained values are $n_{NMOS} = 1.22$ and $n_{PMOS} = 1.17$.

3.2. Early voltage (VA) parameter extraction

The output resistance (Eq. (2)) depends directly of the parameter VA, the early voltage. This parameter is

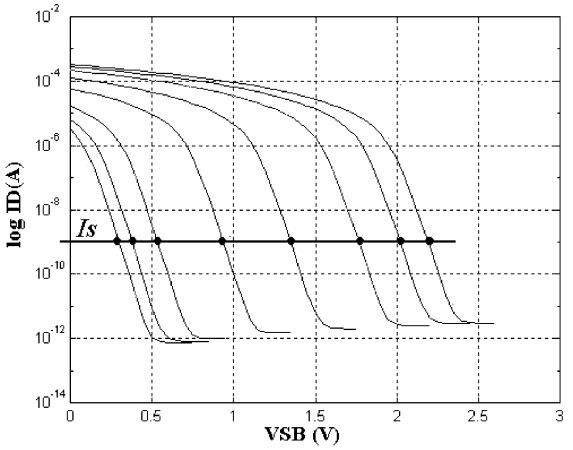

Fig. 2. I_D versus V_{SB} curve of a NMOS transistor.

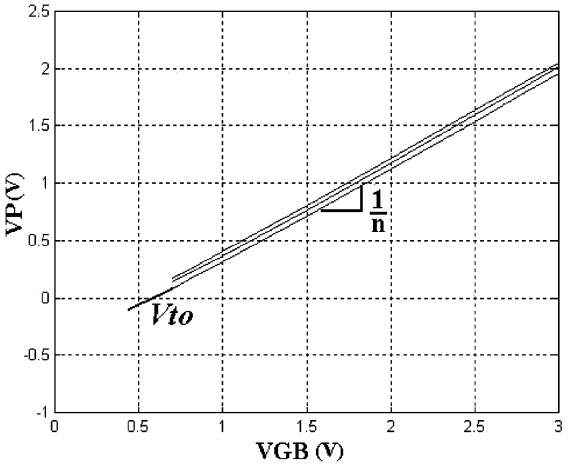

Fig. 3. V_P versus V_{GB} curve of a NMOS transistor.

Table 2
VA as function of the transistor length - $V_{GB} = 3$ V

L (μm)	VA (V)	
	NMOS	PMOS
1	129.5	27.55
2	178.8	48.06
2.5	204.05	57.99
5	297.3	103.9
7.5	357.8	151.5
10	426.2	198.9

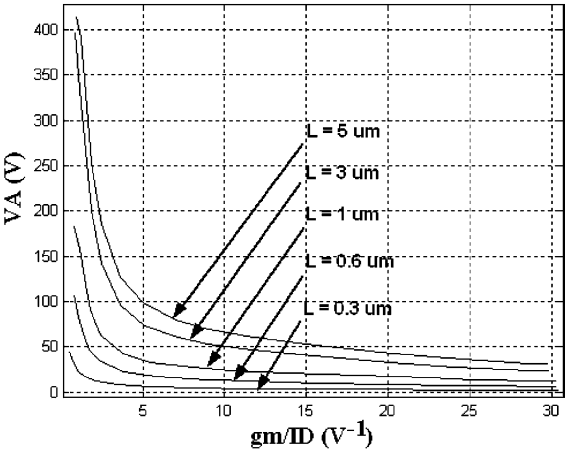

Fig. 4. The g_m/I_D versus VA curve—NMOS transistor.

the voltage per unit-channel length in analogy with the early voltage of a bipolar transistor [1]. This parameter depends directly on the channel length L of the transistor.

The extraction method based on [1,2], considers the channel-length modulation effect variation. Table 2 shows the values of VA, obtained through electrical simulation (using the BSIM3v3 model), as function of the transistor length L for a fixed voltage V_{GB}.

However, sometimes the designer must choose the region of operation of the transistor, and then the W/L of the transistor can be determined. Therefore, it is interesting to the designer to obtain the early voltage as function of the g_m/I_D characteristic, that gives an indication of the device operation region (see Section 4). Fig. 4 illustrates that. The VA versus g_m/I_D curve can be exploited during the design phase, when the transistors lengths are unknown.

4. The GM/ID design methodology

Most methods for analytical synthesis of analog circuits suppose that the MOS transistors are either in

strong inversion or in weak inversion. The design methodology based g_m/I_D characteristic, proposed by [6], allows a unified synthesis methodology in all regions of operation the MOS transistor.

In this method, we consider the relationship between the ratio of the transconductance g_m over DC drain current I_D and the normalized drain current $I_D/(W/L)$ as a fundamental design relation to explore the design space. The choice of g_m/I_D is based on its relevance for the following reasons:

- It is strongly related to the performance of analog circuits.
- It gives an indication of the device operation region.
- It provides way to determine the transistors dimensions.

Considering that the g_m/I_D ratio and the normalized current $I_D/(W/L)$ are independent of the transistor size [6], the relationship between them represent an unique characteristic for all transistors of the same type (NMOS and PMOS) in a given technology.

The "universal" quality of the g_m/I_D versus $I_D/(W/L)$ curve can be exploited during the design phase, when the transistors aspect ratios (W/L) are unknown. Once the value of the g_m/I_D ratio is chosen (the device operation region is determined), the W/L of the transistor can be determined in the curve.

Here the g_m/I_D versus $I_D/(W/L)$ curve is obtained analytically, using a MOS transistor model that provides a continuous representation of the transistor current and small-signal parameters in all regions of operations (the EKV model [3]), and from Spectre simulation using the BSIM3v3 model. Fig. 5 shows the calculated and simulated plots of g_m/I_D versus $I_D/(W/L)$ for NMOS and PMOS AMS0.35 μm transistors.

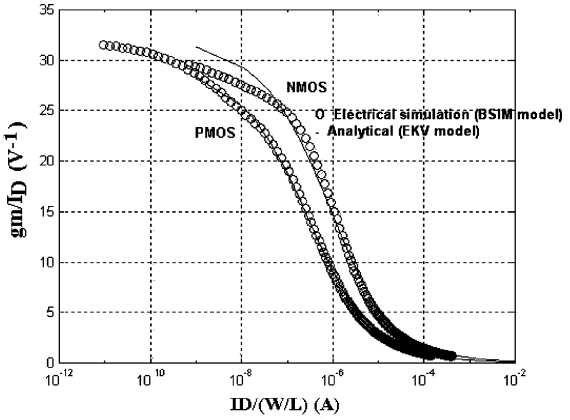

Fig. 5. Calculated (EKV model) and simulated (BSIM3v3 model) g_m/I_D curves for NMOS and PMOS transistors in CMOS 0.35 μm technology.

The g_m/I_D methodology was applied to the synthesis of a Miller amplifier, a two-stage operational amplifier with a feedback capacitor. Fig. 6 shows the amplifier schematics.

The specifications of the design of the Miller amplifier are the following: DC gain Av > 10,000 (80 dB), gain bandwidth GBW > 15 MHz, phase margin MF > 60°, input common mode range ICMR = −1 to 0.5 V, slew-rate SR > 18 V/μs, output load $C_L = 10$ pF and $V_{DD} = 1.65$ V and $V_{SS} = -1.65$ V. The design procedure is illustrated here aiming at best performances in terms of: dc gain (Av), phase margin (PM) and slew rate (SR). However, it can be modified to take account other performance aspects (like noise or common mode rejection), as long as they are directly related to the unified g_m/I_D versus $I_D/(W/L)$ relationship.

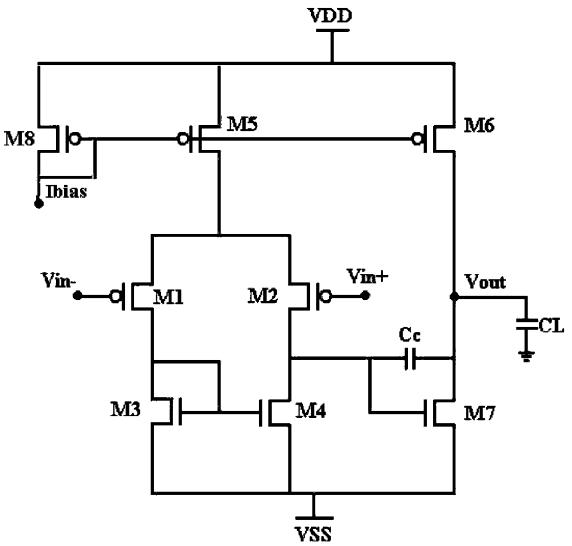

Fig. 6. Miller amplifier schematics.

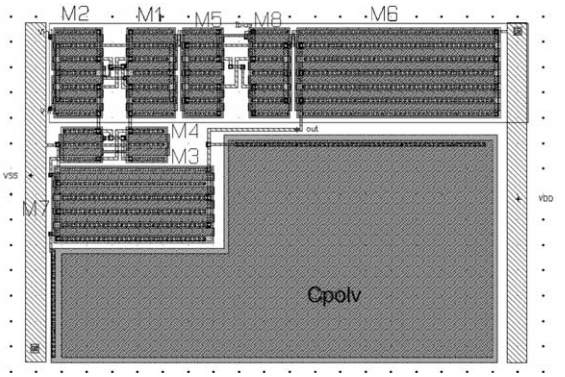

Fig. 7. Miller amplifier layout.

The design procedure is illustrated as follows:

- first, it is necessary to choose the value of the compensation capacitor Cc. From the desired phase margin, the value of Cc is chosen, i.e, for a 60° phase margin we use the following relationship: $Cc > 0.22 \cdot C_L \Rightarrow Cc = 2.5$ pF [1];
- the value of the bias current (Ibias) is determined based on the slew rate requirements: Ibias = 45 μA;
- the current mirror transistors (M3–M4) are operated in strong inversion to guarantee good matching and noise properties: $(g_m/I_D)_3 = (g_m/I_D)_4 = 10$;
- considering the GBW specification, the g_m/I_D ratio of the NMOS differential pair (M1–M2) can be determined: $(g_m/I_D)_1 = (g_m/I_D)_2 = 10.47$;
- from the relation $g_{m7} \geqslant 10 \cdot g_{m1}$ [1]: $(g_m/I_D)_7 = 10$;
- $(g_m/I_D)_5 = (g_m/I_D)_6 = (g_m/I_D)_8 = 7$, considering the transistors are operating in moderate inversion.

Choosing the values for g_m/I_D, the normalized current $I_D/(W/L)$ is determined for each transistor from the g_m/I_D versus $I_D/(W/L)$ curve. Then, with the drain current value found, the W/L of each transistor is found. The intended values of g_m/I_D are chosen according to their effect in the amplifier performance.

The transistors lengths L are determined by a trade-off between area on one side and dc gain (due to the dependence of the early voltage on the transistor length) on the other side. Here, L is considered five times the minimum-length allowed by the technology. The chosen values of the transistors sizes are shown in Table 3.

The circuit was implemented in 0.35 μm CMOS technology, using the CADENCE tool. In Fig. 7 the complete layout of the amplifier can be seen. The compensation capacitor was fixed at 2.5 pF, and layout as a double-poly capacitor. In this way, the non-linear gate capacitance effects will not interfere in the amplifier performance.

Table 4 shows the comparison between the performance calculated by a simple analytical model (see Section 2), and calculated by Spectre simulator (BSIM3v3 model). We can also observe the agreement between the performance simulated of the schematic version and post-layout version (including the parasitic effects).

Table 3
Miller amplifier transistor dimensions obtained through g_m/I_D design methodology

Transistor	W/L	W (μm)	L (μm)	g_m/I_D
M1	36	54	1.5	10.47
M2	36	54	1.5	10.47
M3	10	15	1.5	10
M4	10	15	1.5	10
M5	30	45	1.5	7
M6	158	237	1.5	7
M7	103	154.4	1.5	10
M8	30	45	1.5	7

Table 4
Performance results obtained for the Miller amplifier: analytical and electrical simulation

	Analytical	Electrical simulation	
		Schematics	Post-layout
Av (dB)	107.45	91.97	81.99
$F_{3\,dB}$ (Hz)	530	543	1.037K
PM (°)	60	56.4	55
GBW (MHz)	15	15.14	14.6
SR (V/μs)	18	20.7	20.42
I_{DD} (μA)	325.5	325.48	326.68

Table 5
Comparison of simulation results of g_m/I_D based design with conventional design

	Conventional method	g_m/I_D method
$(g_m/I_D)_1$	10.69	10.47
$(g_m/I_D)_3$	6.33	10
Av (dB)	90.85	91.97
PM (°)	55	56.4
GBW (MHz)	16	15.14
SR (V/μs)	19.2	20.7
I_{DD} (μA)	510.5	325.48

In order to further demonstrate the interest and potential of the g_m/I_D methodology, we compare its results with the results obtained from the conventional design methods based on the zero-order modeling where a current equation is simulation results for both implementations are shown on Table 5.

5. Design of analog building blocks

With a reliable design methodology defined, the analog building blocks of a continuous time band-pass Sigma–Delta Modulator (ΣΔ) were implemented. The system's specifications have been developed aiming the application showed in [7]. A comparator and continuous filter were analyzed and designed with the parameters and methodology proposed.

5.1. Track-and-latch comparator

The comparator is a building block for analog integrated circuit design, extensively used in analog-to-digital (A/D) and digital-to-analog (D/A) converters. The track-and-latch comparator [8], shown in Fig. 8, has NMOS input differential pair M1–M2, inverters M3–M8 and M4–M9 in positive feedback configuration, precharge transistors M6–M7, and a current source controlled (*phi*1) M5. It has the advantage of low stand-by

Table 6
Transistor sizes of the comparator in full-custom methodology

Transistor	W/L	W (μm)	L (μm)
M1	44	66	1.5
M2	44	66	1.5
M3	2.4	6	2.5
M4	2.4	6	2.5
M5	0.277	1.25	4.5
M6	3.33	1	0.3
M7	3.33	1	0.3
M8	0.8	2	2.5
M9	0.8	2	2.5

dissipation, since it shuts down current consumption after the clocked comparison.

The input signals have to be stable during the comparison. At the rising edge of the clock *phi*1, the pre-charge transistors are "open" and the differential pair is activated, initiating the comparison. In the pre-charge phase (inactive semi-cycle), the current of M5 (Itail) is turned off and the V_0^+ and V_0^- are reset and pre-charged to V_{DD}.

The speed of this type of comparator is strongly dependent on the Itail current, that is, speed is directly proportional to the current in M5.

The comparator was designed to meet the following specifications: 5 mV sensitivity, 5 MHz operating frequency, $C_L = 100$ fF, $SR_{min} = 100$ V/μs, $V_{DD} = 1.65$ V and $V_{SS} = -1.65$ V. The design has to optimize both the speed and the power consumption, as long as reasonable sensitivity and gain are achieved. Once the design operating frequency is reached, the power consumption is set by the current Itail. While the design does not meet the specifications, it is iteratively improved by changing the size of the differential pair M1–M2, until the desired performance is achieved. The transistor sizes of the comparator are shown in Table 6.

The track-and-latch comparator was implemented in 0.35 μm CMOS technology, using the CADENCE tool.

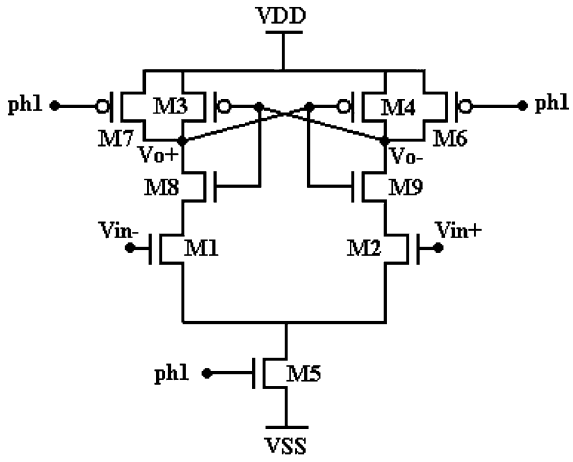

Fig. 8. Track-and-latch comparator schematics.

Table 7
Simulated comparator performance in 0.35 CMOS technology

	Schematics	Post-layout
Delay td_{hl} (ns)$_{phi1 \to V_0^+}$	8.63	7.88
Delay td_{lh} (ns)$_{phi1 \to V_0^+}$	5.15	5.20
$f_{máx}$ (MHz)	40	40
Sensibility $\Delta V_{in}(V_p)$ at 10 MHz	0.5 m	1 m
Itail (μA)	63.5	65

In Fig. 9 the complete layout of the comparator can be seen. The simulated performance results are shown in Table 7. We can note that the comparator maximum frequency is strongly dependent on the current that feeds the differential pair (Itail).

5.2. Gm-C band-pass filter

Integrated continuous-time transconductance-C (*Gm-C*) filters have been widely used for several applica-

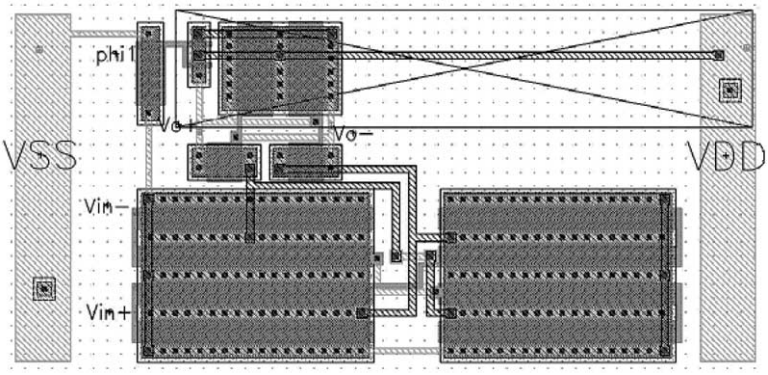

Fig. 9. Layout of the comparator.

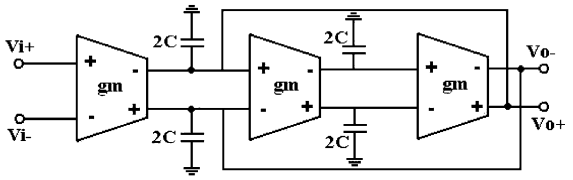

Fig. 10. A *Gm-C* band-pass filter biquad topology.

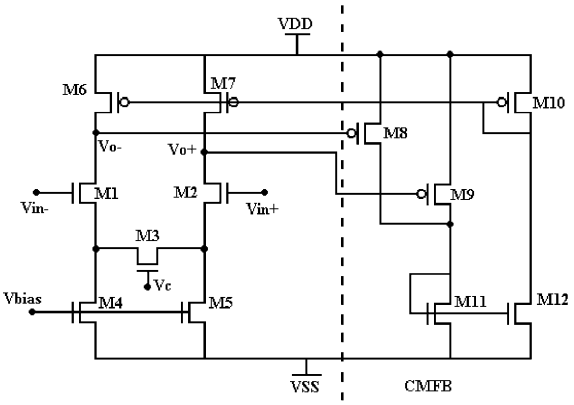

Fig. 11. Differential transconductor with CMFB schematics.

tions such as digital video, RF/IF filters, etc. [9]. *Gm-C* filters offer many advantages over other continuous-time filters in terms of low power and high-frequency capability.

The basic building block of a *Gm-C* filter is an integrator involving a transconductor and a capacitor. The transconductors employed in these filters must be linear over the expected signal swing, so it becomes very important the transconductor design.

Fig. 10 shows the fully-differential continuous-time *Gm-C* band-pass filter with a biquad circuit topology

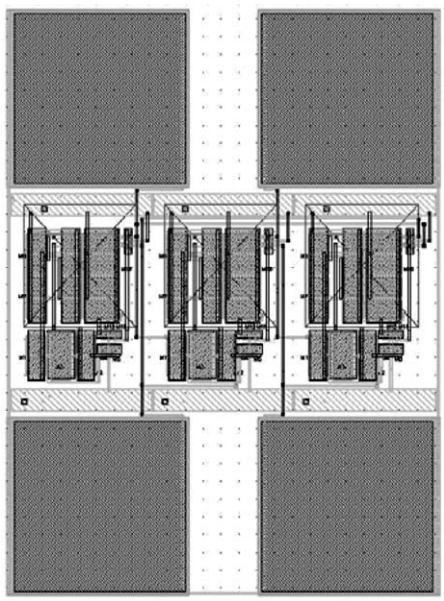

Fig. 12. Complete filter layout.

based on [10]. This topology was selected to provide a simple structure that demonstrated the capabilities of the technology and the transconductor design methodology.

Fig. 11 shows the transconductor used in the filter implementation. The source degeneration technique [10] was used for the transconductor linearization. The NMOS transistor M3, operating in the triode region controlled by the voltage VC, is employed as a tunable resistor.

The circuit was implemented in 0.35 μm CMOS technology, using the CADENCE environment. In Fig. 12 the complete layout of the filter can be seen. The four

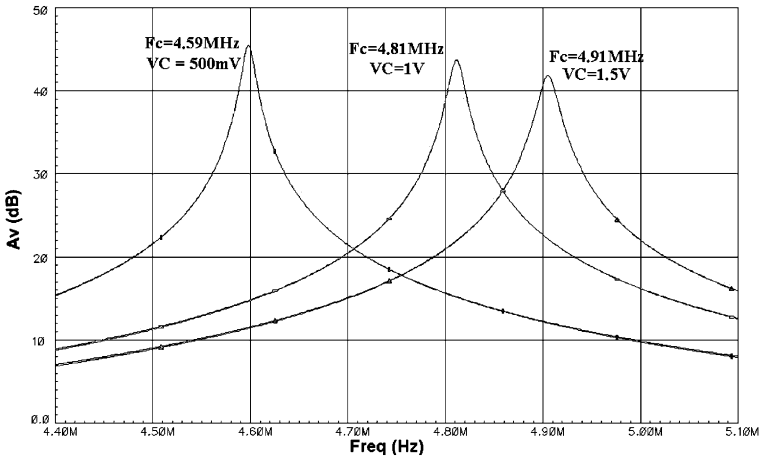

Fig. 13. Electrical simulation of the frequency response of the filter—post-layout version.

capacitors were fixed at 2 pF, and layout as a double-poly capacitor.

The design procedure followed the method developed in Section 3. Simulation results shows that the center frequency has a range of operation from 4.5 MHz and 5 MHz (Fig. 13) while the quality factor is about 250 (a small variation occurs because the transconductor output resistance).

6. Conclusions

The analysis and design using a design methodology based on the g_m/I_D characteristic of three different analog circuits were presented. For the Miller amplifier design, a comparison was made between a conventional design methodology and the g_m/I_D methodology, showing good results, the conventional approach overestimates the power dissipation and achieves a similar gain with larger transistor sizes. The methodology was also validated with electrical simulations (schematic and post-layout, Fig. 13) for the analog modules for comparison and continuous filtering.

Acknowledgements

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