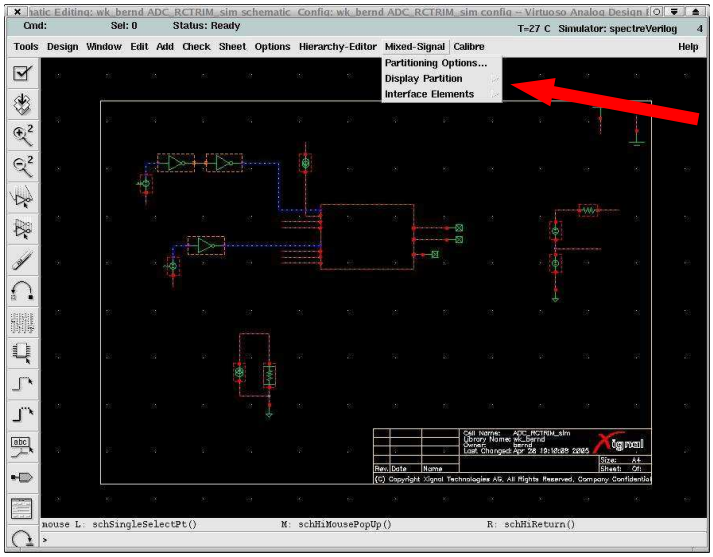

Figure 2.6: Viewing the partition

```
‘timescale 1ns/1ps
‘celldefine
module BUFX2 (Y, A);
...
```

Global Sim Time specifies a value for the global simulating time.

Global Sim Precision a global precision value for the global simulation time.

The Xignal defaults are:

Global TimeScale Overwrite Schematic TimeScale = TRUE

Global Sim Time = 10ps

Global Sim Precision = 1ps

4. Check the *Verilog-XL Options*, with *Simulation–>Options–>Digital ...*, figure 2.8. Use the Verilog Options Form to set the location to the Verilog model library the file that contains all Verilog module definitions. `$TECH_DIR/verilog/<veriloglib>.v`

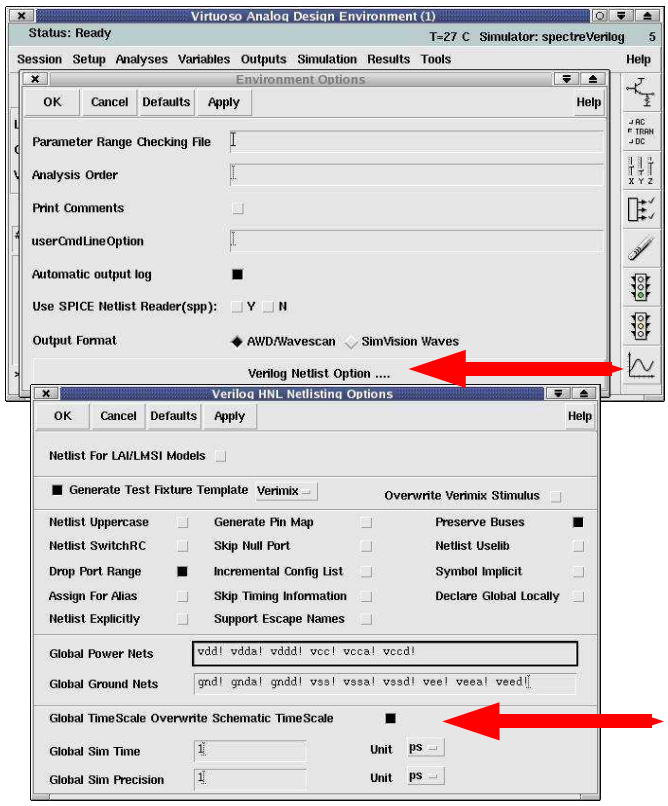

Figure 2.7: ADE Environment Options & Verilog Netlist Options

is the Xignal default. Use the Options Form also to define the delay mode and delay type.

Mode globally alters the delay values specified in your design.

Default uses all of the delays in your netlist.

Zero ignores all module path delays, timing checks, and structural and continuous assignment delays.

Path uses delay information from specified blocks that contain module path delays. It ignores structural and continuous assignment delays.

Unit ignores module path delays and timing checks and converts all structural and continuous assignment delays that are nonzero to one time unit.

Distributed uses the delay on nets, primitives, and continuous assignments. It ignores module path delays.

Type specifies the delay type.

Minimum selects all minimum delays.

Typical selects all typical delays.

Maximum selects all maximum delays.

5. Finally run your Spectre-VerilogXL simulation.

2.3 UltraSim-VerilogXL

1. Select the mixed-signal simulator, for a coupled UltraSim-VerilogXL simulation, select *UltraSimVerilog*, figure 2.9.

2. View the partition in the schematic, as for Spectre-VerilogXL.

3. Check the *Verilog Netlist Options*, as for Spectre-VerilogXL.

4. Check the *Verilog-XL Options*, as for Spectre-VerilogXL.