Research Letter

Investigation of CMOS Varactors for High-GHz-Range Applications

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This paper explores a variety of different CMOS varactor structures for RF and MMICs. A typical 0.18 μm CMOS foundry process was used as the study platform. The varactors' capacitance-voltage characteristics and cutoff frequencies have been examined up to 55 GHz. The primary aim of this work is to design varactors that can improve nonlinear-transmission-line (NLTL) pulse-compression circuits. The results should also be valuable for other applications up to millimeter wavelengths.

1. Introduction

Fast-developing CMOS technologies, with cutoff frequencies over 200 GHz [1], have made millimeter-wave silicon RF and MMICs a reality [2, 3]. These devices help fill the demand for low-cost, low-power, and compact wireless communication products. CMOS varactors, as key components in many RFICs, have received much attention [2–5].

In [6] we discussed six different CMOS varactor structures. They were divided into two groups: one group with monotonic, the other with nonmonotonic $C(V)$s. Two of the structures were manufactured in a 0.18-μm CMOS foundry technology and were tested up to 26 GHz. The capacitance-voltage characteristics $C(V)$s and cutoff frequencies of all six structures were investigated and compared for pulse-compression applications. We developed a strategy to generate CMOS varactors with nonlinear capacitances that are suitable for either single-edge or double-edge pulse compression.

Very few publications have discussed the behavior of CMOS varactors above 50 GHz [2, 3]. Paper [4] gives a very good overview of CMOS varactor structures but covers only up to 5 GHz. Paper [5] has a good discussion of CMOS varactors, but the analysis is based on standard foundry-supplied models, which do not normally extend above 20 GHz range. Here we extend our varactor study to 55 GHz, and we focus on four of the six varactor structures. Figure 1(a) shows an AMOS (accumulation-mode MOS) varactor, and

Figure 1(b) an IMOS (inversion-mode MOS) varactor. Both have monotonic $C(V)$ characteristics. Figure 1(c) depicts a standard NMOS varactor in which the source-drain is connecting to the bulk and producing a nonmonotonic $C(V)$. The structure in Figure 1(d) has differently doped source and drain; we call this device an SnDp (N-type source, P-type drain). Its $C(V)$ is also nonmonotonic. As pointed out in [6], a monotonic $C(V)$ is beneficial for single-edge pulse compression while a nonmonotonic $C(V)$ is more suited for double-edge pulse compression.

We present the $C(V)$ and cutoff frequency curves of the four kinds of fabricated CMOS varactors at 1 MHz, 5 GHz, 20 GHz, and 55 GHz. Simulations and testing results are compared. The results should be most useful for NLTL pulse-compression applications where high harmonic generation is critical, but also of general value in the development of CMOS MMIC technology.

2. Varactor Fabrication and Measurement

The four varactor structures were fabricated in a commercial 0.18-μm CMOS process. The IMOS and NMOS varactors (structures 2 and 3) were standard components in the process. The AMOS varactor (structure 1) was not supported by this process. The SnDp varactor (structure 4) could only be realized with the standard CMOS process by violating the design rules [7]. Both structures required extra layout work.
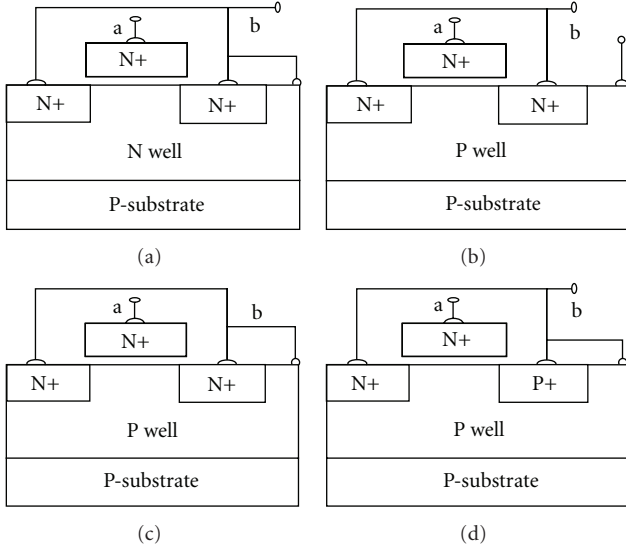
Figure 1: Four different CMOS Varactor Structures: (1) AMOS, (2) IMOS, (3) NMOS, and (4) SnDp types.

The fabricated structures were tested using an HP 4280A 1 MHz capacitance meter for low-frequency behavior. For GHz-range measurements, we used an Agilent N5250A Performance Network Analyzer (PNA) with built-in bias tees, a Karl Suss PA 200 probe station, and programmable heads with Picoprobe GSG-67A-100 probes. On-wafer measurements were extracted up to 67 GHz but for accuracy, postmeasurement calculations were carried only to 55 GHz. A CS-5 calibration kit was used to set the measurement reference plane to the tip of the probes. Koolen's "Open" and "Short" technique [8] was used to deembed the extrinsic parameters due to use of pads, interconnects. A simplified model of the extracted varactor is shown in Figure 2. The parasitic L's and R's are deembedded from all three terminals: DS (drain and source), G (gate), and B (bulk). This yields the intrinsic model shown in the box (Figure 2). The input admittance Y_{in} looking into terminal G in Figure 3 can be extracted as

$$Y_{in} = jw \left[\frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}} + C_{parasitic} \right] + G_{dep} + G_{parasitic}. \quad (1)$$

3. CMOS Varactor Behavior

We simulated the four CMOS varactor types up to 55 GHz, using the Medici process-oriented device simulator [9].

Figure 3 shows the results for the AMOS varactor. The left column contains the simulated data, the right column the measured data. The top row shows the $C(V)$ curves, the bottom row the cutoff frequencies. Similarly, Figure 4 shows the results for the IMOS varactor, Figure 5 for the NMOS varactor, and Figure 6 for the SnDp varactor. In order to evaluate the loss and Q values, Figure 7 shows the series resistances for AMOS, SDF, and SDB varactors at 5 GHz.

On the chip, the gate of each varactor has a length of 0.5 μm, a width of 5.0 μm, and a total of 12 fingers.
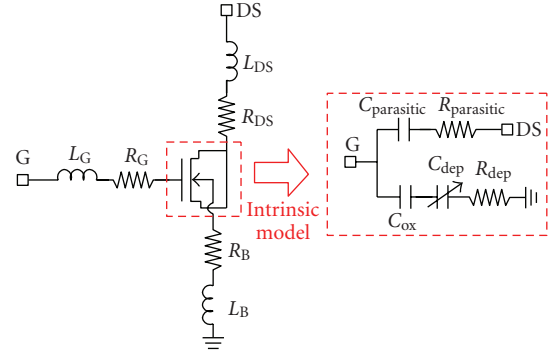

Figure 2: CMOS intrinsic varactor model.
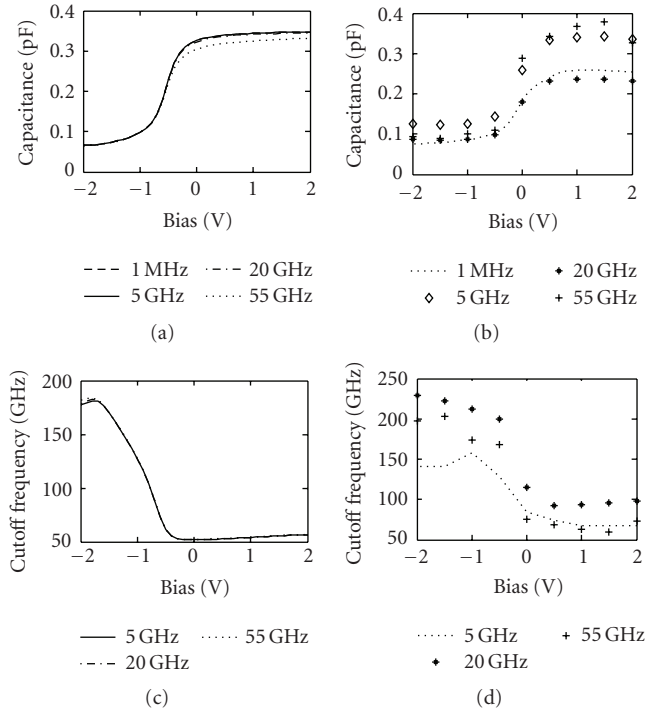

Figure 3: Simulated and measured data for the AMOS varactor.

In the simulation setup, the gate length was 0.5 μm, the width 1.0 μm (Medici's default value), the thickness of the gate oxide 2.5 nm, the two-step uniform well dopings 8×10^{17} cm^{-3}, and 2×10^{17} cm^{-3}, respectively [10]. Therefore, the simulated capacitance was multiplied by 60 to match the measured data.

4. Discussion

The AMOS and IMOS varactors have monotonic $C(V)$ characteristics. The AMOS varactor data of Figure 3 show that on the average, the simulated C_{max}/C_{min} ratios are ~3.8 while measured values are ~3.4. The simulated cutoff frequencies are ~135 GHz while measured values are ~130 GHz. The IMOS varactor data of Figure 5 show that on the average both the simulated and measured C_{max}/C_{min} ratios are ~3. The cutoff frequencies are both ~100 GHz.
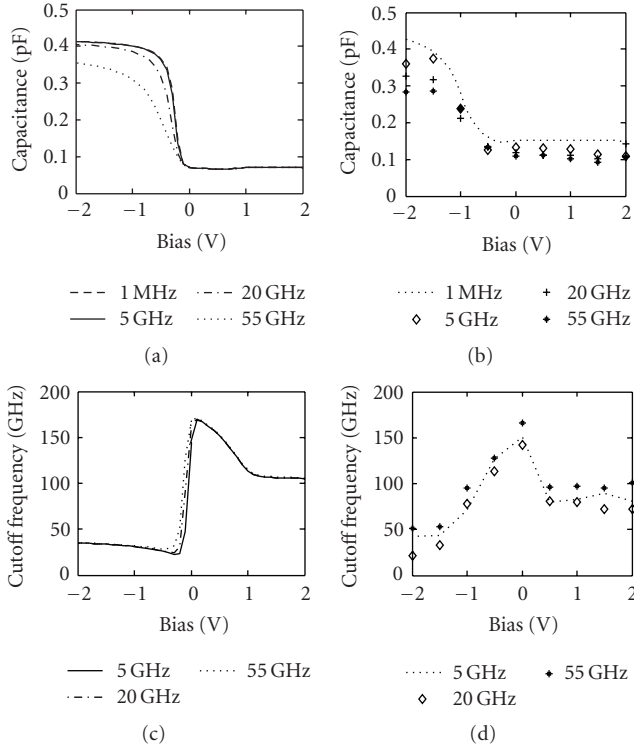
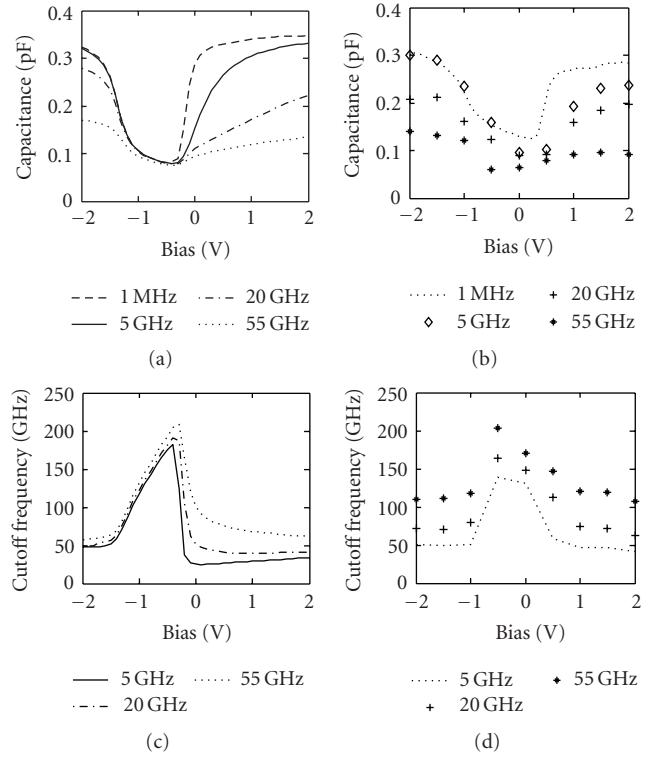FIGURE 4: Simulated and measured data for the IMOS varactor.

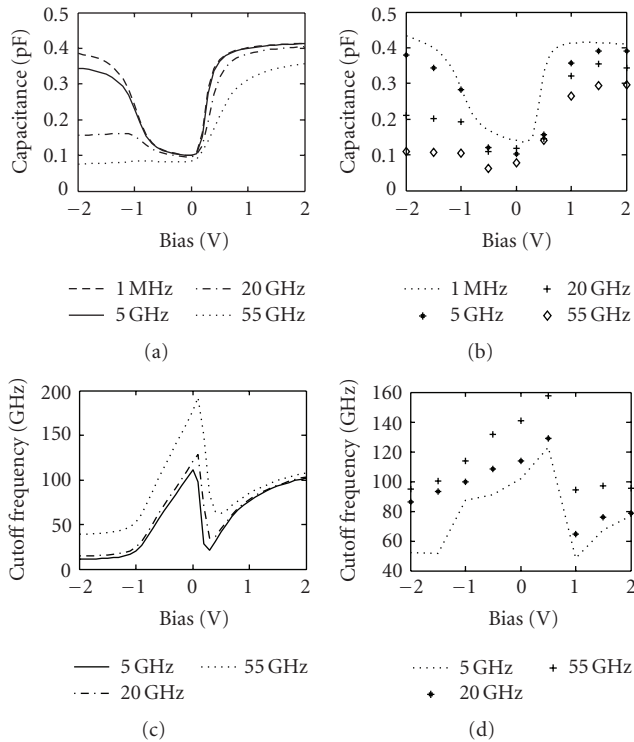FIGURE 5: Simulated and measured data for the NMOS varactor.

FIGURE 6: Simulated and measured data for the SnDp varactor.

Of particular interest is the frequency-dependence of the $C(V)$ curves. For the AMOS varactor, see Figure 3, the simulated $C(V)$s vary little from 1 MHz to 55 GHz. For the IMOS data of Figure 4, the simulated and measured $C(V)$ curves both show decreased nonlinearity as the frequency increases. The reason for this degeneration is that the IMOS varactor has a larger channel resistance than AMOS varactor (shown in Figure 7), since in the IMOS structure the well makes no contribution to the channel conductivity.

The NMOS and SnDp varactors have nonmonotonic $C(V)$ characteristics. Figure 5 shows that on the average, the NMOS varactor simulations predict C_{max}/C_{min} ratios of ~3.6 compared with measured ratios ~3.4. However both simulated and measured $C(V)$ curves degenerate toward monotonicity as frequency increases. The simulated average cutoff frequencies are ~100 GHz while the measured values are ~95 GHz. Figure 6, for the SnDp varactor, shows that at lower frequencies, the average simulated C_{max}/C_{min} ratios are ~3.0 and the measured ratios ~2.7. Both simulated and measured SnDp $C(V)$ curves are flattened in the 20-to-55 GHz range, with C_{max}/C_{min} ratios dropping dramatically. In Figure 6, the average cutoff frequencies are all ~100 GHz.

The relatively poor high-frequency response of the SnDp structure is due to the need for carriers to travel the full length of the channel from the S or D region. In the other structures, carriers need only to travel half the length of the channel. To test this contention, we also simulated NMOS and SnDp varactor structures at 55 GHz with gate lengths shortened to $0.2 \mu m$. Figure 8 compares the results with those obtained for the same devices with $0.5 \mu m$ gates. All capacitances are normalized to the same gate area. Figure 8 shows that with a short-gate length, the SnDp varactor
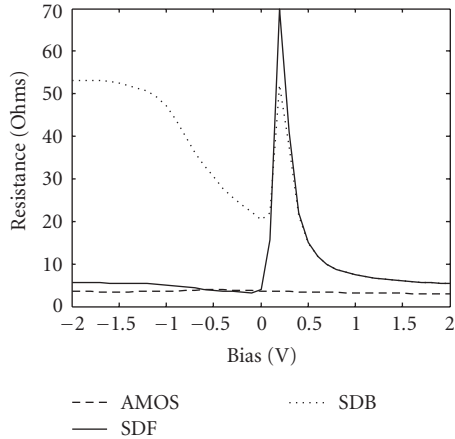
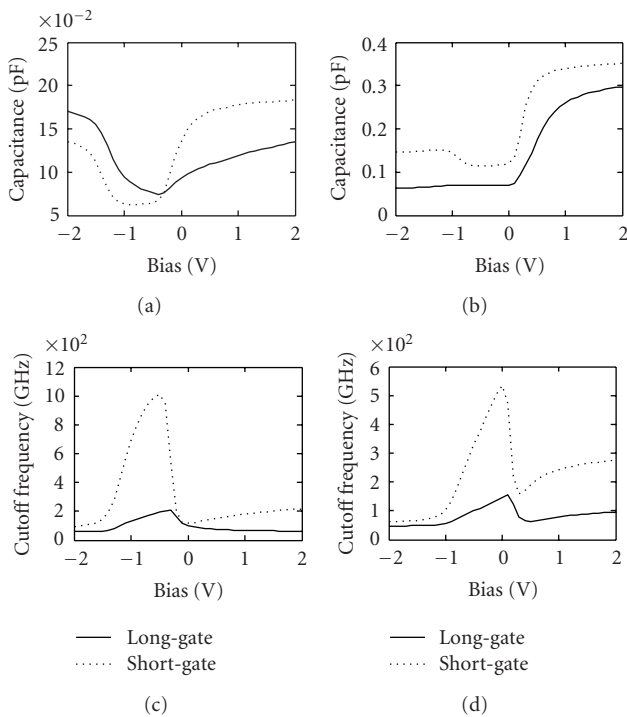FIGURE 7: Series resistances of AMOS, SDF, and SDB varactors at 5 GHz.

(a)

(b)

(c)

(d)

FIGURE 8: SnDp varactor versus NMOS varactor at 55 GHz (short-gate = 0.2 μm, long-gate = 0.5 μm).

has reduced $C(V)$ degeneration and a much higher cutoff frequency than the NMOS varactor.

5. Conclusion

Both AMOS and IMOS varactors are good for single-edge pulse compression due to their higher C_{max}/C_{min} ratios and cutoff frequencies. However, the AMOS varactor has an advantage over the IMOS varactor because its $C(V)$ curve does not degenerate at higher GHz frequencies, as shown in Figure 3, and it has lower series resistance; see Figure 7. Both NMOS and SnDp varactors are good for double-edge pulse

compression. However, the high-frequency degeneration restricts their use to a much lower GHz range. Using a short-gate SnDp varactor can reduce its high-frequency degeneration and improve its performance, as indicated in Figure 8. Our research also shows that because of the lack of degeneration of its $C(V)$ characteristic at high frequencies and no resistance peak near the depletion region, the AMOS varactor should be a good candidate for high-GHz-range applications.

Acknowledgment

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