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MIXED SIGNAL LETTER

Compact low voltage high-Q CMOS active inductor suitable for RF applications

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Abstract A compact active inductor circuit is proposed. The circuit is based on the gyrator-C approach with both transconductance stages realized by MOS transistors in common-source configuration. The circuit has minimal number of transistors, is suitable for low voltage operation, offers a wide inductive band, high quality factor and low power dissipation. Simulation results are provided for a 0.13 μm CMOS process with 1.2 V supply voltage.

Keywords Active inductor · Low voltage · Quality factor · Radio-frequency integrated circuit

1 Introduction

The increasing popularity and growth of wireless communications has inevitably boosted research in the field of radio-frequency integrated circuit (RFIC) design, especially in CMOS technology due to the shrinking of sizes and low cost availability of the process. The inductor, an essential component in RF design, finds use in many blocks such as oscillators, filters, phase shifters, low noise amplifiers, impedance matching circuitry, biasing, etc. [1–4]; however their implementation still remains to be a challenging task in CMOS. An on-chip passive inductor presents major disadvantages such as large silicon area, limited inductance value and quality factor. Most of the time, the inductor will be a major factor in determining the total chip area [4] where higher inductance values imply larger area consumption. Furthermore, their values are not precise even if the technology is well-characterized [3, 5]. On the other hand, active inductors offer much less area consumption independent of the desired inductance value, high quality factors and tunability. Although the noise performance and dynamic range will be degraded, it can be maintained at low enough levels for many applications.

Many active inductor implementations can be found in literature [1, 2, 4, 6, 7]. However, each one of them offers only one or a few of the desirable specifications such as compactness, low voltage operation, wide inductance band, high quality factor, low power consumption, high dynamic range, low noise and tunability.

This letter presents a compact high-Q active inductor implemented in a 0.13 μm CMOS process. The circuit offers almost all of the above specifications in one block. It is based on the gyrator-C approach [8] with both transconductors uncharacteristically realized by MOS transistors in common-source configuration which allows comparably low conductances at critical nodes, hence improved performance. A current mirror is used both to adjust the transconductance and provide biasing to the second stage, thus allowing minimal number of transistors. The circuit is arranged in such a way that no transistor suffers from body effect and is suitable for low voltage operation. Simulation results show that the inductor can be used in many RF applications ranging in the 900 MHz–6 GHz frequency band.

2 Proposed active inductor

The active inductor proposed is depicted in Fig. 1. It is based on the gyrator-C approach shown in Fig. 2(a) [8], with its equivalent passive model given in Fig. 2(b). It can be easily shown that the input impedance function Z_i

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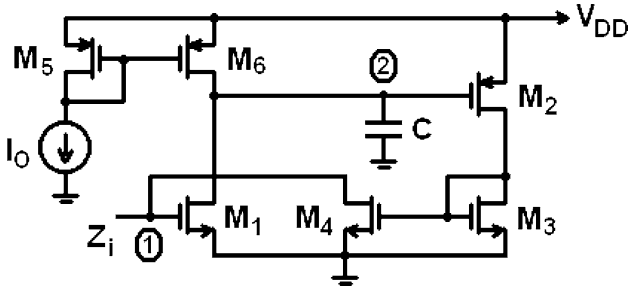

Fig. 1 Proposed active inductor

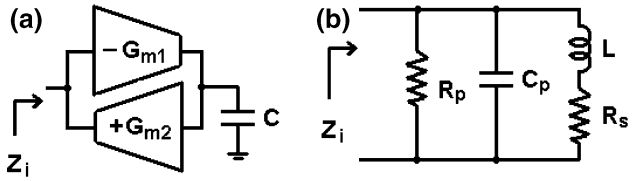

Fig. 2 (**a**) Gyrator-C realization of the active inductor (**b**) Equivalent passive model

has two poles and a zero. Standard circuit analysis techniques yield

$$\omega_Z = \frac{G_2}{C_2} \quad \omega_P = \sqrt{\frac{G_{m1}G_{m2} + G_1G_2}{C_1C_2}} \tag{1a}$$

$$Q_P = \frac{\sqrt{(G_{m1}G_{m2} + G_1G_2)C_1C_2}}{G_2C_1 + G_1C_2} \quad Q_L = \frac{\omega C_2}{G_2} \tag{1b}$$

$$L = \frac{C_2}{G_{m1}G_{m2}} \quad R_S = \frac{G_2}{G_{m1}G_{m2}} \quad C_P = C_1 \quad R_P = \frac{1}{G_1} \tag{1c}$$

where ω_Z, ω_P, Q_P are the zero frequency, self-resonance frequency and quality factor of the resonant circuit, respectively, Q_L is the inductor quality factor, G_1, G_2, C_1 and C_2 are the respective equivalent conductance and capacitances at nodes 1 and 2.

The negative transconductance is realized by M_1 in common-source configuration, whereas M_2–M_4 form the positive transconductance where the simple current mirror comprised of M_3–M_4 is used to invert the negative transconductance of M_2, also configured in common-source connection. M_5–M_6 are used for biasing purposes. The biasing of M_1 can be handled externally by the block the inductor will be incorporated into, or by a current multipled from the M_3–M_4 current mirror. Since the sole contribution practically comes from a minimum number of MOS transistor drain terminal(s), this configuration allows low equivalent conductances especially at node 2 which results in improved performance.

The proposed circuit offers many advantages all in one block. It contains only six transistors of which none of them suffers from body effect which would otherwise modify G_{m1} and/or G_{m2}. The compactness of the circuit results in low power consumption.

According to Eq. 1c, the inductance L and its series resistance R_S is independently adjustable by C_2 and G_2 (I_o), respectively. By neglecting the output capacitance of M_1, one can write $C_2 = C + C_{i2}$, which shows capacitor C can be used for inductance tuning and makes minimizing C_{i2} insignificant where C_i denotes the input capacitance of the MOS transistor. Capacitor C also serves for ensuring the stability of the circuit. Since the open-loop transfer function has two poles very close to each other, introducing a dominant pole at node 2 improves stability. The maximum value of the inductance band depends on minimizing $C_1 = C_{i1} + C_{o2}$ for a constant value of L. This can be achieved by a small-size input transistor.

The minimum voltage required for proper circuit operation is $V_{gs} + V_{dsat}$ which makes it suitable for low voltage operation where V_{dsat} is the minimum V_{ds} voltage required to keep a MOS transistor in saturation. The voltage swing at the input is $V_t \leq V_i \leq V_{DD} - V_{dsat}$ where V_t denotes the threshold voltage. Since only two transistors contribute to the input noise directly, it is expected that the circuit has low noise.

3 Simulation results

The active inductor circuit has been simulated in Cadence using parameters for UMC 0.13 μm CMOS process with V_{DD} = 1.2 V. All transistors have minimum channel length of 0.13 μm. The width of the transistors, the values of I_o and C were chosen to optimize the quality factor of the inductor as W_1 = 4 μm, W_2 = 14.4 μm, $W_3 = W_4$ = 3.6 μm, $W_5 = W_6$ = 10 μm, I_o = 135 μA, C = 104 fF. The input bias voltage is 500 mV. Simulation results show that this choice yields G_{m1} = 1.7 mS, G_{m2} = 3.1 mS, G_1 = 258 μS, G_2 = 304 μS, C_1 = 12 fF.

The simulated frequency response of the inductor is given in Fig. 3. The circuit has a very wide operating bandwidth where the inductive characteristic extends from 300 MHz up to the self-resonance frequency at 7.32 GHz with a nominal inductance of 38 nH. Q_P = 61 is obtained at self-resonance, and Q_L > 100 (>10) in the 4.8–6.4 GHz (2.35–7 GHz) band whereas the phase error is less than 1° over the frequency range 4.4–6.5 GHz. Q_{Lmax} = 3,900 is achieved at 5.75 GHz.

It is worth mentioning that L and R_S can be varied independently. Inductance values between 38 and 144 nH can be obtained by varying capacitor C in the range of 104–500 fF where the dependency proves to be linear. For

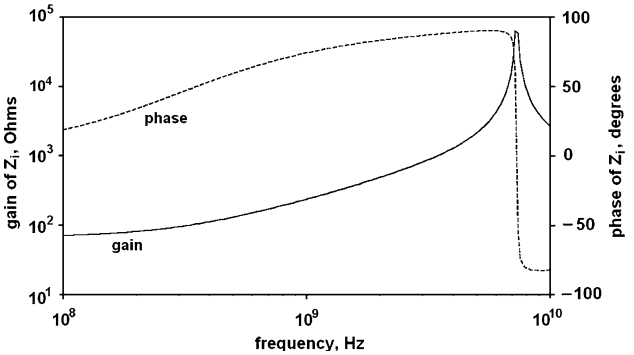

Fig. 3 Frequency response of the active inductor

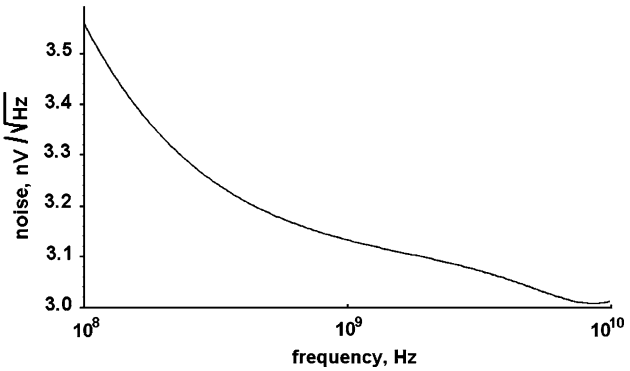

Fig. 5 Noise performance of the active inductor

practical purposes, capacitor C can be replaced by a MOS varactor. Variation of R_S is provided by changing I_o from 120 to 135 μA. This implies Q_L to be varied between 10 and 3,900 for a constant inductance value. Tunability of Q_L is demonstrated in Fig. 4 for 5 μA steps of I_o between 120 μA and 135 μA.

Transient simulations show that there is no danger of instability. Provided that the total harmonic distortion is less than 1%, the maximum input voltage swing at 5.75 GHz was found as 18 mV. The circuit has a spurious-free dynamic range of 30 dB where the total noise voltage was integrated over a 500-MHz bandwidth. The noise performance of the circuit is given in Fig. 5 which proves to be low as expected.

Since the number of transistors in the circuit is minimal, the power dissipation is as low as 1 mW.

Simulations were carried out in order to measure the robustness of the proposed circuit against transistor parameter variations. Analysis of Eq. 1 shows that the most important parameters which affect L and Q_L in this regard are the transistor channel widths. Statistical analysis performed on the circuit yields a quality factor of $Q_L > 10$ over the frequency range 2.45–6.4 GHz, where $\Delta W/W = 2\%$ was assumed. As a result, no significant performance degradation is expected in terms of the inductance quality factor. No noticeable change in the inductance value was observed for the same conditions.

In order to emphasize the performance of the proposed inductor, Table 1 compares this work to previously published active inductors. It should be noted that the structure in [2] is differential. Comparison of performances proves that the low voltage active inductor circuit presented has wide inductance band, high quality factor, low power consumption, high dynamic range and low noise.

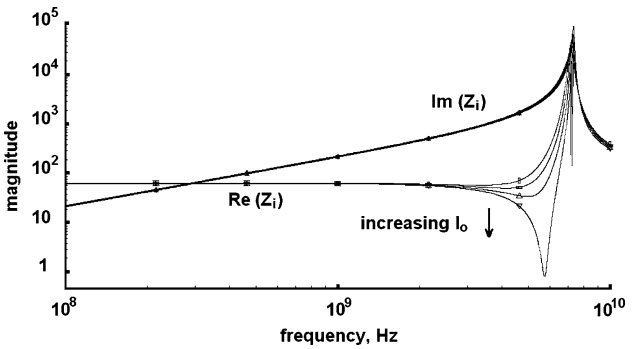

Fig. 4 Q_L tuning of the inductor for I_o = 120, 125, 130, 135 μA

Table 1 Comparison of active inductor performances

Parameter	Ref. [2]	Ref. [6]	Ref. [7]	This work
Technology	0.13μm/1.5 V	0.35μm/1.5 V	0.6μm	0.13μm/1.2 V
Inductive bandwidth	n. a.	6.8 MHz–2.97 GHz	800 MHz–2.5 GHz	300 MHz–7.32 GHz
L (nH)	2.5–13	30.9	15–300	38–144
$Q_{L\max}$	100@5GHz	434@1GHz	350@1GHz	3900@5.75GHz
P_{dis} (mW)	18.6/68 (2 modes)	0.6	n. a.	1
Max. input voltage swing	n. a.	4.5 mV	n. a.	18 mV
Dynamic range	n. a.	30.8 dB	n. a.	30 dB
Noise	n. a.	91.3 μV[a]	n. a.	3.1 nV/√Hz

[a] Integrated over 500 MHz bandwidth

4 Conclusion

A compact active inductor circuit suitable for low voltage operation is proposed. The circuit offers a wide inductive band, high quality factor, low power consumption and tunability. Simulation results are provided for a 0.13 μm CMOS process. Results show that the circuit can be used in many RF applications ranging in the 900 MHz–6 GHz frequency band.

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