A 2.4-GHz 0.18-μm CMOS Self-Biased Cascode Power Amplifier

Tirdad Sowlati, *Member, IEEE,* and Domine M. W. Leenaerts, *Senior Member, IEEE*

***Abstract*—A two-stage self-biased cascode power amplifier in 0.18-μm CMOS process for Class-1 Bluetooth application is presented. The power amplifier provides 23-dBm output power with a power-added efficiency (PAE) of 42% at 2.4 GHz. It has a small signal gain of 38 dB and a large signal gain of 31 dB at saturation. This is the highest gain reported for a two-stage design in CMOS at the 0.8–2.4-GHz frequency range. A novel self-biasing and bootstrapping technique is presented that relaxes the restriction due to hot carrier degradation in power amplifiers and alleviates the need to use thick-oxide transistors that have poor RF performance compared with the standard transistors available in the same process. The power amplifier shows no performance degradation after ten days of continuous operation under maximum output power at 2.4-V supply. It is demonstrated that a sliding bias technique can be used to both significantly improve the PAE at mid-power range and linearize the power amplifier. By using the sliding bias technique, the PAE at 16 dBm is increased from 6% to 19%, and the gain variation over the entire power range is reduced from 7 to 0.6 dB.**

***Index Terms*—Bluetooth, CMOS, power amplifier.**

I. INTRODUCTION

THERE HAS been an increasing interest in designing RF power amplifiers in digital CMOS technology, such as the 0.35- and 0.25-μm processes. This stems from the trend to integrate a complete transceiver together with the digital baseband part on a single chip. The wireless communication standard Bluetooth is one of the applications that requires CMOS integration to achieve low cost and therefore consumer acceptance. Recently, several fully integrated transceivers in CMOS technology for Bluetooth have been demonstrated [1]–[4]. The power amplifier in integrated Bluetooth transceivers usually meets the Class-3 requirements of 0-dBm output power. An additional power amplifier with 20-dB gain is needed to amplify this signal to meet the Class-1 output power requirement of 20 dBm.

There are two main issues in the design of power amplifiers in submicron CMOS, namely, oxide breakdown and hot carrier effect. Both of these get worse as the technology scales. The oxide breakdown is a catastrophic effect and sets a limit on the maximum signal swing on drain. The hot carrier effect, on the other hand, is a reliability issue. It increases the threshold voltage and consequently degrades the performance of the device. The recommended voltage to avoid hot carrier degradation is usually based on dc/transient reliability tests. For production requirements, the recommended voltage is 5%–10% above the maximum allowed supply voltage to guarantee a product lifetime of ten years. For a 0.18-μm process, this leads to a maximum dc drain–gate voltage of 2 V. CMOS power amplifiers have been reported with the dc voltage below the recommended voltage, but with the dc + RF voltage levels exceeding the maximum allowed value [5]. The performance degradation due to hot carrier becomes evident during the first few hours, and the output power of the amplifier decreases in the order of 1 dB after 70–80 hours of continuous operation [6]. Though the performance degradation can be compensated by adjusting the gate bias voltages, it is desirable to have a design that does not need adjustment over time.

The fact that the signal swing in a power amplifier can be two to three times the supply voltage means that the supply voltage must be smaller than the maximum voltage allowed in the technology. Designing a power amplifier at a smaller supply voltage has several drawbacks. In order to get the same output power, the impedance at the output must be reduced by the square value of supply reduction.[1] The output current becomes larger by the inverse of the supply reduction. This increases the loss in the parasitic resistors in the matching network and the transistor. A larger transistor is required to handle the larger current which in turn increases the parasitic capacitances. This reduces the input impedance of the power stage, making the interstage matching more difficult. Overall, the gain and efficiency are reduced as a result of reduced supply voltage.

Cascode configuration and thick-oxide transistors [7], [8] have been used to eliminate the effects of oxide breakdown voltage and the hot carrier degradation, allowing the use of a larger supply voltage. So far, in cascode power amplifiers, the common-gate transistor has had a constant dc voltage with an ac (RF) ground. Under large signal operation, the voltage swing on the gate–drain of the common-gate transistor becomes larger than that of the common-source transistor. Therefore, the common-gate transistor becomes the bottleneck in terms of breakdown or hot carrier degradation. In [7], the 900-MHz 0.2-μm CMOS cascode power stage uses a combination of standard and thick-oxide devices (standard device for the common-source and thick-oxide device for the common-gate). The thick-oxide device is equivalent to a device in 0.35-μm process, so it can tolerate a much larger voltage. However, a thick-oxide device does not have the same high-frequency performance of the standard device. A cutoff frequency Ft of 26 GHz is typical for thick oxide in a 0.2-μm CMOS compared

Manuscript received July 30, 2002; revised April 2, 2003.

T. Sowlati was with Philips Research-USA, Briarcliff Manor, NY 10510 USA. He is now with Skyworks Solutions Inc., Irvine, CA 92629 USA.

D. M. W. Leenaerts is with Philips Research, 5656 AA Eindhoven, the Netherlands.

Digital Object Identifier 10.1109/JSSC.2003.814417

[1] $Ro = V^2/(2.Po)$ where Ro is the output impedance, V is voltage and Po is the output power.

with its standard device which has a typical Ft of 50 GHz. The thick-oxide device basically provides a lower gain at RF. In a cascode combination of thick and standard devices, the thick device limits the high-frequency performance. In other words, even though we use a more advanced technology (0.2-μm process compared with 0.35-μm process), we cannot exploit the higher frequency performance of the scaled-down devices.

This work demonstrates a 0.18-μm CMOS self-biased cascode RF power amplifier (PA) that operates at 2.4 GHz and provides 23 dBm from a 2.4-V supply voltage. Although many RF PAs have been demonstrated in submicrometer CMOS [5]–[10], this design is the first one in a 0.18-μm CMOS technology that can operate at 2.4 V without soft breakdown or hot carrier degradation [11]. By using standard oxide thickness devices in the process (and not thick-oxide devices), the design takes full advantage of the technology and its high Ft. The two-stage design provides 38-dB small-signal gain and 31-dB large-signal gain close to saturation at 2.4 GHz. This is the highest gain reported for a two-stage design in submicrometer CMOS at the 0.8–2.4-GHz frequency range. The high gain simplifies the driver stage in the existing Bluetooth transceiver ICs.

The outline of this paper is as follows. In Section II, the self-biased and bootstrapped cascode techniques are introduced and compared with a conventional cascode configuration. In Section III, the design of the two-stage self-biased PA for Class-1 Bluetooth application is described. The measurement results are presented in Section IV. In Section V, the sliding bias technique is demonstrated to improve power-added efficiency (PAE) significantly at low and mid-power levels, and also reduce gain and phase nonlinearities (AM-AM and AM-PM conversion). Finally, in Section VI, conclusions are given.

II. Self-Biased Cascode Topology

A conventional cascode amplifier is shown in Fig. 1(a). Transistor M1 acts as a common source (CS) and transistor M2 acts as a common gate (CG). The RF signal is applied to G1.[2] Gate G2 is RF grounded with a dc value of V_{dc} which can be equal to the supply voltage V_{dd}. The RF ground at G2 can be achieved by either an off-chip or an on-chip capacitance resonating with the bond-wire inductance. The dc voltage at D2 is equal to the supply voltage with an RF voltage swing around this value. At maximum output power, the voltage at D2 swings down close to zero and up to twice V_{dd}. In order to increase the efficiency, the voltage can be shaped by the choice of the matching network. In the cascode configuration, transistor M1 has a smaller drain–gate voltage swing. This is because the voltage at D1 is always lower than voltage at G2 by an amount equal to the gate–source voltage of G2. Consequently, the supply voltage is limited by the breakdown voltage of M2 rather than M1. This can also be observed from Fig. 1(b) which shows the time domain voltage waveforms for this amplifier. In this simulation, the supply voltage is 2.4 V and the operating frequency is 2.4 GHz.

To overcome this problem, we propose a self-biased cascode transistor [Fig. 2(a)] that allows RF swing at G2. This enables us to design the PA such that both transistors experience the

[2]The dc bias of G1 is not shown for simplicity.

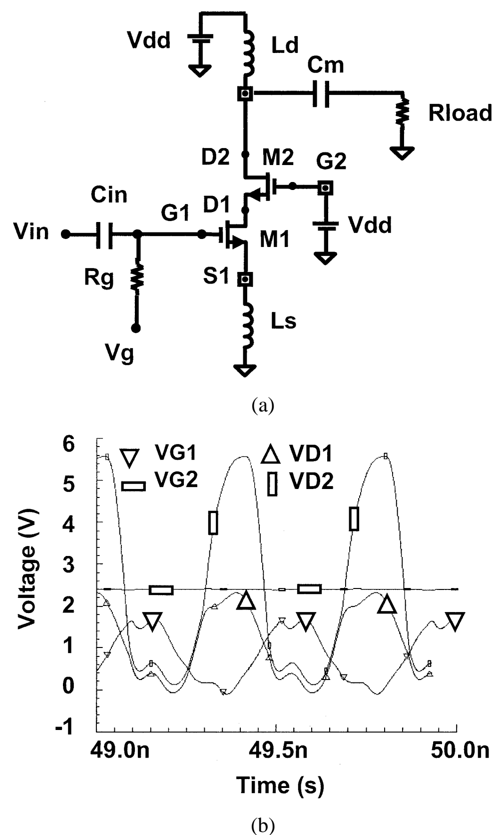

Fig. 1. (a) Conventional cascode amplifier. (b) Voltage waveforms versus time.

same maximum drain–gate voltage. Consequently, we can have a larger signal swing at D2 before encountering hot carrier degradation. The bias for G2 is provided by Rb–Cb, for which no extra bondpad is required. The dc voltage applied to G2 is the same as the dc voltage applied to D2. The RF swing at D2 is attenuated by the low-pass nature of Rb–Cb [Fig. 2(b)]. The values of Rb and Cb can be chosen for optimum performance and for equal gate–drain signal swings on M1 and M2. As G2 follows the RF variation of D2 in both positive and negative swings around its dc value, a nonoptimal gain performance is obtained (compared with a cascode with RF ground at G2).[3] However, as long as both M1 and M2 go from saturation into triode under large-signal operation, the maximum output power and PAE are not degraded. The effect of the self-biased concept is demonstrated in Fig. 2(b). Here, the same dimensions of the devices are used as for the case presented in Fig. 1(b). A reduction of more than 20% in the drain–gate voltage of M2 is obtained.

To further extend this idea, we can add a resistive-diode boosting [see Fig. 3(a)] so that the positive swing of G2 can be made larger than the negative swing. By choosing the value of Rd and the size of the diode connected transistor M3, we can specify the threshold voltage at which the Rd–M3 starts conducting and boosting the positive swing at G2. This extra path enables G2 to follow the rise in D2 with a smaller attenuation than the fall in D2. During this transient response,

[3]The gain remains larger than the gain of a conventional cascode with thick-oxide transistor. A conventional cascode PA with standard oxide transistor could only be used with a lower supply voltage which results in a smaller gain compared with the self-biased cascode.

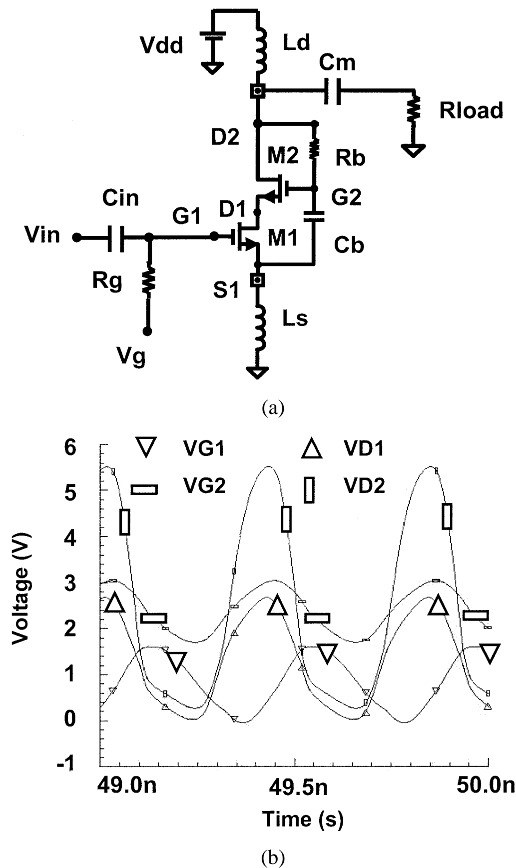

Fig. 2. (a) Self-biased cascode amplifier. (b) Voltage waveforms versus time.

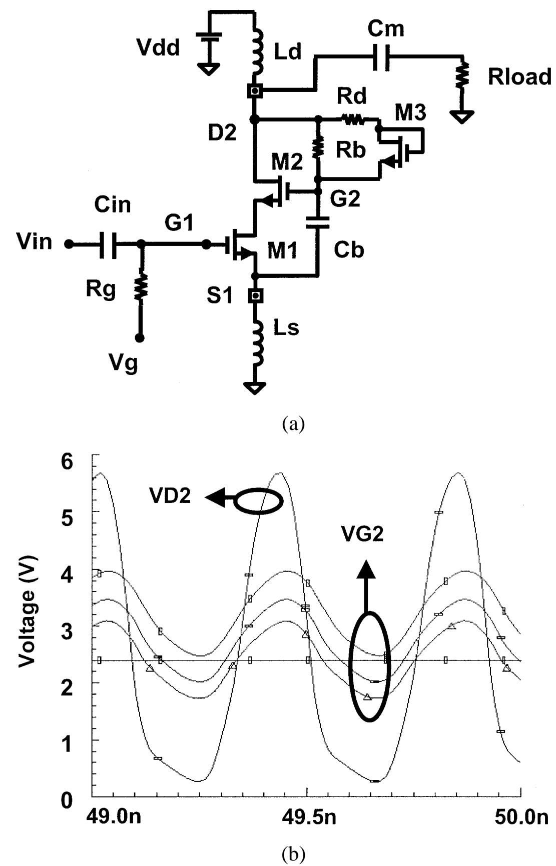

Fig. 3. (a) Bootstrapped cascode amplifier. (b) Voltage waveforms versus time (VG2 shown for three different values of Rd).

the average charge stored on Cb increases causing Rd–M3 to conduct for a smaller percentage of the duty cycle. The average voltage at G2 increases up to the point where Rd–M3 no longer conducts. In steady state, the Rd–M3 path is off and the positive and negative swings at G2 are equal. Fig. 3(b) shows the drain and gate voltages of transistor M2 versus time for different values of Rd. The voltage swing at D2 is not affected by Rd, and the peak-to-peak swing of VG2 depends on Rb–Cb and not Rd. However, as the value of Rd is reduced, the average voltage of VG2 increases. In Class-E PA design, the voltage swing can be about three times the supply voltage (with a larger positive swing than negative around supply). In this situation, the bootstrapped cascode configuration [Fig. 3(a)] can be used to have the same maximum voltage swings at gate–drain of M1 and M2. Therefore, a larger supply voltage can be applied, resulting in a higher output power. For Class-AB/B design, where the signal has roughly the same positive and negative swings around the supply voltage, the self-biased cascode provides the required swing on G2.

III. Power Amplifier Design

The PA was built up around two stages, having an equivalent total gain of three stages in order to simplify the output driver in the existing Bluetooth transceiver ICs. In both stages, we used the self-biased cascode topology. The *RC* time constant was set to about 200 MHz to have an optimal transfer characteristic of the drain voltage to the gate voltage. The two-stage PA is shown in Fig. 4. In the driver stage, the transistors M1 and M2 are 0.6- and 0.3-mm wide, whereas in the power stage the transistors are 2- and 1.5-mm wide, respectively. All devices have the minimum length of 0.18 μm. The gates of the driver and power stages are biased at 0.55 and 0.8 V, respectively. The input and output matching networks are designed to be off chip to increase matching flexibility and avoid excessive power loss of on-chip inductors. Capacitors C1 and C5 are dc blocking capacitors for the 50-Ω source and load. Inductors L1 to L7 are wirebond inductors connecting bondpads of the die to the printed circuit board (PCB) for RF and dc connections. Traces on the PCB (TL1 to TL7) are used as transmission lines as part of the input, inter-stage, and output matching networks. The input is matched to 50 Ω by using an external parallel capacitor C2. The

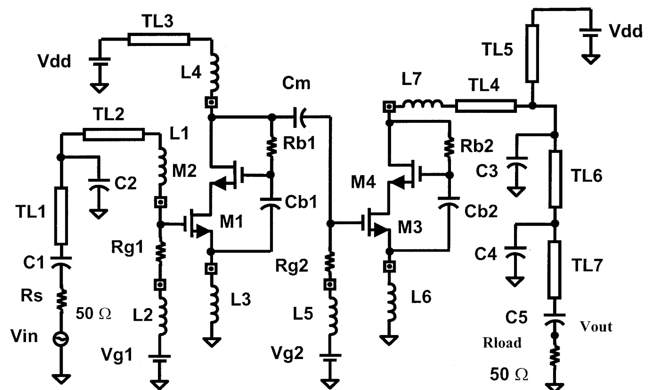

Fig. 4. Two-stage self-biased cascode PA.

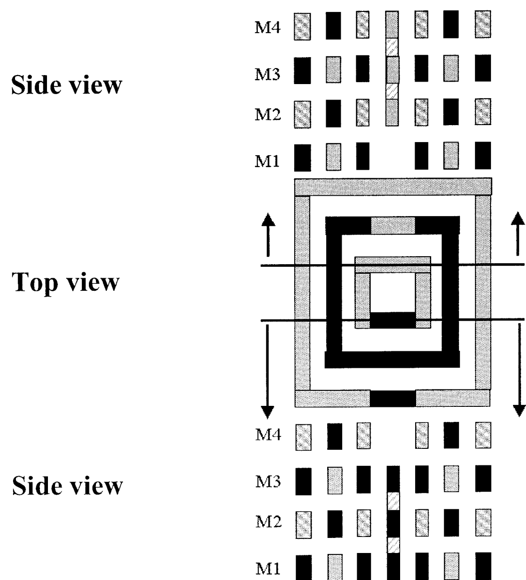

Fig. 5. Horseshoe capacitor top and side views. (Grey: node A; Black: node B of capacitor.)

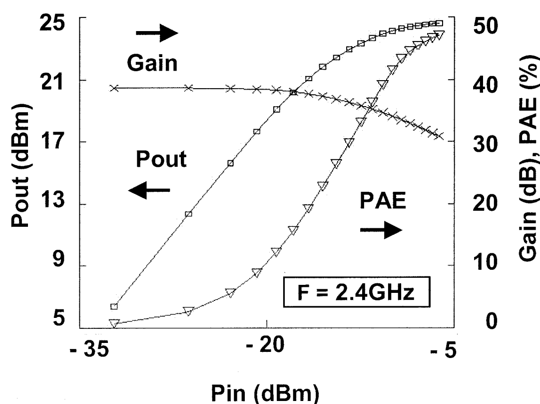

Fig. 6. Two-stage self-biased cascode PA.

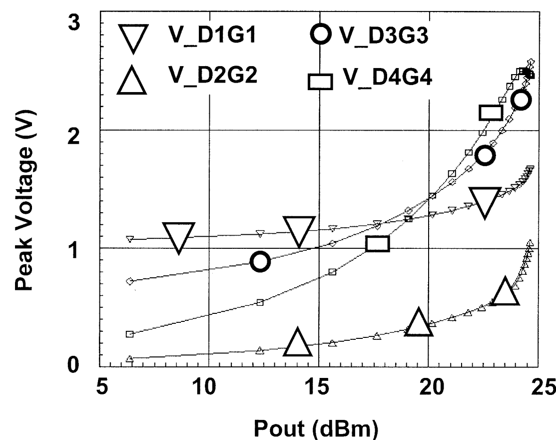

Fig. 7. Two-stage self-biased cascode PA.

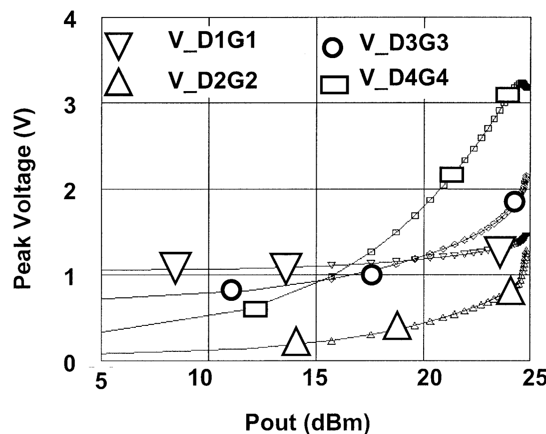

Fig. 8. Two-stage self-biased cascode PA.

inter-stage matching is done by a high-pass *LC* section, consisting of the wirebond inductor L4 and on-chip capacitor Cm. A two-step matching network is used to transform the load to the optimum load at the drain of the output transistor M4. It is composed of transmission lines TL4 to TL7 (traces on PCB) and two parallel capacitors C3 and C4 which also short circuit the second and third harmonics to ground. The inductance of the wirebond L7 at the output is absorbed as part of the matching network.

Deep-submicrometer CMOS processes lack a double-poly capacitor which has a high capacitance per unit area. So, capacitors are designed using back-end metal in the form of multilayer sandwich capacitors. Since the standard metal sandwich capacitor available in digital CMOS has a low capacitance density, the chip area occupied by capacitors required in RF/analog CMOS circuits can be quite large. Gate-oxide-based MOS capacitors can provide higher capacitance densities, however, these capacitors are nonlinear and voltage dependent. Moreover, their oxides are susceptible to breakdown. To reduce die area, we have used a multilayer horseshoe capacitor structure for all the on-chip capacitors [12]. This structure provides a capacitance density of 0.52 fF/μm^2 which is 2.3 times the capacitance density of the conventional multilayer metal capacitor available in the process. Top and side view diagrams of this capacitor structure are shown in Fig. 5 where the gray and black colors indicate the two nodes of the capacitor. Each horseshoe structure has lateral capacitance in the two dimensions in the horizontal plane with its adjacent horseshoes, and parallel plate capacitance in the vertical dimension with its top and bottom horseshoes. The opening in each horseshoe allows the via connections to be made for the other horseshoes, which are above or below it and are connected to the other node. The measured quality factor at 2.45 GHz is better than 30 with a resonance frequency beyond 20 GHz.

A comprehensive in-house RF model, which complements MOS Model 9, is used for the transistors. All the high-frequency parasitics are accounted for in the simulation. Fig. 6 shows the simulated output power, gain, and PAE of the two-stage self-biased cascode PA versus input power at 2.4 GHz and a supply voltage of 2.4 V. The small-signal gain is 39 dB. The maximum output power is 24.5 dBm with a gain of 31 dB and a PAE of 49%. Fig. 7 shows the maximum drain–gate voltages V_{DG} of transistors M1 to M4 versus output power. In transistors M1 and M2 of the first stage, V_{DG} is less than 1.6 V through the entire output power range. V_{DG} of transistors

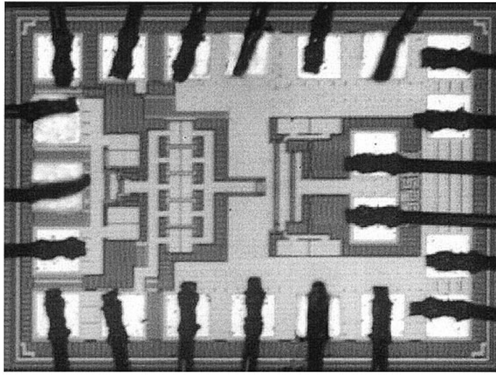

Fig. 9. Microphotograph of the PA.

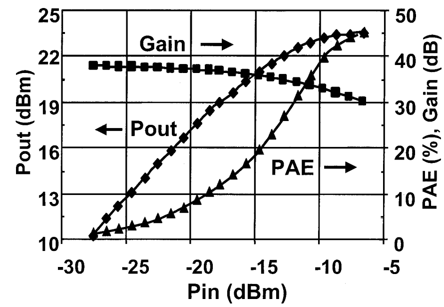

Fig. 10. Measured P_{out}, gain, and PAE versus P_{in}.

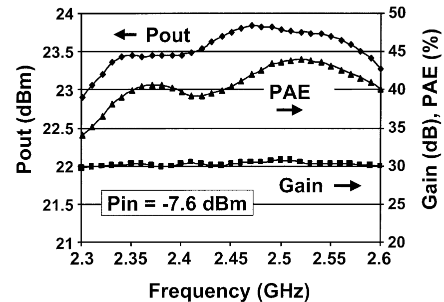

Fig. 11. Measured P_{out}, gain, and PAE versus frequency for input power of -7.6 dBm.

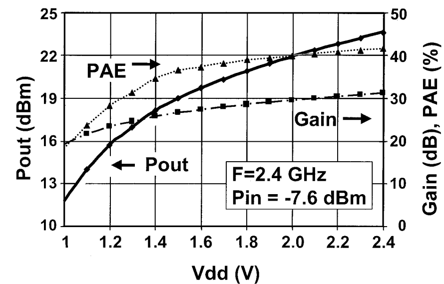

Fig. 12. Measured P_{out}, gain, and PAE versus the supply voltage for input power of -7.6 dBm at a frequency of 2.4 GHz.

M3 and M4 in the second stage have close values and are less than 2.6 V for all output powers. In order to show the effectiveness of the self-biased cascode, we have simulated the two-stage PA with a conventional bias [as shown in Fig. 1(a)]. The drain–gate voltages versus the output power are shown in Fig. 8. In this case, transistors M2 and M4 have a constant gate bias equal to V_{dd}. It is clear from Fig. 8 that transistor M4 is the bottleneck for hot electron degradation. Its V_{DG} reaches 3.2 V at maximum output power, while M3 has a much smaller V_{DG} of 2.2 V. If we want to observe a maximum V_{DG} of 2.6 V, the output power must be less than 22.5 dBm (see Fig. 8). This simulation shows that for the same maximum V_{DG} limit, the self-biased cascode configuration provides 2-dB larger output power compared with a conventional cascode configuration.

IV. Measurements

The PA was fabricated in a five-metal-layer 0.18-μm CMOS process.[4] The nMOS transistor in this process has a cutoff frequency of 60 GHz and a threshold voltage of 0.4 V. The die microphotograph is shown in Fig. 9. The die, which occupies an area of 0.81 mm by 0.57 mm, was mounted chip-on-board on FR4 PCB. We have used two bondpads to ground the source of the first stage which results in an inductance of about 0.4 nH. Since it is more critical to have a low ground inductance at the second stage, we have used ten bondpads for down bonds providing an inductance of about 0.1 nH. The two stages have separate grounds to avoid feedback from second stage to first stage. The bondpads were especially developed for RF applications and have a quality factor of more than 300 at 2.4 GHz [13].[5]

Large-signal load pull measurements at 2.4 GHz revealed the optimum load to be similar to what has been simulated. The measured optimum load had a gamma of 0.66 which is close to the gamma of the simulated 12-Ω output impedance ($\Gamma = 0.62$). A reasonable performance was measured for loads with gamma of 0.6–0.8. Considering the loss in the PCB, this translates to impedances of about 12 to 7 Ω at the drain of the output cascode transistor. The PA with both input and output matched to 50-Ω loads (as shown in Fig. 4) was tested under a continuous-wave (CW) input at 2.4 GHz and a supply voltage of 2.4 V. As seen in Fig. 10, the small-signal gain is 38 dB, and the large-signal gain close to saturation is greater than 31 dB. The amplifier provides 23.5 dBm of output power with a PAE of 45%. During this test, the bias voltages were chosen as $V_{\mathrm{G}}1 = 0.55$ V and $V_{\mathrm{G}}2 = 0.8$ V resulting in dc currents of 29 and 217 mA for the first and second stages, respectively.

We also measured the performance of the PA as a function of the frequency for an input power of -7.6 dBm. Fig. 11 shows that the gain of the prototype remains almost flat over the Bluetooth band, which is from 2.402 GHz to 2.48 GHz. The minimum PAE is 38% while the P_{out} is above 23.5 dBm for the entire Bluetooth band, thereby fulfilling the 20-dBm output power requirement. Fig. 12 shows the measured output power, gain, and PAE as a function of the supply voltage for a fixed input power of -7.6 dBm. At the supply voltage of 1.8 V, an output power of 21 dBm with 28.6-dB gain and 39% PAE is achieved, thereby still fulfilling the Bluetooth output power requirements.

[4]The circuit was fabricated in both a standard CMOS process with a low-resistivity (10 m$\Omega \cdot$ cm) substrate and a high-resistivity (10 $\Omega \cdot$ cm) variant of that. The measurements showed negligible difference in performance between the two, mainly because no on-chip inductors were used.

[5]The bondpads did not include electrostatic discharge protection; this remains an issue for this kind of application.

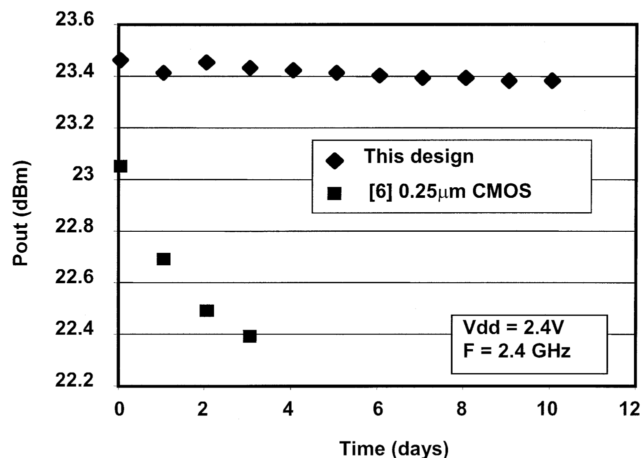

Fig. 13. $P_{\rm out}$ versus time of continuous operation for this design and the design given in [10].

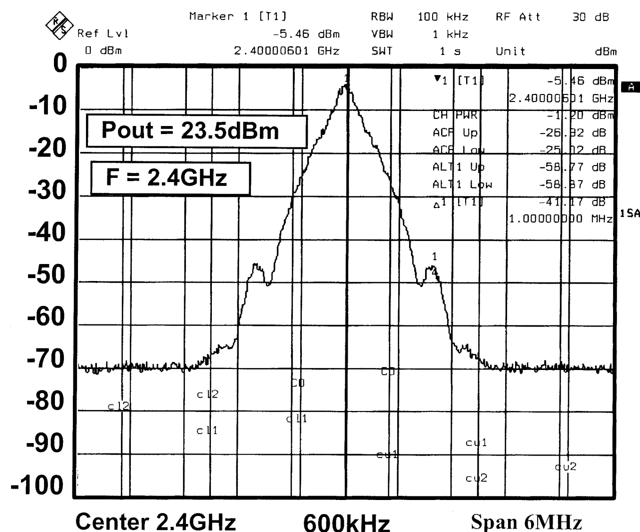

Fig. 14. Bluetooth spectrum at the output of the PA ($P_{\rm out} = 23.5$ dBm, $V_{\rm dd} = 2.4$ V).

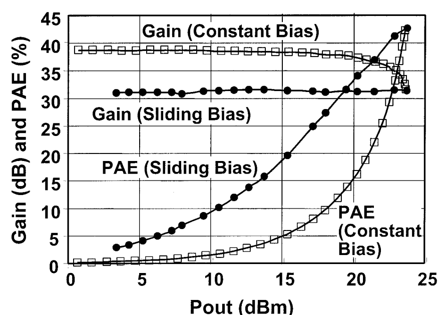

Fig. 15. Measured Gain and PAE versus Pout for constant/sliding gate bias voltages.

The important question is whether the PA is robust against breakdown and hot carrier effects. The restriction on maximum supply voltage, 1.8 V, and the transistor's breakdown voltage, 4 V, are stringent. In a conventional PA design, the hot carrier degradation prohibits the use of a common-source output stage with a supply voltage higher than 1.5 V. However, the self-biased cascode design reduces the maximum drain–gate voltage across each transistor. We let the PA operate continuously for ten days at 2.4-V supply while providing 23-dBm output power. The PA, as seen in Fig. 13, showed no sign of hot carrier degradation, whereas in [6], hot carrier degradation was seen during the first 24 h. This confirms the effectiveness of the self-biased cascode design.[6]

Finally, a Bluetooth signal at 2.4 GHz (GFSK, m $=$ 0.32, symbol rate 1 Msymbol/s) has been applied to the input of the PA. For this particular modulation index, the frequency offset is 0.32 $\times$ 500 kHz, yielding 160 kHz. The pseudorandom bit sequence used was 15 bits long.[7] The output spectrum is shown in Fig. 14. The measured output power at 2.4 V is 23.5 dBm for a gain of 31.8 dB. The input adjacent channel power ratio for lower and upper channels (ACPR low and up) at 1 MHz are -25.3 and -27.1 dBc, respectively. The output ACPR low and ACPR up are -25 and -26.8 dBc, respectively. The Bluetooth requirement is -20 dBc at 1 MHz and -40 dBc at 3 MHz, and therefore easily met by the design. There is hardly any change in the ACPR before and after amplification. Therefore, the self-biased cascode PA faithfully amplifies the Bluetooth waveform.

V. Sliding Bias Technique

This design was primarily meant for the Bluetooth/1 standard with a GFSK modulation scheme which does not require linearity. However, Bluetooth/2 is under development and requires a linear transmit architecture due to amplitude modulation of the RF signal. To improve the linearity of a PA, one can modify the design in at least three ways. The first one is to operate the PA in class-A/AB mode over the entire power range at the cost of a decrease in PAE. The second approach is to let the PA operate over most of the power range in class-A/AB and use a bias boosting and/or gain boosting technique at the point where the PA goes into compression [14]. The third approach is to employ a de-biasing technique at low and intermediate power levels to have the same gain as at maximum power. This so-called sliding biasing technique has a major advantage in improved PAE at the cost of a decreased, but more constant, power gain. We have used this third approach to linearize our PA.

Based on simulation results, a piecewise linear analog function that could be easily realized in CMOS was chosen for sliding the bias as a function of input power. The bias voltages were then manually changed according to this function. The measurement in Fig. 15 demonstrates that by varying the gate bias voltage of both stages as a function of the input signal, both AM-to-AM and AM-to-PM conversions are reduced. The gain variation over the output power range is reduced from 7 dB to less than 0.6 dB. The efficiency is greatly improved; at an output power of 16 dBm the PAE increases from 6% to 19%. In Fig. 16, the measured phase variations as a function of input power for both the fixed bias and the sliding bias are shown. As can be seen, the sliding bias reduces the phase variation from 20° to 10°. Therefore, the sliding bias technique can be used

[6]The device has not been tested for reliability under severe mismatch conditions.

[7]A sequence of 23 bits results in the same performance, however, the time variation in the spectrum is larger due to a longer sequence.

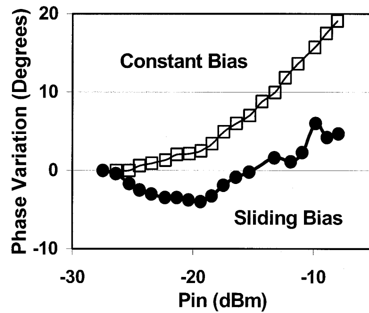

Fig. 16. Measured phase variations versus inputs power for constant/sliding bias.

for linearization of PAs with the added benefit of increasing PAE significantly at low/mid-power levels.

VI. Conclusion

We have demonstrated the feasibility of an RF PA with 23.5-dBm output power in a 0.18-μm CMOS process technology. A self-biased cascode topology was applied to reduce hot carrier effects. An extensive hot carrier test was performed, showing that no performance degradation occurs after ten days of continuous operation under maximum output power conditions. It was demonstrated that by using a sliding biasing technique on both stages, the gain variation can be reduced drastically and the PAE at low/mid-power levels improved significantly. The PA presented in this paper fulfills the Bluetooth Class-1 requirements.

Acknowledgment

The authors would like to thank S. Mukherjee, D. Alok, R. Conrad, B. Rodriguez, V. Vathulya, S. Luo, D. McCoach, and F. Molinaro from Philips Research-USA, and P. Hooijmans and the RadioMatic team from Philips Research, the Netherlands, for their support.

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Tirdad Sowlati (S'94–M'96) was born in Tehran, Iran, in 1964. He received the B.A.Sc. (with honors) and M.A.Sc. (with honors) degrees in electrical engineering from Tehran Polytechnic University, Amir Kabir, Iran, in 1987 and 1989, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1997.

He was a contract Design Engineer with the Iranian Telecommunication Research Center in 1987 and with the Research Center, Sharif University, Tehran, from 1989 to 1990. From 1989 to 1991, he was the Microwave Laboratory Manager and a University Lecturer in Communication Circuits at the Tehran Polytechnic University. From 1992 to 1996, he designed RFICs in the Microelectronic Research Laboratory, University of Toronto. From 1996 to 1998, he was with the Video Products R&D Group, Gennum Corporation, Burlington, ON, Canada, designing analog circuits for data communication. In 1998, he joined Philips Research, Briarcliff Manor, NY, where he was a Project Leader for RFIC design in BiCMOS and deep-submicrometer CMOS. In January 2002, he joined the Wireless Communication Division of Conexant, which later became Skyworks Solutions, Inc. He is currently a Senior Principal Engineer with the RFIC Design Engineering Department, Skyworks Solutions, Irvine, CA. He holds eleven U.S. patents. His research interests include RFIC design for wireless communications and high-speed circuit design for data communication.

Domine M. W. Leenaerts (M'94–SM'96) received the Ph.D. degree in electrical engineering from Eindhoven University of Technology, Eindhoven, The Netherlands, in 1992.

From 1992 to 1999, he was with Eindhoven University of Technology as an Associate Professor with the Micro-electronic Circuit Design group. In 1995, he was a Visiting Scholar with the Department of Electrical Engineering and Computer Science, University of California, Berkeley. In 1997, he was an Invited Professor with the Technical University of Lausanne (EPFL), Lausanne, Switzerland. Since 1999, he has been a Principal Scientist with Philips Research Laboratories, Eindhoven, where he is involved in RF integrated transceivers design. He has published over 100 papers in scientific and technical journals and conference proceedings. He holds several patents. He has coauthored two books, including *Circuit Design for RF Transceivers* (Boston, MA: Kluwer, 2001). His research interests include nonlinear dynamic system theory, ADC/DAC design, and RF and microwave techniques.

Dr. Leenaerts is an IEEE Distinguished Lecturer and an Associate Editor of the IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications.