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A 2.4V, 12mW Stereo Audio D/A Converter with Double Sampling Switching

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Abstract

A 2.4V 16-bit stereo audio digital-to-analog(D/A) converter was implemented using a 0.35 um CMOS technology. The DAC utilize an interpolation filter, 1-bit 4th-order noise shaper, switched-capacitor (SC) -postfilter with double sampling switching circuit and achieves the low power, high resolution from a single 2.4V supply. The proposed double sampling capacitor switching technique of SC-postfilter is applied to improve the signal-to-noise ratio(SNR) which is limited by sampling noise depending on the capacitor value. Since the proposed technique can be implemented by adding simple switching circuit compared with previous SC-postfilter techniques, it allows smaller area and lower power consumption. The D/A converter occupies a die area of 3 mm²(2000umX1600um) and dissipates 12 mW at 44.1 KHz sampling rate with a 2.4V single supply voltage in measurement result.
Typical dynamic range and signal-to-noise,distortion ratio(SNDR) are 95 dB and 88dB, respectively.

I. Introduction

The power consumption is the most important thing in the portable audio equipments such as portable CD, MD players. Multi-bit and double sampling sigma-delta D/A converter has been reported for low power consumption and high resolution[1-3]. Multi-bit sigma-delta takes an advantage of lowering the over-sampling ratio(OSR) but it must be calibrated for multi-bit linearity problem. Some calibration techniques like dynamic element matching method improved the multi-bit linearity characteristic. But it does less effective for chip area and circuit complexity because of the calibration circuits and increase of capacitive load while decreasing the OSR. The sigma-delta D/A converter in this paper uses a traditional 64OSR 1bit 4th-order sigma-delta noise shaper to achieve high resolution and it does not require calibration when D/A processing. This paper presents a double sampling switching technique of the SC-postfilter to implement low power high resolution sigma-delta D/A converters. This technique reduces the sampling noise(kT/C) by half, so it improves power consumption of D/A converter, keeping high resolution. The high resolution D/A converter using the proposed technique can be implemented with small chip area and low power.

II. Sigma-Delta Architecture

Fig. 1 shows a sigma-delta D/A converter. The input resolution is 16-bits. The sample rate(fs) is 44.1kHz. The fs rate allows serial multiplication of the coefficients in the half-band filter enabling both FIR filter functions for both channels to be served by a single engine at 128fs rate. A simple zero order hold register provides the final 16x interpolation. The interpolator passband ripple is ±0.0072dB. The stopband attenuation is 62.7dB. The analog circuits of the two channels are separated and the RC-LPF convert the SC-Postfilter differential output to single-ended.

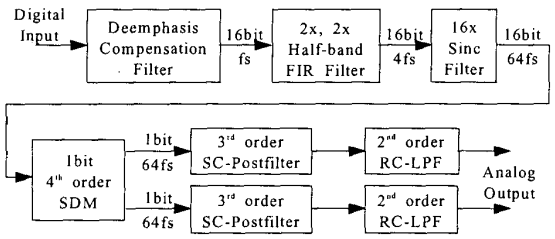

Fig. 1. Stereo Audio DAC Block Diagram.

The digital sigma-delta modulator(SDM) is illustrated in Fig. 2. A local loop with coefficient -g gives a

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quantization noise zero near 20kHz, a good trade-off between passband and out-of-band noise. The passband quantization noise is -98dB, allowing the entire noise budget to be allocated to the analog circuits. Out-of-band noise with post-filtering is -70dB.

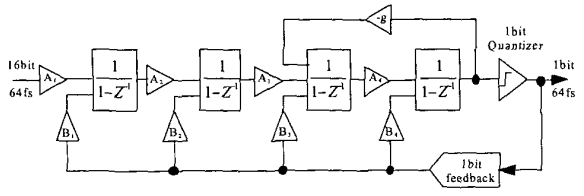


Fig. 2. 1bit 4th-order Sigma-Delta Modulator

III. Proposed the SC-Postfilter with Double Sampling

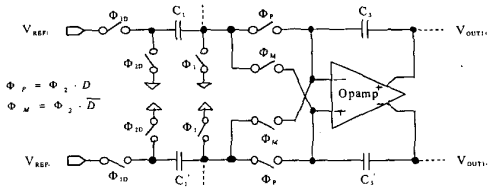
Quantization noise is sufficiently low by 64OSR 4th-order noise shaper, so the rest of noise sources located in the analog circuit and mixed environment. The noise sources are sampling noise(kT/C), thermal noise, flick noise($1/f$) and clock feed-through, substrate clock noise, etc. The kT/C noise is most dominant factor because an increase of capacitor size to reduce kT/C noise requires a corresponding increase of power.

In Fig. 3, $V_{OUT}=V_{OUT+}-V_{OUT-}$, $V_{REF}=V_{REF+}-V_{REF-}$, $C_1=C_1'$, $C_3=C_3'$ and D is 1bit output data from digital sigma-delta modulator, it was synchronized with Φ_1 phase. The integrator output was represented by Eq. (1) and (2). The single sampling case is Eq.(1) and Eq.(2) is for double sampling switching technique.

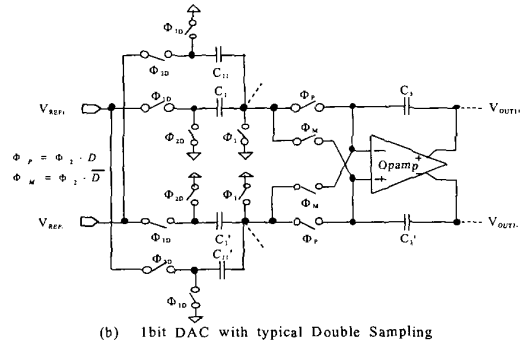
$$V_{OUT(N)} = V_{OUT(N-1)} \pm \frac{C_1}{C_3} V_{REF} \quad (1)$$

$$V_{OUT(N)} = V_{OUT(N-1)} \pm 2\frac{C_1}{C_3} V_{REF} \quad (2)$$

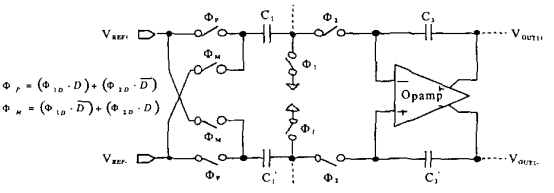
Eq. (2) shows that integrator output change is double than typical case. So double sampling switching technique makes 2-times smaller sampling capacitor for the same charge transfer. Generally integration capacitor is much bigger than sampling capacitor. The capacitor loads of opamp are sampling capacitors and bottom plate stray capacitors and input stray capacitor of opamp.



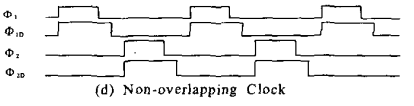
(a) Typical 1bit DAC with single sampling



(b) 1bit DAC with typical Double Sampling



(c) 1bit DAC with Double Sampling in this paper



(d) Non-overlapping Clock

Fig. 3. Sampling Technique in SC-Postfiler

The proposed double sampling technique is implemented by adding the switch without another sampling capacitor for the rest half phase. So it sampled twice with same capacitor at each half phase and it has no gain errors according to different paths in the conventional double sampling circuit with two capacitors like Fig. 3 (b). And it employs staggered clocking. In other words, while one stage is in the hold mode, both the previous and next stages are sampling with the advantages of minimizing the folding noise like *sin x/x* function when resampling the previous stage output[4].

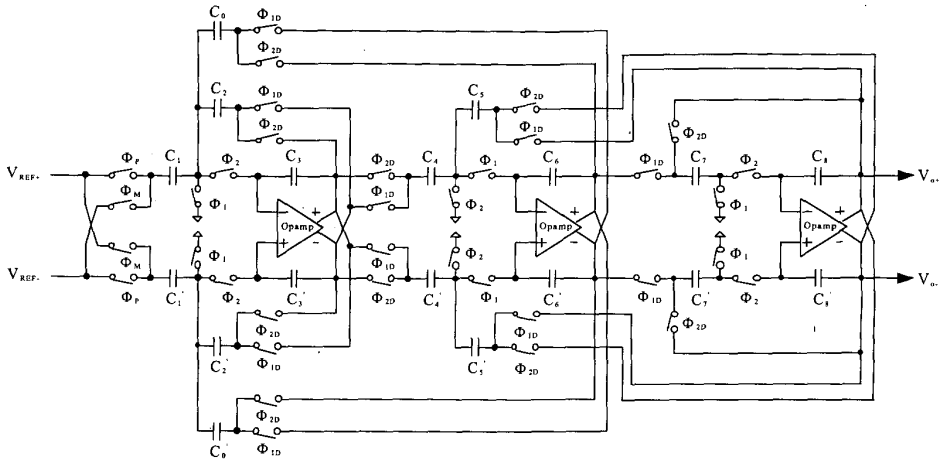


Fig. 4. The Proposed SC-Postfiler with Double Sampling Switching Technique

Fig. 4 shows proposed a novel SC-Postfilter with double sampling switching technique. The sampling rate is 2.8224MHz. The signal tranfer function is given in Eq.(3). Its coefficients are optimized to minimize phase error in passband less than 0.35 degree.

$$H(z)=\frac{4a_1a_2a_3z^{-1}}{1+\left(\frac{4a_2b_1r_3+2a_3b_2r_0-r_0-2r_3}{r_0r_3}\right)z^{-1}+\left(\frac{-4a_2b_1-2a_1b_2r_{0b}+2+r_{0b}r_3}{r_0r_3}\right)z^{-2}-\frac{r_{0b}}{r_0r_3}z^{-3}}$$

$$a_1=\frac{C_1}{C_3},a_2=\frac{C_4}{C_6},a_3=\frac{C_7}{C_8},b_1=\frac{C_2}{C_3},b_2=\frac{C_5}{C_6},b_0=\frac{C_0}{C_3}$$

$$r_0=1+b_0,r_{0b}=1-b_0,r_3=1+a_3 \qquad (3)$$

Φ_P, Φ_M clocks are generated by 1-bit stream data. Its 1-bit D/A conversion operation is done by bottom plate switching with some logical operation. This removes the crossing switches at virtual ground of the first opamp for 1-bit D/A conversion. So it takes an advantage of excluding different clock feedthrough noise distortion when polarity switches are changed by 1-bit input. Fig. 5 shows input equivalent noise transfer function of each stage. Only the first stage has a positive noise gain of 5.5dB while both second and third stages exhibit negative values. Therefore the first stage noise like *kT/C* noise and opamp's thermal noise are most important. However *1/f* noise of opamp is not dominant in simulation. A novel SC-Postfilter in this paper adopts double sampling switching technique which reduces *kT/C* noise without the penalty of larger capacitor and power consumption in the first and second stages. And the third stage utilize switched capacitor buffer to reduce the distortion of opamp's slewing limit when the signal is filtered in continuous-time by 2nd-order RC-LPF.

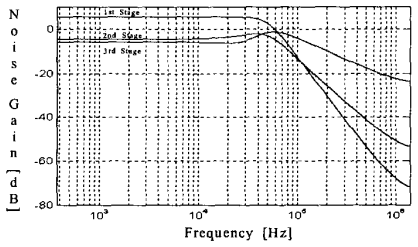


Fig 5. Each stage noise gains in proposed SC-Postfilter

The SC-Postfilter opamp is described in Fig. 6. Two-stage design with a folded-cascode first stage supports a large signal swing and a large dc gain at 2.4V operation. The self bias cascode load takes advantage of the significant short channel effect in sub-micron process[5]. Compared to M1, M2 has 4x shorter channel length, and smaller saturation voltage due to larger W/L ratio. The opamp dc gain is 110dB and operate in the wide supply range from 2.2V to 3.6V.

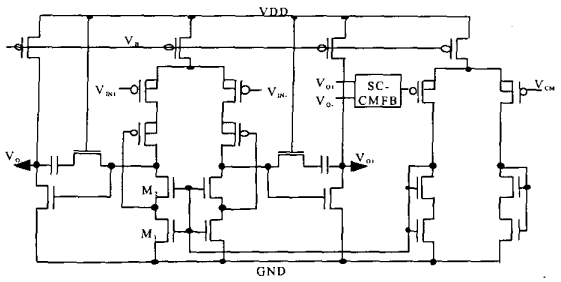


Fig 6. Fully differential Opamp with self-bias cascode load in SC-Postfilter

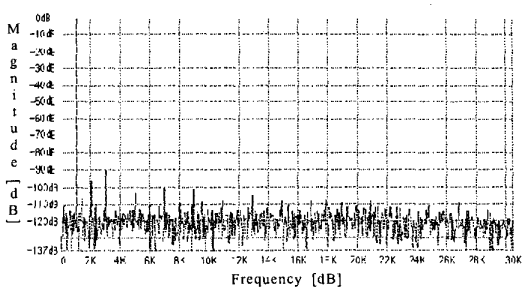


Fig 7. Measured Output FFT spectrum for 1kHz, 0dB

IV. Experimental Results

The measured performances of the prototype are summarized in Table I. A 4096-point FFT spectrum of 1kHz, 0dB signal is shown in Fig. 7. Fig. 8 shows S/(N+D) vs. input level of 1kHz signal. The power consumption is 12 mW at a 44.1kHz sampling rate with a 2.4 V single supply.

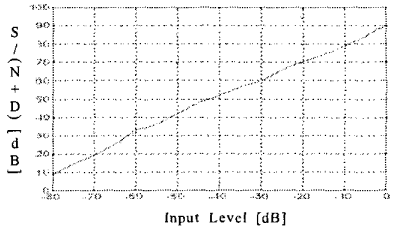


Fig 8. Measured S/(N+D) vs. Input Level for 1kHz

Table I. Summary of measurement results.

Resolution	16-bit
Power Supply	2.4V
Clock Rate	44.1kHz
Power Consumption	12mW
Dynamic Range	95dB (1kHz, -60dB)
SNR	96dB (1kHz, 0dB)
THD	89dB (1kHz, 0dB)

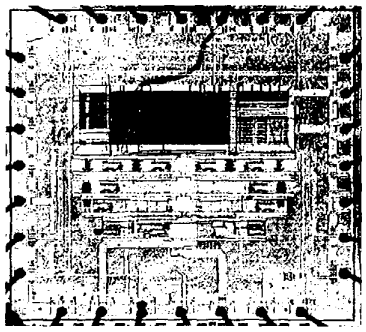


Fig. 9. Chip photography of the D/A converter

V. Conclusion

A 2.4V 16-bit stereo audio D/A converter was implemented with a novel SC-Postfilter of double sampling switching technique to improve the performance of the D/A converter. The proposed technique has advantages of smaller chip area and power consumption and higher resolution compared with the conventional sigma-delta D/A converters by employing calibration technique and others.

The proposed D/A converter was fabricated in 0.35um CMOS process, and the chip photograph is illustrated in Fig. 9. The chip area excluding pads is $3mm^2$(2000umX1600um).

Reference

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[4] J. H. Fischer, "Noise Sources and Calculation Techniques for Switched Capacitor Filters," *IEEE J. Solid-State Circuits*, vol. SC-17, No.4, Aug. 1982.

[5] Castello, R. et al., "A 500-nA Sixth-Order Bandpass SC Filter,," *IEEE J. Solid-State Circuits*, vol. 25, no. 3, pp.669-676, Jun. 1990.