JEDEC STANDARD

Stress-Test-Driven Qualification of Integrated Circuits

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STRESS DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS

(From JEDEC Board Ballot, JCB-07-81, JCB-07-91, and JCB-09-15, formulated under the cognizance of the JC14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This standard describes a baseline set of acceptance tests for use in qualifying electronic components as new products, a product family, or as products in a process which is being changed.

These tests are capable of stimulating and precipitating semiconductor device and packaging failures. The objective is to precipitate failures in an accelerated manner compared to use conditions. Failure Rate projections usually require larger sample sizes than are called out in qualification testing. For guidance on projecting failure rates, refer to JESD85 Methods for Calculating Failure Rates in Units of FITs. This qualification standard is not aimed at extreme use conditions such as military applications, automotive under-the-hood applications, or uncontrolled avionics environments, nor does it address 2nd level reliability considerations, which are addressed in JEP150.

This set of tests should not be used indiscriminately. Each qualification project should be examined for:

a) Any potential new and unique failure mechanisms.
b) Any situations where these tests/conditions may induce invalid or overstress failures.

If it is known or suspected that failures either are due to new mechanisms or are uniquely induced by the severity of the test conditions, then the application of the test condition as stated is not recommended. Alternatively, new mechanisms or uniquely problematic stress levels should be addressed by building an understanding of the mechanism and its behavior with respect to accelerated stress conditions (Ref. JESD91, “Method for Developing Acceleration Models for Electronic Component Failure Mechanisms” and JESD94, “Application Specific Qualification using Knowledge Based Test Methodology”).

Where use conditions are established, qualification testing tailored to meet those specific requirements optimizes resources and is the preferred approach to this default standard (Ref. JESD94).

Consideration of assembly-level effects may also be necessary. For guidance on this, refer to JEP150, Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components.

This document does not relieve the supplier of the responsibility to assure that a product meets the complete set of its requirements.

2 Reference documents

The revision of the referenced documents shall be that which is in effect on the date of the qualification plan.

2.1 Military

MIL-STD-883, *Test Methods and Procedures for Microelectronics*

MIL-PRF 38535

2.2 Industrial

UL94, *Tests for Flammability of Plastic Materials for Parts in Devices and Appliances.*

ASTM D2863, *Flammability of Plastic Using the Oxygen Index Method.*

IEC Publication 695, *Fire Hazard Testing.*

J-STD-020, Joint IPC/JEDEC Standard, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Devices*.

JP-001, *Foundry Process Qualification Guidelines (Wafer Fabrication Manufacturing Sites).*

JESD22 Series, *Reliability Test Methods for Packaged Devices*

JESD46, *Guidelines for User Notification of Product/process Changes by Semiconductor Suppliers.*

JESD69, *Information Requirements for the Qualification of Silicon Devices*.

JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components*.

JESD78, *IC Latch-Up Test*.

JESD85, *Methods for Calculating Failure Rates in Units of FITs*.

JESD86, *Electrical Parameters Assessment*.

JESD94, *Application Specific Qualification using Knowledge Based Test Methodology*.

JESD91, *Methods for Developing Acceleration Models for Electronic Component Failure Mechanisms*.

JEP122, *Failure Mechanisms and Models for Semiconductor Devices*.

JEP143, *Solid State Reliability Assessment Qualification Methodologies.*

JEP150, *Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components.*

JESD201, *Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy SurfaceFinishes*

JESD22A121, *Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes*

3 General requirements

3.1 Objective

The objective of this procedure is to ensure that the device to be qualified meets a generally accepted set of stress test driven qualification requirements. Qualification is aimed at components used in commercial or industrial operating environments.

3.2 Qualification family

While this specification may be used to qualify an individual component, it is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs. Interactive effects of the silicon and package shall be considered in applying family designations.

3.3 Lot requirements

Test samples shall comprise representative samples from the qualification family. Manufacturing variability and its impact on reliability shall be assessed. Where applicable the test samples will be composed of approximately equal numbers from at least three (3) nonconsecutive lots. Other appropriate means may be used to evaluate manufacturing variability. Sample size and pass/fail requirements are listed in Tables 1-3. Tables A and B give guidance on translating pass/fail requirements to larger sample sizes.

Generic data and larger sample sizes may be employed based upon a Chi Squared distribution using a total percent defective at a 90% confidence limit for the total required lot and sample size. ELFR requirements shall be assessed at a 60% confidence level as shown in Table B. If a single unique and expensive component is to be qualified, a reduced sample size qualification may be performed using 1/3 the sample size listed in the qualification tables.

3.4 Production requirements

All test samples shall be fabricated and assembled in the same production site and with the same production process for which the device and qualification family will be manufactured in production. Samples need to be processed through the full production process including burn-in, handling, test, and screening.

3.5 Reusability of test samples

Devices that have been used for nondestructive qualification tests may be used to populate other qualification tests. Devices that have been used in destructive qualification tests may not be used in subsequent qualification stresses except for engineering analysis. Non-destructive qualification tests are: Early Life Failure Rate, Electrical Parameters Assessment, External Visual, System Soft Error, and Physical Dimensions.

3.6 Definition of electrical test failure after stressing

Post-stress electrical failures are defined as those devices not meeting the individual device specification or other criteria specific to the environmental stress. If the cause of failure is due to causes unrelated to the test conditions, the failure shall be discounted.

3.7 Required stress tests for qualification

Tables 1, 2, and 3 list the qualification requirements for new components. Tables 2 and 3 are differentiated by package type, but these are not exclusively packaging tests. Interactive effects of the packaging on the silicon also drive the need for tests in Tables 2 and 3. Power supply voltage for biased reliability stresses should be Vccmax or Vddmax as defined in the device datasheet as the maximum specified power supply operating voltage, usually the maximum power supply voltage is 5% to 10% higher than the nominal voltage. Some tests such as HTOL may allow for higher voltages to gain additional acceleration of stress time. JEP122 can provide guidance for accelerating common failure mechanisms.

Table 4 lists the required stresses for a qualification family or category of change. Interactive effects from the unchanged aspects of both the silicon and packaging must be assessed.

3.8 Pass/Fail criteria

Passing all appropriate qualification tests specified in Tables 1 through 3, either by performing the test, showing equivalent data with a larger sample size, or demonstrating acceptable generic data (using an equivalent total percent defective at a 90% confidence limit for the total required lot and sample size), qualifies the device per this document. When submitting test data from generic products or larger sample sizes to satisfy the Tables 1-3 qualification requirements of this document, the number of samples and the total number of defective devices occurring during those tests must satisfy 90% confidence level of a Poisson exponential binomial distribution as defined in MIL-PRF 38535. MIL-PRF 38535 is available for free from http://www.dscc.dla.mil/Programs/MilSpec/listdocs.asp?BasicDoc=MIL-PRF-38535. The minimum number or samples for a given defect level can be approximated by the formula:

$$N >= 0.5\ [\chi^2\ (2C+2,\ 0.1)]\ [1/LTPD - 0.5] + C$$

where C = accept #, N=Minimum Sample Size, χ^2 is the Chi Squared distribution value for a 90% CL, and LTPD is the desired 90% confidence defect level. Table A is based upon this formula, but in some cases the sample sizes are slightly smaller than MIL-PRF-38535.

3.8 Pass/Fail criteria (cont'd)

Table A — Sample Size for a Maximum % Defective at a 90% Confidence Level

Acceptance Number C	LTPD 10	LTPD 7	LTPD 5	LTPD 3	LTPD 2	LTPD 1.5	LTPD 1
0	22	32	45	76	114	153	230
1	38	55	77	129	194	259	389
2	53	76	106	177	266	355	532
3	67	96	134	223	334	446	668
4	80	115	160	267	400	533	800
5	94	133	186	310	465	619	928
6	107	152	212	352	528	703	1054
7	119	170	237	394	590	786	1179
8	132	188	262	435	652	868	1301
9	144	205	287	476	713	949	1423
10	157	223	311	516	773	1030	1543
11	169	240	335	556	833	1110	1663
12	181	258	359	596	893	1189	1782

EXAMPLE: Using generic data for HTOL with a requirement of 0 rejects from 230 samples. If 700 samples of generic data are available, the maximum number of failures that will meet the qualification test requirement is 3 failures from the LTPD=1 column.

4 Qualification and requalification

4.1 Qualification of a new device

New or redesigned products (die revisions) manufactured in a currently qualified qualification family may be qualified using one (1) wafer/assembly lot. Electrical parameter assessment is one of the most important tests to run.

4.2 Requalification of a changed device

Requalification of a device will be required when the supplier makes a change to the product and/or process that could potentially impact the form, fit, function, quality and/or reliability of the device. The guidelines for requalification tests required are listed in Table 4.

4.2.1 Process change notification

Supplier will meet the requirements of JESD46 "Guidelines for User Notification of Product/Process Changes by Semiconductor Suppliers" for product/process notification changes.

4.2.2 Changes requiring requalification

All product/process changes should be evaluated against the guidelines listed in Table 4.

4.2 Requalification of a changed device (cont'd)

4.2.3 Criteria for passing requalification

Table 4 lists qualification plan guidelines for performing the appropriate Table 1-3 stresses. Failed devices should be analyzed for root cause and correction; only a representative sample needs to be analyzed. Acceptable resolution of root cause and successful demonstration of corrective and preventive actions will constitute successful requalification of the device(s) affected by the change. The part and/or the qualification family can be qualified as long as containment of the problem is demonstrated until corrective and preventive actions are in place.

5 Qualification tests

5.1 General tests

Test details are given in Tables 1 through 3. Not all tests apply to all devices. Table 1 tests generally apply to design and fabrication process changes. Table 2 tests are for non-hermetic packaged devices, and Table 3 is for hermetic packaged devices. Table B lists the pass/fail requirements for common infant mortality levels. Table 4 gives guidance as to which tests are required for a given process change. Some of the data required may be substituted by generic process or package data.

5.2 Device specific tests

The following tests must be performed on the specific device to be qualified for all hermetic and organic packages . Passing or failing these tests qualifies or disqualifies only the device under qualification and not the associated qualification family:

1) Electrostatic Discharge (ESD) - All products - See Table 1.
2) Latch-up (LU) – Required for CMOS, BiCMOS, and Bipolar technologies. See Table 1.
3) Electrical Parameters Assessment - The supplier shall be capable of demonstrating, over the application temperature range, that the part is capable of meeting parametric limits in the individual device specification or data sheet.

5.3 Wearout reliability tests

Qualification family testing for the failure mechanisms listed below must be available upon request when a new wafer fabrication technology or a material relevant to the appropriate wearout failure mechanism is to be qualified. JP001 lists requirements for Fabrication Process Qualification. JEP122 explains how to project wearout lifetime for these failure mechanisms. The following mechanisms need to be considered, but there may be other mechanisms to consider based upon technology details.

- Electromigration; EM
- Time-Dependent Dielectric Breakdown; TDDB or Gate Oxide Integrity Test such as Charge to Breakdown.
- Hot Carrier Injection; HCI
- Negative Bias Temperature Instability; NBTI
- Stress Migration; SM, may be performed on an actual product.

The data, test method, calculations, and internal criteria need not be demonstrated or performed on the qualification of every new device.

5.4 Flammability/oxygen index

Certificates of compliance to UL94-0 or ASTM D2863 must be available upon request.

5.5 Device qualification requirements

Table 1 — Device qualification tests

Stress	Ref.	Abbv.	Conditions	Requirements	
				# Lots / SS per lot	Duration / Accept
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	Tj ≥ 125 °C Vcc ≥ Vccmax	3 Lots / 77 units	1000 hrs / 0 Fail
Early Life Failure Rate	JESD22-A108, JESD74	ELFR	Tj ≥ 125 °C Vcc ≥ Vccmax	See ELFR Table	48 ≤ t ≤ 168 hrs
Low Temperature Operating Life	JESD22-A108	LTOL	Tj ≤ 50 °C Vcc ≥ Vccmax	1 Lot / 32 units	1000 hrs / 0 Fail
High Temperature Storage Life	JESD22-A103	HTSL	Ta ≥ 150 °C	3 Lots / 25 units	1000 hrs / 0 Fail
Non-Volatile Memory Cycling Endurance	JESD22-A117	NVCE	25 °C and 85°C ≥Tj ≥ 55 °C	3 Lots / 77 units	Up to Spec. Max Cycles per note (e) / 0 Fails
Data Retention for Non-Volatile Memory: High Temperature	JESD22-A117	HTDR	Option 1: Tj = 100 °C	3 Lots / 39 units	Cycles per NVCE (≥55 °C) / 96 and 1000 hrs / 0 Fail / note (f)
			Option 2: Tj ≥ 125 °C		Cycles per NVCE (≥55 °C) / 10 and 100 hrs / 0 Fail / note (f)
Non-Volatile Memory Low-Temperature Retention and Read Disturb	JESD22-A117	LTDR	Ta = 25 °C	3 Lots / 38 units	Cycles per NVCE (25 °C) / 500 hrs / 0 Fail / note (g)
Latch-Up	JESD78	LU	Ta = 25 °C and Tjmax	6 units	0 Fail
Electrical Parameter Assessment	JESD86	ED	Datasheet	3 Lots / 10 units	Ta per datasheet
Human Body Model ESD	JESD22-A114	ESD-HBM	Ta = 25 °C	3 units	Classification
Charged Device Model ESD	JESD22-C101	ESD-CDM	Ta = 25 °C	3 units	Classification
Accelerated Soft Error Testing	JESD89-2, JESD89-3	ASER	Ta = 25 °C	3 units	Classification
"OR" System Soft Error Testing	JESD89-1	SSER	Ta = 25 °C	Minimum of 1E+06 Device Hrs or 10 fails.	Classification

5.5 Device qualification requirements (cont'd)

a) **HTOL-** The duration listed here is generally acceptable to qualify for the given Application Level. However, it does not necessarily imply the demonstration of the lifetime requirement for a particular use condition. It depends on failure mechanisms and application environments. For example, with apparent activation energy of 0.7 eV, 125 °C stress temperature and 55 °C use temperature, the acceleration factor (Arrhenius equation) is 78.6. This means 1000h stress duration is equivalent to 9 years of use. This might be shorter than the application requirement. In order to assure adequate lifetime requirement, it would be necessary to include Wafer Level Reliability Test information. Wafer Level Reliability can provide information about long term or intrinsic reliability of specific wearout mechanisms, the onset to failure time and design rule (e.g. maximum current density). For many failure mechanisms, such as dielectric breakdown, elevated voltage will provide additional acceleration and can be used to increase effective device hours or achieve an equivalent life point with a shorter stress duration. Refer to JEP122 for voltage acceleration models.

b) **ELFR -** Several methods can be used to calculate the Early Life Failure Rate (ref. JESD74). The objective of ELFR is to measure the failure rate in the first several months or year of operation. Knowledge of the life distribution is generally required to accurately predict ELFR. Equivalently, Table B can be used to determine sample sizes to satisfy a particular FPM (cumulative failures) target. Voltage and temperature acceleration may be used to further accelerate effective unit hours.

c) **LTOL –** This requirement is aimed at Hot Carrier Degradation and may be satisfied by appropriate wafer level data as specified in JP-001. This test is particularly useful when the wafer level data cannot demonstrate adequate life. This test should be run at the maximum frequency of the device with speed parameters data logged.

d) **HTSL –** High temperature storage may be accelerated by utilizing a higher temperature; however care must be taken that new failure mechanisms are not introduced such as Kirkendal Voiding at too high a temperature or suppressing failure mechanisms such as stress migration at temperatures above 180 °C. Alternatively, this test may be performed at the wafer level if packaged device reliability has been addressed with generic data.

e) **NVCE** – See Figure A for linked flow for NVCE, HTDR, and LTDR. Half of the devices are cycled at room temperature and half at elevated temperature. Quantity of Cycling: Cycling should be performed to the max spec. cycle count on 50% of cells and to 10% of max spec. cycle count on the other 50% of cells when this is possible within 500 hours. For large memories where this would be impossible, the total program/erase operations are to be the number possible in 500 hours. This will be accomplished by reducing the fraction of cells cycled to max spec. and increasing the fraction cycled to 10% of max spec. In some cases it will be necessary to cycle some fraction of cells to less than 10% of max spec. to ensure that all cells receive some cycling. At least one-third of the operations should be devoted to cycling blocks to 100% of maximum specification. For multi-block memories, at least one block of each device must be cycled to the max. spec. cycle count, regardless of the time required. Such cycling conditions are generally acceptable also for system implementing wear leveling; otherwise, a knowledge based qualification can be implemented. Delays between Cycles: The supplier may specify that cycling not exceed a certain rate per day or that delays or bakes be inserted between cycles, to avoid overstress due to unrealistic conditions or to emulate delays expected in intended application, subject to four constraints. First, the quantity of cycling is for 500 hours of actual cycling operations, not counting inserted delays. Second, inserted delays must be distributed per the guideline in JESD22-A117. Third, for room-temperature cycling, no high-temperature delays are to be inserted. Fourth, for high-temperature cycling, the delays plus the cycling time itself must not add up to more than 500 hours at 85 °C (longer delays acceptable at lower temperatures per JESD22-A117, 4.1.2.4).

5.5 Device qualification requirements (cont'd)

These delays do not necessarily demonstrate the effect that would be seen with a particular use condition. For example, with apparent activation energy of 1.1 eV for dielectric charge detrapping, the delay durations are equivalent to 1.5 years of cycling at 55 °C. An application condition with less delay would be more severe than is represented by the qualification delays specified above. If application use conditions deviate considerably from the cycle counts or equivalent times described above, then an application-specific qualification methodology can be pursued per JESD94. For devices operated with Bad Block Management and specified to have a non-zero bad-block rate, a unit with blocks failing program/erase is to be counted as a failure if the number of such blocks exceeds the allowed bad-block specification (see JESD22-A117, 2.5). For devices specified to have some non-zero bit read error rate, bit errors are not to be counted towards device failure but must be shown to meet the bit error rate specification (see JESD22-A117, 2.8, and 5.2).

f) **HTDR** – See Figure A for linked flow for NVCE, HTDR, and LTDR. The NVCE devices cycled at elevated temperature are placed in high-temperature retention bake. Two options are given, either of which is acceptable for qualification, and for each option two bake durations. The longer of the two durations is to be applied to the blocks cycled to ≤ 10% of the max. spec. cycles. The shorter of the two is to be applied to blocks cycled to 100% of max. spec. cycles. For example option 2 requires that blocks cycled to ≤ 10% of max. spec. cycles retain data for 100 hours of 125 °C bake, and blocks cycled to 100% of max. spec. cycles must retain data for 10 hours of 125 °C bake. The durations listed are generally acceptable for qualification but do not necessarily demonstrate the retention requirement for a particular use condition, which depends on failure mechanisms and application environments. For example, with activation energy of 1.1 eV for dielectric charge detrapping, 125 °C stress temperature (option 2) and 55 °C use temperature, the acceleration factor (Arrhenius equation) is 939. Bake time is then equivalent to 11.3 years for 10% of max. spec. cycles and 1.1 years for 100% of max. spec. Retention lifetime necessary in use will be less than total product lifetime, because the HTDR requirement is a sequential reliability stress that is preceded by up to one lifetime's worth of endurance cycling (NVCE). If the application requirement does not match these retention values, or the technology has different activation energy, then a knowledge-based qualification should be followed (see JESD94). For devices specified to have some non-zero bit error rate, bit errors may not be counted towards device failure but must be shown to meet the bit error rate specification (see JESD22-A117).

g) **LTDR** – See Figure A for linked flow for NVCE, HTDR, and LTDR. The NVCE Devices cycled at room temperature are placed into room-temperature operating-life stress which sequentially performs dynamic read accesses on all memory addresses. 25 °C stress temperature is used to determine sensitivity to non-temperature-accelerated retention failure mechanisms, or to mechanisms that can entirely recover at high temperatures, such as the SILC mechanism. Biased life stress is performed to detect voltage-induced disturbs due to random bit accesses, in addition to unbiased data retention mechanisms which occur when a bit is not being accessed. Inserted bakes as described for NVCE are not acceptable for the 25 °C cycling condition used prior to LTDR. If the cycle counts from note (e) or the retention lifetimes of 500 hours are insufficient to meet a specific application requirement, or if bit accesses in application are expected to be highly concentrated on specific bits, then knowledge-based qualification methods using special techniques should be used (see JESD94). For devices specified to have some non-zero bit error rate, bit errors may not be counted towards device failure but must be shown to meet the bit error rate specification (see JESD22-A117).

h) **LU** – Verify Vcc overvoltage and I/O trigger current resistance to latch-up.

5.5 Device qualification requirements (cont'd)

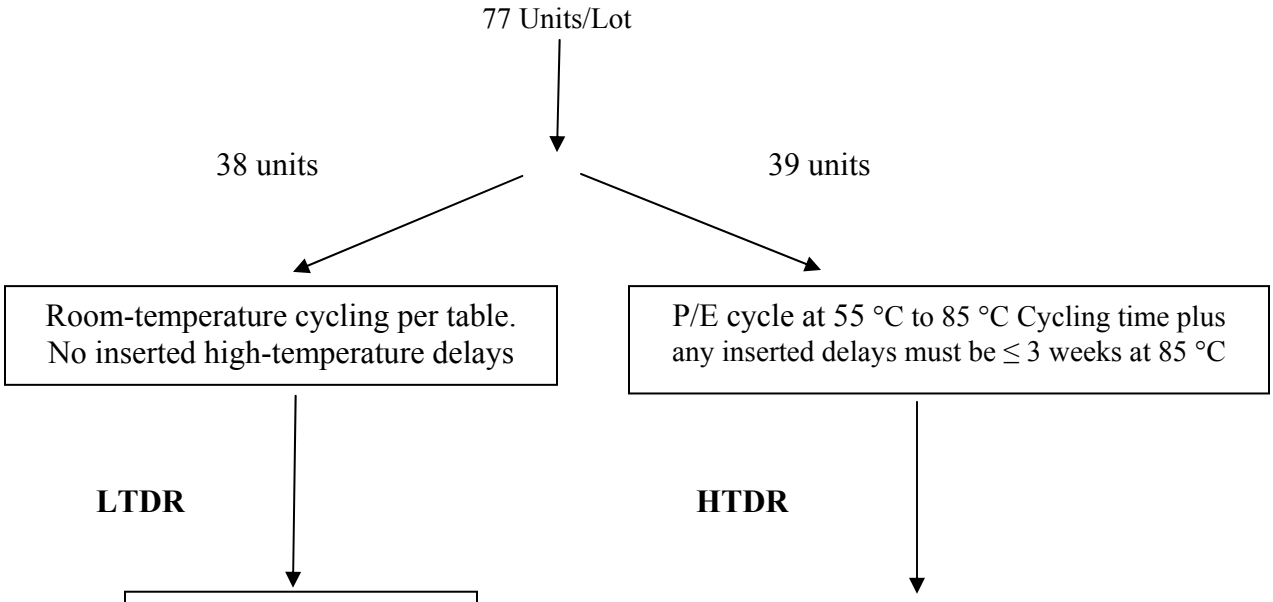
i) **ED** – This study is to be performed on key device parameters, it is not aimed at all datasheet parameters.

j) **ESD-HBM** Classification of Human body Model ESD resistance

k) **ESD-CDM** Classification of Charge Device model ESD resistance.

l) **ASER** – Accelerated alpha particle and beam soft error testing may be utilized together to project the field soft error rate. For parts without B^{10} in the process, the only beam soft error testing required is high energy neutron or proton soft error testing; thermal neutron soft error beam testing is not required for such parts. This test is required for devices with a significant portion of the circuit utilizing volatile memory elements or latches. Generic data taken on products or test devices with similar memory elements or latches and equivalent critical charge may be substituted.

m) **SSER** – System soft error testing requires enough device hours to be accumulated to produce 10 failures or at least 1E6 device hours must be accumulated. High altitude testing may be used to accelerate this stress. This test may be utilized in lieu of or in addition to accelerated soft error testing. Generic data taken on products or test devices with similar memory elements or latches and equivalent critical charge may be substituted.



Cycle Count	Option 1 100 °C	Option 2 125 °C
100% spec	96 hr	10 hr
10% spec	1000 hr	100 hr
<10% spec	1000 hr	100 hr

Figure A — NVCE/HTDR/LTDR

5.5 Device qualification requirements (cont'd)

Table B — Minimum sample size to demonstrate various ELFR targets in FPM (Failures per million) at 60% confidence level

Number of observed failures	Equivalent failures at 60% Confidence Level ($\chi^2/2$)	Minimum sample sizes required to meet FPM target at 60% confidence level					
		4000 FPM	2000 FPM	1000 FPM	500 FPM	250 FPM	100 FPM
0	0.92	229	458	916	1,833	3,665	9,163
1	2.02	505	1,011	2,022	4,045	8,089	20,223
2	3.11	778	1,553	3,105	6,211	12,422	31,054
3	4.18	1004	2,088	4,175	8,351	16,701	41,753
4	5.24	1310	2,618	5,237	10,473	20,946	52,366
5	6.29	1573	3,146	6,292	12,584	25,168	62,919
6	7.34	1835	3,671	7,343	14,685	29,371	73,426
7	8.39	2098	4,195	8,390	16,780	33,559	83,898
8	9.43	2358	4,717	9,434	18,868	37,736	94,340
9	10.48	2620	5,238	10,476	20,951	41,903	104,757
10	11.52	2800	5,758	11,515	23,031	46,061	115,153

5.6 Nonhermetic package qualification test requirements

Table 2 — Qualification tests for components in nonhermetic packages

Stress	Ref.	Abbv	Conditions	Requirements	
				# Lots / SS per lot	Duration /Accept
MSL Preconditioning Must be performed prior to: THB, HAST,TC, AC, & UHAST	JESD22 -A113	PC	Per appropriate MSL level per J-STD-020		Electrical Test (optional)
High Temperature Storage[1]	JESD22 -A103 & A113	HTSL	150 °C + Preconditioning if Required	3 Lots / 25 units	1000 hrs / 0 Fail
Temperature[2] Humidity bias (standard 85/85)	JESD22 -A101	THB	85 °C, 85 % RH, Vccmax	3 Lots / 25 units	1000 hrs / 0 Fail
Temperature[2, 3] Humidity Bias (Highly Accelerated Temperature and Humidity Stress)	JESD22 -A110	HAST	130 °C / 110 °C, 85 % RH, Vccmax	3 Lots / 25 units	96/264 hours or equivalent per package construction / 0 Fail
Temperature Cycling	JESD22 -A104	TC	*B*[4] -55 °C to +125 °C	3 Lots / 25 units	700 cycles / 0 Fail
			G[4] -40 °C to +125 °C		850 cycles / 0 Fail
			C[4] -65 °C to +150 °C		500 cycles / 0 Fail
			K[4] 0 °C to +125 °C		1500 cycles / 0 Fail
			J[4] 0 °C to +100 °C		2300 cycles / 0 Fail
Unbiased Temperature/Humidity (Unbiased HAST[3])	JESD22 -A118	UHAST	130 °C / 85% RH 110 °C / 85% RH	3 Lots / 25 units	96 hrs / 0 Fail 264 hrs / 0 Fail
Unbiased Temperature/Humidity (Autoclave[5])	JESD22 -A102	AC	121 °C / 100% RH	3 Lots / 25 units	96 hrs / 0 Fail **Not Recommended**
Solder Ball Shear	JESD22 -B117	SBS	Characterization	30 balls / 5 units	
Bond Pull Strength	M2011	BPS	Characterization, Pre Encapsulation	30 bonds / 5 units	Ppk≥1.66 or Cpk≥1.33 (note 6)
Bond Shear	JESD22 -B116	BS	Characterization, Pre Encapsulation	30 bonds / 5 units	Ppk≥1.66 or Cpk≥1.33 (note 6)
Solderability	M2003 JESD22 -B102	SD	Characterization	3 lots / 22 leads	0 Fail
Tin Whisker Acceptance	JESD22 -A121 through rqmts of JESD 201	WSR	Characterization per JESD201	See JESD 201	See JESD201, Based on Appropriate Classification

5.6 Nonhermetic package qualification test requirements (cont'd)

Notes to Table 2 — Qualification tests for components in nonhermetic packages

[1] Preconditioning to JESD22A113 is recommended, specifically for wirebonded products qualified to Pb-free reflow profiles. Moisture soak as part of the preconditioning is optional.

[2] Either HAST or THB may be chosen.

[3] If THB or HAST is run, then UHAST need not be run.

[4] It is recommended that the Temperature Cycling condition is chosen applying the following criteria:

- Condition ***G, B or C*** may not be appropriate unless the device will be subjected to a sub 0 °C cycle in its routine field operating life.
- Condition ***G, B or C*** may not be appropriate for Flip Chip packages with organic substrates.
- The condition chosen must encompass the range that device will be subjected to in its routine field operating life.
- Annex A explains the failure mechanisms and models used for the choice of temperature cycling conditions.
- Any Temperature Cycling condition specified in JESD22-A104 may be used following the methodology in Annex A.

[5] Autoclave is not recommended as a qualification test; Unbiased or biased HAST is the recommended stress and is required for organic substrates instead of Autoclave.

[6] Ppk = $\frac{\bar{x} - LSL}{3\sigma}, \frac{USL - \bar{x}}{3\sigma} \geq 1.66$. Process capability data may be substituted for Ppk with data on more than 30 lots with the requirement that $Cpk \geq 1.33$.

CONDITIONS:

A) HTSL This test is basically used to determine if the effects of diffusion, oxidation, intermetallic growth, and chemical degradation of packaging components will affect product life.

B) THB will accelerate the three basic corrosion models: Galvanic, Electrochemical and direct Chemical. It will also accelerate ion migration. Must be run at minimum power dissipation.

C) HAST is a test used to accelerate the **THB test.** Must be run at minimum power dissipation. It is suggested that 130 °C for 96 hours be used for leaded devices and 110 °C for 264 hours be used for Ball Grid Arrays.

D) TC will accelerate damage caused by thermal-mechanical stress as a result of thermal mismatch and dimensional differences.

E) UHAST is the preferred technique to test for Galvanic and direct Chemical corrosion.

F) AC (Autoclave) is the less desirable alternative to UHAST testing. It can introduce condensation and pressure induced mechanical damage that are not representative of package field life stresses. Autoclave is not recommended for organic substrate packages.

G) PC (Pre-Conditioning) ensures that a device will be able to withstand multiple assembly cycles, and to simulate the stress from Printed Circuit Board assembly that a device in a field operation would receive prior to acceleration stress testing.

H) SBS (Solder Ball Shear) ensures that the BGA balls have the desired shear strength attachment to the package.

I) BPS (Bond Pull Strength) ensures that wire bond exhibits the desired tensile strength.

J) BS (Bond Shear) ensures that the wire ball bond exhibits the desired shear strength.

K) SD (Solderability) ensures that the device leads are capable of being wetted by the board attachment solder.

L) WSR (Tin Whisker Susceptibility) for use when tin (Sn) or tin alloy surface finishes are used. This acceptance procedure provides a basis for comparison between surface finishes with respect to the propensity for whisker growth, but does not provide a basis for prediction of whisker growth in field use conditions.

5.7 Hermetic package qualification tests

These packages are typically used in long term applications and severe environments so some requirements may be different than for non-hermetic packages.

Table 3 — Qualification test for components in hermetic packages

Stress	Ref.	Abbv.	Conditions	Requirements	
				# Lots/SS per lot	Duration/Accept
Temperature Cycling	JESD22-A104	TC	-55 °C to +125 °C or alternatives with temperature justification	3 Lots / 25 units	700 cycles / 0 Fail
Bond Pull Strength [3]	M2011	BPS	Characterization	1 lot / 30 bonds / 5 units	Ppk ≥ 1.66 or Cpk ≥ 1.33
Bond Shear [3]	JESD22-B116	BS	Characterization	1 lot / 30 bonds / 5 units	Ppk ≥ 1.66 or Cpk ≥ 1.33
Solderability	M2003 JESD22-B102	SD	Characterization	3 lots / 22 leads	0
Solderball Shear	JESD22-B117	SBS	Characterization	5 units	10 balls per unit
Mechanical Shock[1]	JESD22-B104 M2002	MS	Y1 plane only, 5 pulses, 0.5 ms duration, 1500 g peak acceleration	3 lots / 39 units	TEST after CA
Vibration Variable Frequency[1]	JESD22-B103 M2007	VVF	20 Hz to 2 kHz (log variation) in > 4 minutes, 4X in each orientation, 50g peak acceleration	Sequence from MS	TEST after CA
Constant Acceleration[1]	M2001	CA	Y1 plane only, 30 kg force <40 pin packages, 20 kg for ≥ 40 pins.	Sequence from VVF	Test at room temp. pre & post –stress
Gross /Fine Leak	JESD22-A109 M1014	GFL	Any fine test followed by gross test. May also be performed at the beginning of the mechanical sequence before mechanical shock test		
External Visual		EV			[1]
Physical Dimensions		PD		1 lot / 30 units	[2]
Lead Integrity		LI		45 leads; min of 5 units	[1]
Lid Torque		LT		1 lot / 5 units	[1]
Internal Water Vapor	MIL-STD 883 M1018	IWVC	Residual Gas Analysis of Package Cavity Water Vapor Content	3 lots / 1 unit ea.	Characterization
Tin Whisker Acceptance	JESD22-A121	WSR	Characterization per JESD201	See JESD201	See JESD201, Based on Appropriate Classification

[1] Based upon manufacturer specification or applicable procurement documents.
[2] Reference applicable JEDEC spec, supplier specification, or procurement document for significant dimensions and tolerances.
[3] $Ppk = \frac{\bar{x} - LSL}{3\sigma}, \frac{USL - \bar{x}}{3\sigma} \geq 1.66$. Process capability data may be substituted for Ppk with data on more than 30 lots with the requirement that $Cpk \geq 1.33$.

5.8 Results are to be reported in accordance with JESD69.

6 Explanatory comments regarding process/product changes

6.1 The following changes require re-qualification:

Active Circuit Element: New type of circuit element or modification of transistors beyond original qualification or spec limits.

Major Circuit Elements: Addition of a major new circuit block to an existing circuit such as adding a Digital Signal Processor or embedded memory block to an existing product.

Wafer Diameter Change

Metallization: New Materials or a significant change in composition

Change In Minimum Feature Size: A reduction of greater than 20% shall be considered a new process.

Wafer Fab Process: Utilizing different process techniques at critical points (excluding wafer transport equipment)

Diffusion/Dopant: New material or technique

Polysilicon or other MOSFET gate material: Composition, design rules, process

Lithography: Change in wavelength, method (air / immersion / ebeam), or etch technique

Wafer Frontside Metallization: Composition, design rules, process and/or technique

VIA: Composition, design rules, process and/or technique

Passivation Overcoat: Either glass or organic material composition, design rules, process and/or technique

Dielectric Materials: Composition, design rules, process and/or technique

Low-K Dielectric: A dielectric material used for inter-metal isolation with a K value less than 3.2.

Wafer Backside Operation: Metal composition, design rules, process and/or technique

New Wafer Manufacturing Line: Not already qualified for the fabrication process

Assembly Process: Utilizing different process techniques at critical points

Die Coating: Material, process, and/or technique

Lead Frame: Base material, finish, and critical dimensions

Bond Wire: Material, diameter

Bonding: Process and/or technique

Die Preparation: Separation and clean methods

Die Attach: Material, process, and/or technique

Encapsulation: Material, composition, process and/or technique

Hermetic Package: Material, composition, seal material, process and/or technique

Wafer Bumping Material: process, or technique (including flip chip assembly process)

Package Dimension Change: Larger package body size or reduction in lead or solder ball pitch.

Die Thickness

New Chip-Package Combination

6.2 Changes that may not require re-qualification:

Assembly location already qualified for that package.

The movement of product manufacturing (wafer fab or assembly) from one location to another where the new location is already qualified for the same process and techniques requires only completion of manufacturability tests at the new location.

The addition of previously qualified equipment requires completion of process capability study only, to assure that the added equipment delivers an adequate process distribution.

A change to a test program or test equipment requires proof of continued conformance to product specification only.

Any change in a process, product or material parameter that does not exceed the current specified production process range is not a major change.

Minor changes to device logic operation may only require functional verification.

Smaller package or die where the product family has already been qualified.

6.3 Multiple family qualifications

When the specific product attribute to be qualified will affect more than one wafer fab or assembly family, the qualification test vehicles should be:

1) One lot of a single device type from each of the three (3) products that are projected to be most sensitive to the changed attribute, or
2) Three lots total from the most sensitive families if only one or two exist.

Below is the recommended process for qualifying changes across many process and product families:

1) Identify all products affected by the proposed changes.
2) Identify the critical structures and interfaces potentially affected by the proposed change.
3) Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces. Note that steps 1 to 3 are equivalent to the creation of an FMEA.
4) Define the product groupings or families based upon similar characteristics as they relate to the structures and device sensitivities to be evaluated, and provide technical justification for these groupings.
5) Provide the qualification test plan, including a description of the change, the matrix of tests and the representative products that will address each of the potential failure mechanisms and associated failure modes.
6) Robust process capability must be demonstrated at each site (e.g. control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process steps.

6.4 Guidelines for stress tests for typical process changes

Table 4 lists the recommended (R) qualification tests for each type of change in the process, package, or device design, and additional tests that should be considered (C) based upon technology considerations.

Table 4 — Guidelines for major process change selection of tests

Process Attribute	HTOL	ELFR	LTOL	HTSL	NVCE+DR	LU	ED	ESD-HBM	ESD-CDM	ASER	THB/HAST	TC	UHAST	BPS	BS	SD	SBS	MS	VVF	CA	GFL	LI	LT	EM	HC	NBTI	TDDB
Active Circuit Element	C		C																						R	R	
Major Circuit Change	R		C			C	C	C	C																		
5% to 20% Die Shrink	R	R	C	C		R	R	R	R	R	R	C												C	R	R	
Lithography	C		C				R																		C	C	
Doping	C					C		C																	R	R	
Polysilicon	C				R							R													R	R	C
Metallization	C	C		R							C	R	C											R			
Gate Oxide	R	C	C		R		C																		R	R	R
Interlayer Dielectric Non low-k	C	C		C								C												R			C
Low-K Dielectric	R	C		R							R	R												R			C
Passivation	C	C			C						C	C	R														
Contact	C	C		R	C																			R			
Via	C	C		R																				R			
Wafer diameter	R		C	C	R			C	C		C	R	C												R	R	R	R
Fab site	R			R							C	R	C														
New Package to Qualified Product	C			C					C		C	R	R	R	R	R	R	R	R	R	R	R	C				
Leadframe plating[1]																R						C					
Leadframe Material												C				R			C	C		R					
Package Dimensions, including trace pitch												C	C				C		C	C	C	C					
Wire Bonding				R								R	C	R	R			C	C								
Multi-Chip Module Die Separation												R	C														
Die Attach												R	C					C	C	C							
Molding Compound	C			R							R	R															
Package Substrate Material											C	R					R	C	C	C							
Package Substrate Plating											C			R			R										
Molding Process				C								R	C														
Assembly Site											R	R		R	R	R	R	C	C	C	C	C	C				
Burn-in Elimination		R																									
Burn-in Reduction**		C																									
Flip Chip Attach Method				C							R	R															
Wafer Bump Materials or Process				C						*		R	R														
Wafer Bump Under-Metal				R						*		C	R														
Bump Site				R						*			R														
Flip Chip Underfill										*		R	R														
Die thickness	C				C							R	R														

R – Recommended
C – Consider

* - Measure material alpha emissivity
** - May be based upon defect density reduction with justification

[1] Additional considerations may be necessary when evaluating product changes with respect to tin whiskers. Consult JESD201 when making changes involving high tin content materials. A separate table is located in JESD201 that addresses whisker test requirements based on various types of changes.

Annex A (informative) Nonhermetic package temperature cycling requirements

Solder joint Reliability is generally the limiting factor for component life in a system subjected to temperature cycling. Solder joint life is well modeled by a Coffin-Manson relation of $\Delta \mathbf{T}^{\mathbf{n}}$ where n=2. Other failure mechanisms as reported in JEP122 have larger acceleration factors so this becomes a worst case condition. The temperature cycling requirements have been normalized to the historical requirement of 500 cycles of Condition C using the n=2 factor. As a sanity check the typical use conditions for a number of common applications have been compared to these qualification conditions. As can been seen in the table below the qualification requirements exceed the use conditions by a wide margin.

Use Condition	**Use Condition Requirement**	**Equivalent Condition B -55 °C to +125 °C 700 cycles**	**Equivalent Condition G -40 °C to +125 °C 850 cycles**	**Equivalent Condition J 0 °C to +100 °C 2300 cycles**
Desktop 5 yr Life	ΔT 40 °C 2000 cy	14,175 cy (12,475 cy)* (11,057 cy)**	14,463 cy (12,761 cy)* (11,332 cy)**	14,375 cy (12,675 cy)* (11,250 cy)**
Mobile 4 yr Life	ΔT 15 °C 1500 cy	100,800 cy	102,850 cy	102,221 cy
Server 11 yr Life	ΔT 40 °C 44 cy	14,175 cy	14,463 cy	14,375 cy
Telecom (uncontrolled) / Avionics Controlled 15 yr Life	ΔT 25 °C 5500 cy	36,288 cy	37,026 cy	36,800 cy
Telecom (controlled) 15 yr Life	ΔT 6 °C 5500 cy	630,000 cy	642,812 cy	638,889 cy
Networking 10 year Life	ΔT 30 °C 3000 cy	25,200 cy	25,712 cy	25,557 cy

*JESD94, Table 1, Consider desktop with add'l ΔT 8 °C for 31,025 cycles and ΔT 20 °C for 1828 cycles

** Consider Desktop with additional ΔT 10 °C for 50,000 cycles

Annex B (informative) Differences between JESD47G and JESD47F

This summary briefly describes most of the changes made to entries that appear in this standard, JESD47G, compared to its predecessor, JESD47F (December 2007). Some punctuation changes are not included.

Page	Description of Change
7	In table 1, NVCE, change temperature range to 85°C ≥ Tj ≥ 55 °C and add fail criteria (0 fails)
7	In table 1, LTDR, change reference document to JESD22-A117
7	In table 1, NVCE, HTDR and LTDR entries, add number of note.
8	note (e): Specify fraction of device that needs to be cycled 100%, 10% and less than 10% of endurance spec. Specify constrains for delays between cycles
9	note (e): In definition of failure, add consideration of Bad Block management and allowed bit-error rate.
9	note (f), (g): In definition of failure, add consideration of allowed bit-error rate
10	Figure: Set NVCE temperature range to 85°C ≥Tj ≥ 55 °C, remove table redundant to note (e),

B.1 Differences between JESD47F and JESD47E

In 2.2; added references, JESD201 and JESD22A121
In Table 2; added “Tin Whisker Acceptance” row
In Table 3; added “Tin Whisker Acceptance” row
In 6.4, Table 4; under “New package to Qualified Product”, changed ESD-HBM from “R” to blank (no requirements) and ESD-CDM from “R” to “C”. Added reference 1 below table

B.2 Differences between JESD47E and JESD47D

This summary briefly describes most of the changes made to entries that appear in this standard, JESD47E, compared to its predecessor, JESD47D (November 2004). Some punctuation changes are not included.

JESD47E is a complete rewrite of the Specification for Stress Driven Qualification of Integrated Circuits. Every section was upgraded. This document lists the major changes by section. Many changes are for clarification or to conform to current JEDEC specification formats.

1. Scope: Updated references to allied JEDEC specifications that address similar issues.
2. Reference Documents: A more complete and current list is provided.
3. General Requirements: Clarifies using family qualification and generic data. Breaks up qualification into Silicon and Package Requirements. Clarifies use of X^2 distribution for generic and larger sample sizes. Gives guidance on the use of accelerated voltage stressing in addition to temperature.
4. Qualification and Requalification: No major changes
5. Qualification Tests: Test information is organized by fabrication process and package requirements. Information regarding a test is contained within a single table. More extensive reference to requirements for wearout testing and reference to JP001 Fabrication Process Qualification. Sample sizes were reduced for many tests that are intrinsic wearout mechanisms. The traditional 77 piece per lot sample size was only retained for lifetest and non-volatile memory endurance for which defect mechanisms are significant contributors to the observed failure rate.

B.2 Differences between JESD47E and JESD47D (cont'd)

Extensive notes were added to explain test methodologies.

a. Early Life Failure Testing: The methodology was specified and requirements were enumerated in Table B.
b. Low Temperature Operating Life: Minimum temperature was raised max frequency operation required, can be replaced by wafer level HCI testing.
c. NonVolatile memory: Endurance and Data Retention methodology was changed along with test method JESD22-A117 and JEP122.
d. Preconditioning: Is now required before all package tests
e. Temperature Cycling: Requirements were changed for all conditions except condition "C".
f. Autoclave: No longer recommended, especially for BGAs.
g. Power Temperature Cycling no longer required
h. Explained Cpk vs Ppk

6. Process/Product Changes: Improved explanation of changes requiring requalification and testing required.
7. Annex A: Added to explain change in component temperature cycling requirements.

Standard Improvement Form **JEDEC JESD47G**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

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_____

_____

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3. Other suggestions for document improvement:

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