Charge Pump with ACTIVE CYCLE Regulation -Closing the Gap between Linear- and Skip Modes

Erich Bayer, Hans Schmeller
Texas Instruments Deutschland GmbH, 85356 Freising, Germany

Abstract- ACTIVE CYCLE regulation, a novel dual-loop regulation technique for Charge Pumps closes the gap between conventional "Linear"- and "Skip" modes. It produces about the ripple of a "Linear" controlled Charge Pump which is one order of magnitude less than the ripple of a "Skip" mode converter. At the same time it consumes just the quiescent current of a "Skip" controlled Charge Pump, which is a few orders of magnitude less than that of a "Linear" one. Thus it combines the best of the two worlds we saw so far.

I. INTRODUCTION

Today's electronic systems usually cannot be operated with the voltage generated directly from the power source, which is the unregulated voltage from a battery or a mains-adapter. The load, which may be a microprocessor controlled equipment like a cellular phone or a medical instrument needs a very specific operating voltage with tight tolerances, low supply-voltage ripple and a good line- and load regulation. Therefore a voltage converter is necessary to transform the unregulated voltage into a stable system supply. Since more and more equipment is portable and powered from batteries there are additional requirements for this voltage converter which are high efficiency and low quiescent current, small board space, low weight and it must be cheap. The traditional approach to perform the voltage conversion uses an inductive DC/DC-converter, but sub-micron technologies, the availability of high value multi layer ceramic capacitors and new methods to increase the efficiency [1] are making Charge Pumps more and more attractive even in applications that need higher output currents. The major advantage of a Charge Pump is that it stores energy in a capacitor instead of in an inductor. Inductors are voluminous, can saturate, produce EMI and are quite expensive. Charge Pumps can produce a very low output voltage ripple when they work in "Linear" mode, they also consume a very low quiescent current when they work in "Skip" mode. What was missing so far is an operation mode that supports both requirements, a low ripple in combination with a low quiescent current. It will be shown, that "Active Cycle" regulation can combine the advantages of the two existing regulation schemes.

II. DESCRIPTION OF THE BEHAVIOUR OF A CHARGE PUMP VOLTAGE CONVERTER

There are many methods to analyze a switched capacitor DC-DC converter [2]-[6]. The basic approach in this paper that is similar to [7], is not aiming at a precise solution, but delivers a way to describe how the controlled system "Charge Pump" responds to the different regulation and disturbance quantities.

A. Regulated Voltage Doubler Topology and Operation

A inductor-less voltage doubler shown, in Fig. 1. consists of four switches (M1...M4), a "flying" capacitor, C_F and an output capacitor C_{OUT} on the node V_{OUT}. A single operation cycle of a Charge Pump can be divided into three phases:

Phase A (Charging Phase; M1 and M2 are conducting):
C_F is charged from V_{IN}. The average voltage across C_F is the input voltage V_{IN} reduced by the voltage losses across the On-resistances R_{M1} and R_{M2} of M1 and M2.

$$V_{CF} = V_{IN} - I_A (R_{M1} + R_{M2}) \tag{1}$$

Phase B (Transfer Phase; M3 and M4 are conducting):
C_F is placed in series with V_{IN} and discharged into the load capacitor C_{OUT}. The average voltage V_{OUT} is

$$V_{OUT} = V_{IN} + V_{CF} - I_B (R_{M3} + R_{M4}) \ . \tag{2}$$

Phase C (Wait Phase; M1...M4 are off):
No energy transfer from V_{IN} to C_F and C_{OUT}; V_{CF}=const.

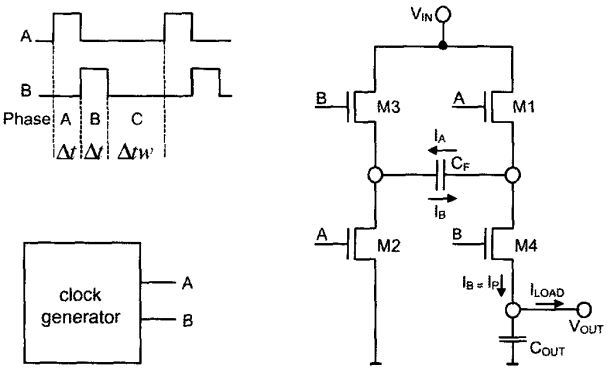

Fig. 1. Basic Structure of a Switched-Capacitor Voltage Doubler

In steady state, the average voltage across C_F stays constant. That means:

$$|\Delta Q_{CF}| \text{ (Phase A)} = |\Delta Q_{CF}| \text{ (Phase B)} \quad (3)$$

With 50% Duty-Cycle the duration of Phase A, Δt_A is equal to the duration of Phase B, Δt_B which is equal to Δt. Therefore the average charging current of C_F is equal to the average discharging current. Provided that the time constants in Charging Phase A and Transfer Phase B are big enough

$$C_F (R_{M1} + R_{M2}) \geq 10\,\Delta t \quad (4)$$

and

$$C_F (R_{M3} + R_{M4}) \geq 10\,\Delta t \quad (5)$$

then

$$|I_P| = |I_A| = |I_B| \quad . \quad (6)$$

The switches M1...M4 periodically toggle through Phases A, B and C so energy is transferred from the battery (V_{IN}) to the load (V_{OUT}) . A single-ended Charge Pump delivers energy to C_{OUT} only during the Transfer Phase B. During the rest of the cycle (Phases A and C), the load current is delivered from the output capacitor C_{OUT}. When the Charge Pump is working in a closed loop system, and the output voltage V_{OUT} has stabilized, the average energy the Charge Pump delivers must be equal to the energy consumed by the load. Therefore the output current I_P during the Transfer Phase can be written as

$$I_P = I_{LOAD} (2 + \Delta t_w / \Delta t) \; . \quad (7)$$

B. General Description of Output Voltage, Output Ripple and Quiescent Current

From the equations above we can obtain the output voltage as

$$V_{OUT} = 2V_{IN} - I_{LOAD} (2 + (\Delta t_w / \Delta t)) * \sum_{i=1}^{4} R_{Mi} \; . \quad (8)$$

The behavior of a Switched Capacitor Converter is shown in Fig. 2. Here, the regulated section "Charge Pump" produces

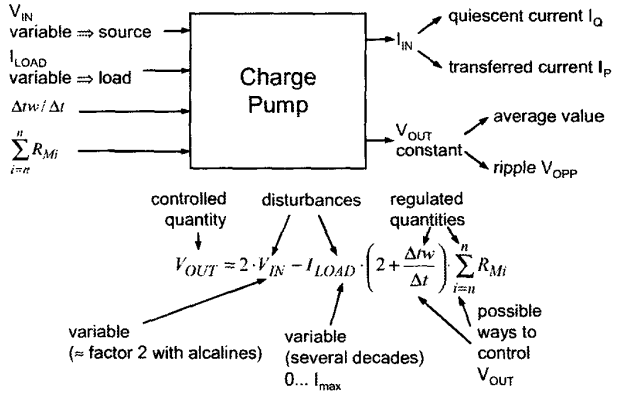

Fig. 2. Symbolic Description of a Switched-Capacitor Output Stage as a Regulated Section.

the controlled quantity V_{OUT}. There are two independently regulated quantities, the ratio ($\Delta t_w / \Delta t$) and the sum of the resistances ΣR_{Mi}. One of these two quantities is usually used to define the output voltage V_{OUT}. V_{IN} and I_{LOAD} act as disturbances, since they are defined by the application. The quantities V_{IN} and I_{LOAD} are normally not constant. V_{IN} varies with a factor of 2 when the device is operated from alkaline cells. In battery powered portable devices I_{LOAD} usually varies over several decades (from I_{LOAD}=0 to I_{LOAD}=$I_{LOADMAX}$).

Since C_{OUT} is periodically charged and discharged by a certain amount, the output voltage has a ripple.

During Transfer Phase B the current into C_{OUT}, I_{COUT} is

$$I_{COUT}(B) = I_{LOAD} (1 + \Delta t_w / \Delta t) \; . \quad (9)$$

In the Charging- and Wait Phases A and C, C_{OUT} is discharged with I_{LOAD}, so

$$I_{COUT}(A, C) = -I_{LOAD} \; . \quad (10)$$

With (9) and (10) the output voltage ripple V_{OPP} (peak to peak) can be written as follows:

$$V_{OPP} = I_{LOAD} [ESR(2 + (\Delta t_w / \Delta t)) + (\Delta t / C_{OUT})(1 + (\Delta t_w / \Delta t))]$$

The *ESR* (*E*quivalent *S*eries *R*esistance) of C_{OUT} can be neglected if it is much smaller than the ratio $\Delta t/C_{OUT}$. For an operation frequency of 500 kHz (Δt=1µs) and a C_{OUT} of 10µF, the ESR must be smaller than 0.1 Ω. If we use a multi layer ceramic capacitor with an ESR in the 20 mΩ range for C_{OUT} in this case, the output voltage ripple V_{OPP} can be written as

$$V_{OPP} \cong I_{LOAD} (\Delta t / C_{OUT})(1 + (\Delta t_w / \Delta t)) \; . \quad (11)$$

The quiescent current of a Charge Pump is that supply current from V_{IN} which is not transferred via C_{FLY} to the output capacitor C_{OUT}. It is the sum of the basic quiescent current I_{QB} and a current I_{QS} due to the switching process of the MOS-transistors M1 ... M4.

$$I_Q = I_{QB} + I_{QS} \quad (12)$$

I_{QB} is the supply current of the blocks (bandgap, comparators, voltage divider...) needed in additional to the voltage converter output stage to get a properly working closed loop system. This current which is in the range of 10...100 µA is more or less constant. The second component I_{QS} is the average current from V_{IN} needed to charge the gate capacitors C_{Mi} of the MOS-transistors M1...M4. Since each transistor M1...M4 is switched on and off once per operating cycle (Δt_{CYCLE} = 2Δt + Δt_w), I_{QS} depends on Δt_{CYCLE}. The total quiescent current I_Q is equal to

$$I_Q = I_{QB} + \frac{1}{(1 + (\Delta t_w / 2\Delta t))} (V_{IN} / 2\Delta t) * \sum_{i=1}^{4} C_{Mi} \; . \quad (13)$$

With V_{IN}=2.5V, an operating frequency of 1MHz (Δt=0.5µs), a total effective gate capacitance $\sum C_{Mi}$ of 1nF and zero Δt_w, $I_Q \cong I_{QS}$ = 2.5mA.

II. "LINEAR"- AND "SKIP" MODES: ADVANTAGES AND LIMITATIONS

The two traditional ways to control a Charge Pump to produce a constant output voltage, "Skip" mode that is shown in Fig. 3., and "Linear" mode that is illustrated in Fig. 4. are representing two special cases of formula (8) for V_{OUT} .

In "Skip" mode the sum of all On-resistances $\sum R_{Mi}$ is constant. Since this sum of resistances must be low enough to produce the specified output voltage at min. V_{IN} and max. I_{LOAD} it can be written as

$$\sum_{i=1}^{4} R_{Mi}(Skip) = \left(2V_{IN\,\min} - V_{OUT}\right)/2I_{LOAD\max} = const\,. \quad (14)$$

The output voltage is controlled by means of a comparison of output voltage level with a reference level and altering the ratio ($\Delta t_w/\Delta t$) which is the regulated quantity. A "Skip" regulation loop is a two-limits regulator.

A "Linear" mode Charge Pump runs with a constant frequency f = $1/(2\Delta t)$, the wait time Δt_w is zero and the sum of the On-resistances $\sum R_{Mi}$, which are controlled by the output voltage of a regulating OP-amp, is the regulated quantity.

Ref. [8] describes a PWM-type approach control of the inductor-less voltage converter. This is like the On-resistance control a "Linear" approach. The great disadvantage of a PWM-regulation is that it cannot support a wide dynamic range in load current, since there is a problem in generating extremely narrow control pulses for the power transistors.

If we put above conditions into (11) and (13) we get the following set of results for the output voltage ripple and the quiescent current in "Skip" – and "Linear" mode.

$$V_{OPP}(Skip) = I_{LOAD}\left(\Delta t/C_{OUT}\right)\left(1+\left(\Delta t_w/\Delta t\right)\right) \quad (15)$$

$$V_{OPP}(Linear) = I_{LOAD}\left(\Delta t/C_{OUT}\right) \quad (16)$$

$$I_Q(Skip) = I_{QB} + \frac{1}{\left(1+\left(\Delta t_w/2\Delta t\right)\right)}\left(V_{IN}/2\Delta t\right) * \sum_{i=1}^{4} C_{Mi} \quad (17)$$

$$I_Q(Linear) = I_{QB} + \left(V_{IN}/2\Delta t\right) * \sum_{i=1}^{4} C_{Mi} \quad (18)$$

From (15) and (16) one can see that the "Linear" mode produces the lowest possible ripple since the wait time Δt_w is zero. In "Linear" mode the peak current during the Transfer Phase B is exactly two times the load current.

$$I_P(Linear) = 2I_{LOAD} \quad (19)$$

Formula (14) shows that the sum of the On-resistances in a "Skip" mode operated Charge Pump must be defined at min. V_{IN} and max. I_{LOAD}. Therefore at max. V_{IN} the peak current in "Skip" mode can be written as

$$I_{P\max}(Skip) = 2I_{LOAD\max}\frac{2V_{IN\max} - V_{OUT}}{2V_{IN\,\min} - V_{OUT}}\,. \quad (20)$$

For the same load current, the output voltage ripple in "Skip" mode is $1+(\Delta t_w/\Delta t)$ times bigger than in "Linear" mode.

$$V_{OPP}(Skip) = V_{OPP}(Linear)\left(1+\left(\Delta t_w/\Delta t\right)\right) \quad (21)$$

A "Skip" controlled voltage doubler which is designed to deliver 3.3V from two alkaline cells produces a ripple which is 25 times higher than that of a "Linear" regulated one when operated at max. V_{IN} and max. I_{LOAD}.

If we compare the two results for the quiescent current (17) and (18) then we see the reverse behavior. With $I_{QS} >> I_{QB}$ we find that for the same load current, the quiescent current in "Linear" mode is $1+(\Delta t_w/2\Delta t)$ times bigger than in "Skip" mode.

$$I_Q(Linear) = I_Q(Skip)\left(1+\left(\Delta t_w/2\Delta t\right)\right) \quad (22)$$

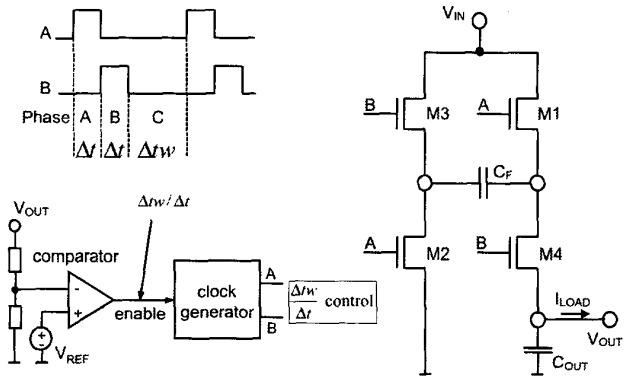

Fig. 3. Charge Pump working in "Skip" Mode.

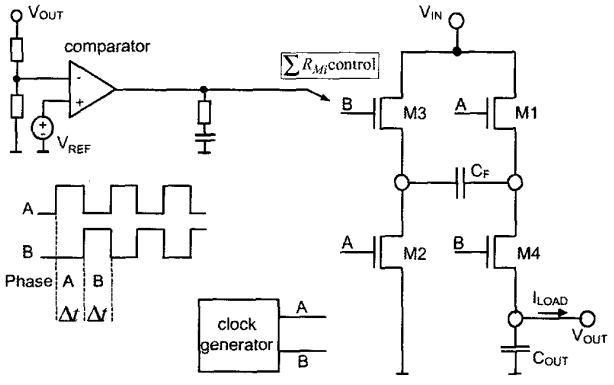

Fig. 4. Charge Pump operating in "Linear" Mode

When operated with low load currents the quiescent current of a "Linear" regulated Charge Pump can be a few orders of magnitude greater than that of an equivalent "Skip" controlled one.

To summarize one can say that both "Linear" – and "Skip" control cannot support a low output voltage ripple in combination with a low quiescent current.

III. "ACTIVE CYCLE" REGULATION – PRINCIPLE OF OPERATION

The "Active Cycle" controlled Charge Pump shown in Fig. 5. closes the gap between "Linear" mode with its good noise- but poor quiescent current performance, and "Skip" mode with its minimized quiescent current but high output ripple thus combining the best of the two worlds we saw so far.

This new control method for a Charge Pump varies both the ratio, $(\Delta t_w/\Delta t)$, and the sum of the On-resistances, $\sum R_{Mi}$, to get a stable output voltage. When operating at high loads it runs at a fixed ratio $(\Delta t_w/\Delta t)$ to keep the ripple as low as the "Linear" mode. Under light loads it keeps the resistance of the switches constant at a high value thus producing about one order of magnitude times less output voltage ripple than the "Skip" mode and more than ten times less quiescent current than the "Linear" mode.

Since there are two independent regulation quantities to be fixed in formula (8) there are two control loops necessary in an "Active Cycle" regulated Charge Pump. The first loop, a traditional "Skip" mode regulation loop, defines the output voltage V_{OUT}. Here the output voltage, V_{OUT}, is compared with a reference level, V_{REF}. If V_{OUT} is too small the Charge Pump is activated and pumps energy into C_{OUT}. When the voltage on V_{OUT} reaches V_{REF}, the device is turned off.

The second loop is responsible for determining the ratio $(\Delta t_w/\Delta t)$. The output signal of the "Skip" comparator has a ratio of $(\Delta t_w/2\Delta t)$. A pair of current sources I1/I2 in push/pull configuration with a filter capacitor, C_C, tied to its output converts this ratio into a DC voltage.

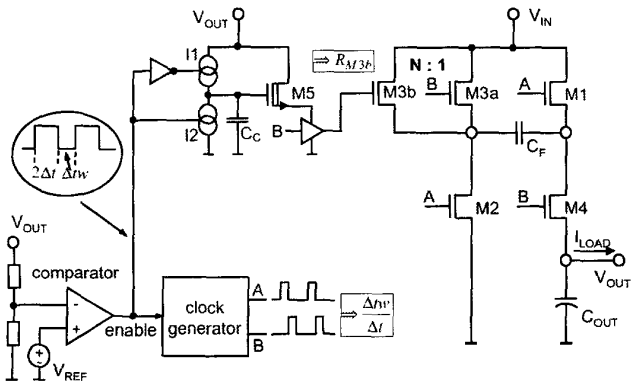

Fig. 5. Charge Pump with "Active Cycle" Regulation.

With the source follower, M5, controlling the supply voltage of the gate driver of M3b, the gate voltage of M3b is proportional to the voltage on C_C. Therefore the On-resistance of M3b is controlled by the ratio $(\Delta t_w/\Delta t)$, which means the $R_{DS\text{-}ON}$ increases with increasing wait time, Δt_w.

With growing On-resistance of M3b the amount of energy transferred per cycle decreases. To keep the output voltage V_{OUT} stable the "Skip" control loop has to reduce the wait time Δt_w to transfer more energy to the output by means of an increased number of operation cycles. With shorter wait time Δt_w the On-resistance again is reduced and so on. So the additional loop forces the ratio $(\Delta t_w/\Delta t)$ to stabilize to a value which is defined by the ratio of I1 to I2 independently of V_{IN} and I_{LOAD}. A smaller ratio of I1/I2 yields a smaller value of $(\Delta t_w/\Delta t)$.

To avoid a quasi-linear operation with fixed $(\Delta t_w/\Delta t)$ at low load currents which automatically results in a high I_Q, the second loop for determining $(\Delta t_w/\Delta t)$ is inhibited at low loads with the MOS-transistor M3 split into two parts. A larger part M3b (area = N) is $R_{DS\text{-}ON}$ controlled with the loop described above. M3a (area = 1) which is N times smaller than M3b runs with the full gate signal amplitude. So it has an N-times larger, but fixed $R_{DS\text{-}ON}$. When the load current is reduced, the two loops want to generate a stable V_{OUT} with a fixed $(\Delta t_w/\Delta t)$ by means of increasing the $R_{DS\text{-}ON}$ of M3b. Since the On-resistance of M3 in total (M3a and M3b in parallel) cannot be larger than that of M3a, at a certain level of I_{LOAD} the ratio $(\Delta t_w/\Delta t)$ can no longer be kept stable. To avoid a growing V_{OUT} with a further reduced I_{LOAD} the "Skip" control loop has to increase the wait time Δt_w. Now the "Active Cycle" controlled Charge Pump runs like a "Skip" regulated one with a large internal resistor $\sum R_{Mi}$ which is approximately the $R_{DS\text{-}ON}$ of M3a. When the On-resistance of M3a is N times larger than that of M3b and the rest of the switching MOS-transistors M1, M2, and M4 have about the $R_{DS\text{-}ON}$ of M3b, then the output voltage ripple at low load current is reduced by a factor of (N+3)/4 compared to a conventional "Skip" mode Charge Pump.

$$V_{OPP}(Act.-Cycle) = V_{OPP}(Skip)\ 4/(N+3) \quad (23)$$

Compared to a "Linear" controlled converter the output ripple V_{OPP} increases with a factor of $1+(\Delta t_w/\Delta t)$ which is a relatively small constant factor.

$$V_{OPP}(Act.-Cycle) = V_{OPP}(Linear)\ (1+(\Delta t_w/\Delta t)) \quad (24)$$

With an "Active Cycle" controlled Charge Pump, the switching portion of the quiescent current in (13) increases by a factor of (N+3)/4 which is the same factor as for the ripple reduction.

$$I_{QS}(Act.-Cycle) = I_{QS}(Skip)\ (N+3)/4 \quad (25)$$

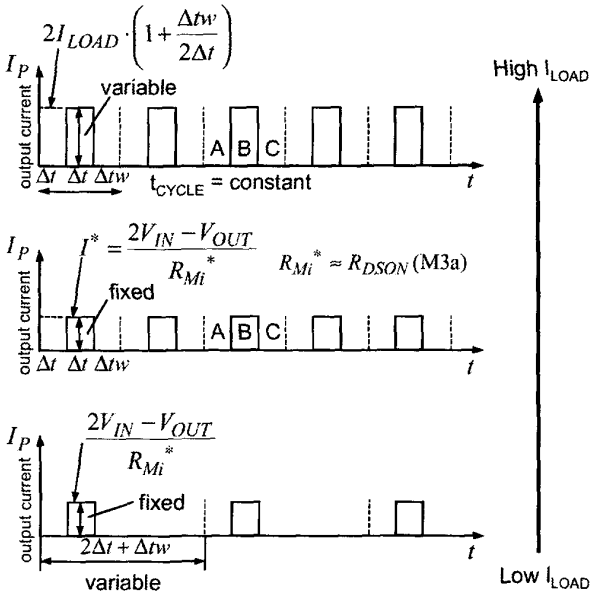

Fig. 6. Output Current I_P in "Active Cycle" Mode at Various Load Currents

Since I_{QB} dominates at low loads, the value of I_Q of an "Active Cycle" controlled Charge Pump is about the same as that for a "Skip" regulated one.

$$I_Q(Act.-Cycle) \cong I_{QS}(Skip) \cong I_{QB} \qquad (26)$$

Fig. 6. shows the different operating states of an "Active Cycle" regulated Charge Pump when operated at high-, medium- and low load current I_{LOAD}.

To summarize, one can say the following for the "Active Cycle" controlled Charge Pump in Fig. 5.:

1) For high load currents the ratio I1/I2 defines the ratio $(\Delta t_w/\Delta t)$ and therefore the increase in output ripple compared to a "Linear" regulated Charge Pump. (For $(\Delta t_w/\Delta t) = 1$, the ripple doubles.)

2) When operated at low load currents, the ratio: M3a/M3b = N defines the reduction in output voltage ripple and also the increase in quiescent current due to switching activity compared to a "Skip" Charge Pump.

3) At constant load, the amount of energy transferred with one cycle grows with increasing $(\Delta t_w/\Delta t)$, so the load transient response also improves with increasing $(\Delta t_w/\Delta t)$. For that reason, an "Active Cycle" controlled Charge Pump always has a better load transient response than a "Linear" regulated one.

4) An "Active Cycle" regulated Charge Pump is still a two-limits regulator. That means it has infinite DC-loop gain when regulating the output voltage V_{OUT}. Therefore the DC Line- and Load rejection is also infinitely high.

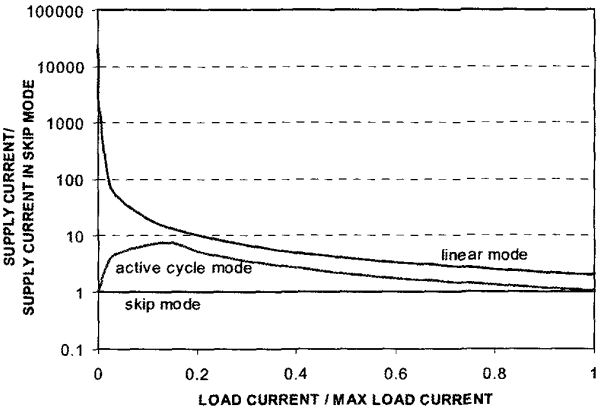

Fig. 7. Quiescent Supply Current versus Load Current

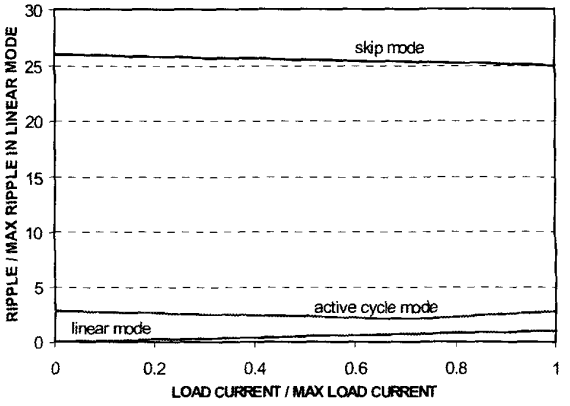

Fig. 8. Output Voltage Ripple versus Load Current

The graphs in Fig. 7. and Fig. 8. give a comparison between "Linear"- "Skip"- and "Active Cycle" modes:

At low load currents, I_{QB} dominates, I_Q of the "Active Cycle" mode is the same as in "Skip" mode. At medium load, the ripple reduction in "Active Cycle" is equal to the increase in I_Q compared to "Skip". At high loads, the ripple produced in "Active Cycle" mode is higher than in "Linear" but still a much lower ripple than in "Skip".

IV. Experimental Results

An "Active Cycle" regulated voltage tripler, TPS60140, that generates 5V from two primary cells (1.8V to 3.6V) was realized. The device TPS60140 can deliver an output current of 100mA, it runs at a frequency of 300kHz. A 10µF multi-layer ceramic capacitor is used for the output capacitor C_{OUT}. Fig. 9. and Fig. 10. show the output voltage ripple and the quiescent current at a variable load current.

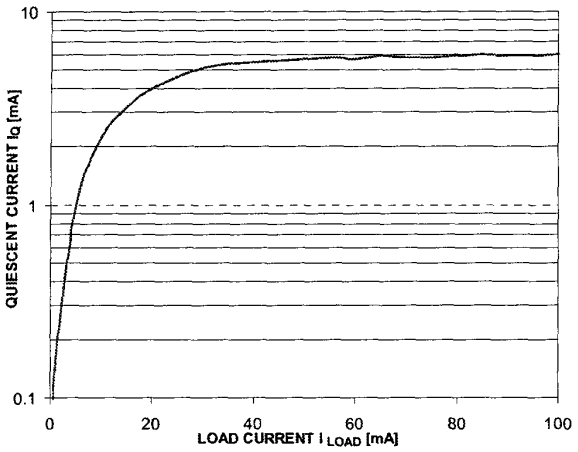

Fig. 9. Quiescent Supply Current of TPS60140 versus Load Current

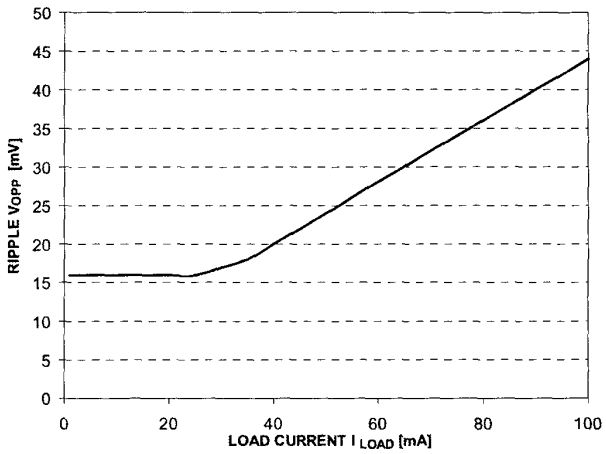

Fig. 10. Output Voltage Ripple of TPS60140 versus Load Current

It can be seen, that for I_{LOAD} = 0...30mA, the device runs with a fixed internal resistance $\sum R_{Mi}$ (constant output voltage ripple) and for load currents bigger than 30mA the device keeps ($\Delta t_w/\Delta t$) constant (output voltage ripple proportional to I_{LOAD}).

V. Limitations of "Active Cycle" Regulation

Looking at formula (11) one can see that the output voltage ripple is reduced with increasing output capacitance C_{OUT} or applying a higher operation frequency which means a reduction of Δt. This does not automatically mean that the ripple can be minimized without any limits. Since "Active Cycle" regulation is like "Skip" mode a two-limits regulator, it needs a certain ripple for proper operation. This minimum possible ripple comes from the fact that the propagation delay of a comparator increases with a reduction in input-overdrive. Therefore the minimum possible ripple of an "Active Cycle" controlled Charge Pump is represented by that input-overdrive of the comparator where the propagation delay is equal to Δt. With overdrive voltages below this critical value the Charge Pump fails to produce a proper sequence of charge- discharge- and wait Phases.

VI. Conclusion and Outlook

It has been demonstrated that the "Active Cycle" regulated Charge Pump can combine the requirements: low output voltage ripple and low quiescent current. "Active Cycle" regulation is the control method of choice for a single-ended Charge Pump topology. By its nature it is a "modified" "Skip" mode Charge Pump with a well defined output current and therefore still a two-limits regulator.

A "Linear" push-pull topology for the Charge Pump output stage can reduce the ripple even further. For a low quiescent current at small output currents a similar approach to "Active Cycle" regulation can be applied to the "Linear" regulator. This "modified Linear" or "Linear-Skip" regulator runs with zero ($\Delta t_w/\Delta t$) at high load currents. At light loads it keeps the internal resistance $\sum R_{Mi}$ constant and varies Δt_w like in "Active Cycle" mode to reduce the quiescent current.

Acknowledgement

The authors want to thank Gisela Oed for preparing the pictures, Guenter Goelz for his support with the Word-Software, Eckart Mueller and Kevin Scoones for going through the paper.

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