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Design and Optimization of a Low Power Voltage Reference Generator Circuit in 45nm CMOS Technology

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Abstract:
This paper presents a temperature compensated sub-threshold voltage reference generator which generates a reference voltage of 310 mV at a supply voltage of 0.8 V. Variation of output voltage with temperature over a range of 0 to 100°C is 310.219 to 309.765 mV which gives temperature coefficient of 14.62 ppm/°C. The proposed circuit is designed in 45nm CMOS technology. The quiescent current of the circuit is obtained 17.16 **μA** *and the total power consumption is found to be 13.73* **μW**.

Key words*: Sub-threshold circuit, Voltage reference, Temperature compensation*

1. Introduction

Voltage reference generator circuits find application in multiple quarters such as flash memories, analog to digital and digital to analog converters and analog signal processing systems. Due to extensive use of reference voltage generators, there is a need for a reference voltage generator circuit which is independent of variations in supply voltage, process parameter as well as temperature. If a circuit is independent of temperature variation, it is most likely independent of variation in process parameter since process parameters generally depend on temperature [2]. A reference generator circuit must be designed in such a way that it is independent of temperature, i.e, having zero TC. The most standard technique with regard to design of a voltage reference generator is bandgap reference. Bandgap reference generator circuits have a limitation that a reference output voltage less than 1.25 V can't be generated [3]. In earlier days these bandgap reference circuits performed very well because of high power supply of 5 V or 3 V. In the current scenario, such bandgap reference circuits are not suitable because the power supply voltage has reduced to 1 V or even 0.8 V. Therefore, in order to provide a stable reference voltage at these low supply voltages, the sub-threshold reference circuits are used. This is because in sub-threshold the transistor operates near threshold voltage. A sub 1 V voltage reference circuit was presented in [1]. In this work, the sub-threshold operation of MOSFET is used to minimize the power supply. In this work, two current sources are generated one with positive TC and other with negative TC. Both the currents are summed in proper ratio to get an output of nearly zero TC.

2. Principle of Operation

In sub-threshold operation when $V_{GS}=V_{TH,}$ the drain current of NMOS is significantly lower than the drain current of NMOS in either the saturation or in the triode region. The drain current in subthreshold conduction is given by the equation(1) [4].

$$I_D = I_o \frac{W}{L} \exp\left(\frac{V_{GS}}{\varsigma V_T}\right) \quad (1)$$

where I_o is reverse saturation current and ς is non-ideality factor, V_T is the thermal voltage, I_D is the drain current and V_{GS} is the gate to source voltage. Also, when the transistors are in sub-threshold conduction mode, the V_{GS} shows a linear relationship with temperature as given by the equation (2) [5].
i.e;

$$V_{GS} = V_{GS}(T_o) - K_G\left(\frac{T}{T_o} - 1\right) \quad (2)$$

where K_G is temperature coefficient and its value is greater than 0.
With the help of equation (1) current component in a circuit is derived which has a positive TC.With the help of equation (2) a current component is derived which gives an output current having negative TC. Both the output currents are added together in proper ratio to produce a current of zero TC. With the help of zero TC current, a zero TC voltage is obtained.

3. The Proposed Circuit and Analysis
Fig 1 shows the circuit diagram of the proposed circuit. Table II shows the W and L values of the transistors while table I shows the resistances values for various resistors that have been used in the simulation. The circuit consists of two current sources, one with positive TC and the other with negative TC where the MOSFET's are biased in sub-threshold and saturation region. Both the current sources are added together in a proper ratio so that they generate a constant current independent of temperature. This constant current passes through a resistor from where reference voltage is measured.

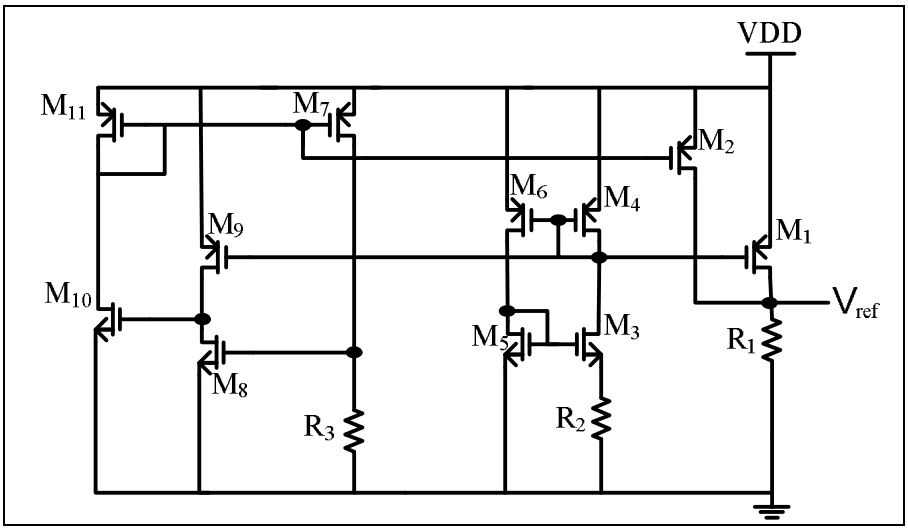

Figure1: The Proposed Circuit Diagram

Passive Components	Value in Kohm
R1	30
R2	40
R3	100

Table 1: The Value of All the Passive Components Used In the Proposedcircuit

Transistor	Channel length in nanometers	Channel width in nanometers
M1	100	1200
M2	100	200
M3	100	625
M4	100	250
M5	100	100
M6	100	100
M7	100	100
M8	100	625
M9	100	100
M10	100	100
M11	100	100

Table 2: The Values of W & L of All the Mosfets Used In the Proposed Circuit

3.1. Circuit Analysis

3.1.1. Generation of Proportional to Absolute Temperature (PTAT) Current Source

In this circuit, transistor $M_3 - M_6$ and R_2 generate PTAT current source and current generated through these transistors is mirrored to M_1. Therefore, the current I_{D_1} is the PTAT current source. In this circuit transistors, $M_3 - M_6$, the transistors M_3 and M_5 operate in sub-threshold mode and the others operate in saturation mode.

The expression for I_{D_1} is given in equation (3) and its derivation is given in appendix A.

$$I_{D1} = \frac{\varsigma v_T}{R_2} \frac{\left(\frac{W}{L}\right)1}{\left(\frac{W}{L}\right)4} \ln\left(\frac{\left(\frac{W}{L}\right)3\left(\frac{W}{L}\right)6}{\left(\frac{W}{L}\right)5\left(\frac{W}{L}\right)4}\right) \quad (3)$$

3.1.2. Generation of Complementary to Absolute Temperature (CTAT) Current Source

The current with negative temperature coefficient is generated by M_7, M_8 and R_3 and the current generated through these transistors is mirrored to M_2. So, the current I_{D2} is CTAT current source. The expression of I_{D2} is given in equation (4) and its derivation is given in appendix B.

$$I_{D2} = \frac{\left(\frac{W}{L}\right)2}{\left(\frac{W}{L}\right)7} \frac{V_{gs8}}{R_3} \quad (4)$$

The total current generated at R_1 is $I_{D1} + I_{D2}$,
So output reference voltage is

$$V_{ref} = R_1(I_{D1} + I_{D2}) \quad (5)$$

3.1.3. Temperature Compensation

Since I_{D1} having positive TC and I_{D2} having negative TC so adding them in proper ratio gives a constant current source independent of temperature. The constant current is flowing through resistance R_1 and gives constant V_{ref} independent of temperature .The proper ratio of I_{D1} and I_{D2} is selected by varying the W and L of the transistors. The W and L are selected on the basis of equation (6).

$$\frac{\partial V_{ref}}{\partial t} = 0 \quad (6)$$

4. Measurement Results

The proposed circuit in this paper is simulated in LTSpice using 45 nm CMOS technology.

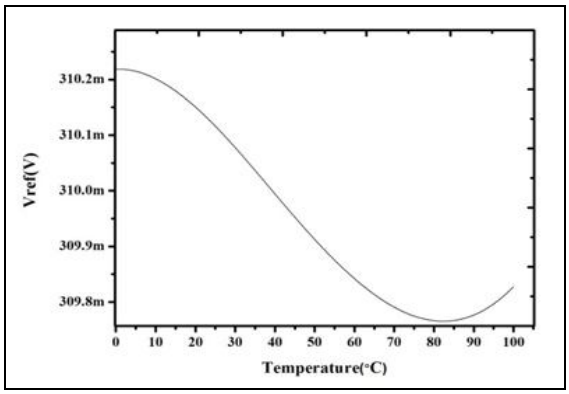

Figure 2: Temperature dependence of the generated reference voltage

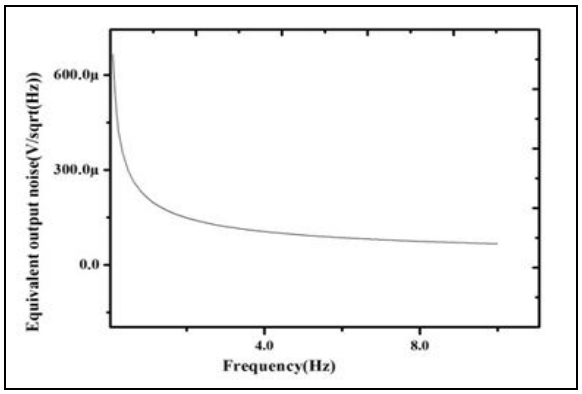

Figure 3: Simulated equivalent output noise $(V/\sqrt{Hz})$

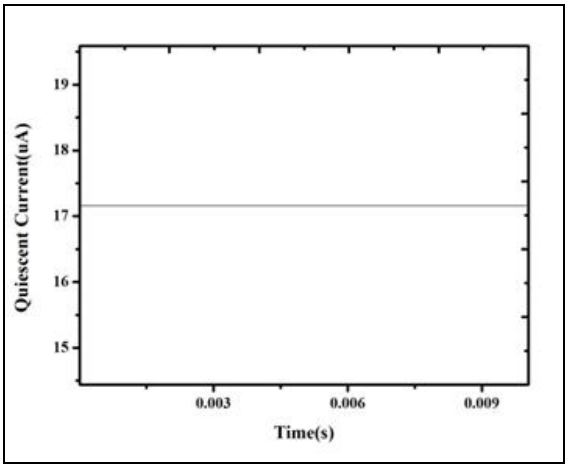

Figure 4: Simulated Quiescent current at VDD =0.8V

The reference voltage dependence on temperature is shown in figure 2. The ΔV_{ref} on the considered temperature range is 453.264 μV leading to an average TC of 14.62 ppm/°C. The mean output reference voltage is 310mV at 0.8V supply voltage.
The simulated equivalent output noise amplitude is shown in figure 3. The simulated quiescent current of the circuit is 17.16 μA approximately which has been shown in figure 4. The total power consumption of the proposed circuit is 13.73 μW .
The proposed circuit exhibits a very low TC at 0.8 V supply voltage. In order to validate the simulated results of the circuit used in this study, various parameters of previously reported circuits have been compared in table III.

	proposed circuit	ref.[6]	ref.[7]	ref.[8]	ref.[9]	ref.[10]
TC (ppm/°C)	14.62	18	32	14.8	16	48
Temperature range (°C)	0 to 100	-20 to 120	0 to 100	0 to 100	-20 to 80	0 to 100
Technology Node	45 nm	0.18 um	0.13 um	0.35 um	0.18 um	0.13 um
Output Voltage (mV)	310	695.6	182	905.5	591.6	718
supply voltage (V)	0.8	1.5	0.5	3.3	0.9	1.2

Table 3: The Comparison of Proposed Circuit with Some Recent Voltage Reference Circuits

5. Conclusion

The proposed circuit is simulated in 45nm CMOS technology. The circuit shows a remarkable reduction in temperature coefficient. The extremely small temperature coefficient i.e. 14.62 ppm/°C and low supply voltage, i.e. 0.8 V make it very attractive for battery operated electronic applications.

Appendix A

The derivation of equation (3), refer to figure 1, the transistor M_3 & M_5 are in sub-threshold conduction mode. We have

$$V_{gs5} = V_{gs3} + I_{D4}R_2 \tag{7}$$

In sub threshold conduction

$$V_{gs} = \varsigma v_T \ln\left(\frac{I_D}{I_o \frac{W}{L}}\right) \qquad From\,equation\,1 \tag{8}$$

So,

$$\varsigma v_T \ln\left(\frac{I_{D5}}{I_o\left(\frac{W}{L}\right)5}\right) = \varsigma v_T \ln\left(\frac{I_{D3}}{I_o\left(\frac{W}{L}\right)3}\right) + I_{D4}R_2 \tag{9}$$

$$\Rightarrow I_{D4} = \frac{\varsigma v_T}{R_2} \ln\left(\frac{I_{D5}\left(\frac{W}{L}\right)3}{I_{D3}\left(\frac{W}{L}\right)5}\right) \tag{10}$$

We also have
Because in the same branch

$$I_{D3} = I_{D4} \tag{11}$$

$$\Rightarrow I_{D5} = I_{D4}\left(\frac{\left(\frac{W}{L}\right)6}{\left(\frac{W}{L}\right)4}\right) \quad (12)$$

$$\Rightarrow I_{D4} = \frac{\varsigma v_T}{R_2}\ln\left(\frac{\left(\frac{W}{L}\right)6\left(\frac{W}{L}\right)3}{\left(\frac{W}{L}\right)4\left(\frac{W}{L}\right)5}\right) \quad (13)$$

This I_{D4} is mirrored to M_1 so we have

$$\Rightarrow I_{D1} = I_{D4}\left(\frac{\left(\frac{W}{L}\right)1}{\left(\frac{W}{L}\right)4}\right) \quad (14)$$

So

$$\Rightarrow I_{D1} = \left(\frac{\left(\frac{W}{L}\right)1}{\left(\frac{W}{L}\right)4}\right)\frac{\varsigma v_T}{R_2}\ln\left(\frac{\left(\frac{W}{L}\right)6\left(\frac{W}{L}\right)3}{\left(\frac{W}{L}\right)4\left(\frac{W}{L}\right)5}\right) \quad (15)$$

Appendix B

The derivation of equation 4 is, refer to figure 1, the current flowing through R3 is given by,

$$I_{R_3} = \frac{V_{gs8}}{R_3} \quad (16)$$

This $I_{R_3} = I_{D7}$ (17)

Because in the same branch

This I_{D7} is mirrored to M_2 so we have

$$\Rightarrow I_{D2} = I_{D7}\left(\frac{\left(\frac{W}{L}\right)2}{\left(\frac{W}{L}\right)7}\right) \quad (18)$$

$$\Rightarrow I_{D2} = \left(\frac{\left(\frac{W}{L}\right)2}{\left(\frac{W}{L}\right)7}\right)\left(\frac{V_{gs8}}{R_3}\right) \quad (19)$$

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