# Random Offset in CMOS IC Design

**ECEN4827/5827 Analog IC Design**

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# Where to start?

- How do we choose what transistor sizes to use in a design?

- One topic not often discussed in classes is random offset and how transistor sizing affects this phenomenon.

# Introduction

- 2 devices (MOSFET's, resistors, capacitors) of the same size, laid out next to each other, are not identical.
- How they differ is generally the function of random offsets during processing.
- These offsets vary from chip to chip and set a limit on precision attainable which is typically reflected as data sheet specifications.

# Misc. Definitions/Notation

- The following I-V equation for a MOSFET in saturation is used:

$$I_D = \frac{\beta}{2}(V_{GS} - V_t)^2 \quad \text{where} \quad \beta = \mu C_{ox}\frac{W}{L}$$

- A mixture of $V_t$ & $V_T$ is used where both are referring to threshold voltage, not thermal voltage

# Agenda

Systematic vs. random offset

Sources & profiles of random offset

Current Mirror/Diff Pair offset derivation & insights

Propagation of uncertainties math

Current Mirror/Diff Pair exercises

# Systematic vs. random mismatch

- Systematic
  - Mismatch in the circuit (or layout) because of poor designer choices (i.e. avoidable)
  - Each copy of the circuit should share this; calculable based on the average values of element parameters
  - Viewable using SPICE DC operating point simulation
- Random
  - Mismatch in the circuit because of wafer processing
  - Different chips will have different values, but the value will mostly remain the same (subject to temperature shifts, drift, etc.)
  - Each copy of the circuit should share this; calculable based on the statistical values of element parameters
  - Viewable using DCmatch and Monte Carlo simulations
  - This is what is usually thought of as matching

# Sources of random mismatch

- Sources of random mismatch include:
  - Edge effects (rough edges)
  - Implantation (finite number of charges & distribution)
  - Mobility
  - Oxide effects

See References (after Summary slide) for more information.

# Mismatch parameters

- Commonly investigated mismatch parameters:
  - MOSFET

    $V_t$, $\beta$ (mobility and W/L), $\gamma$ (Body Effect)
  - Resistors

    $\rho$ (resistivity)
  - Capacitors

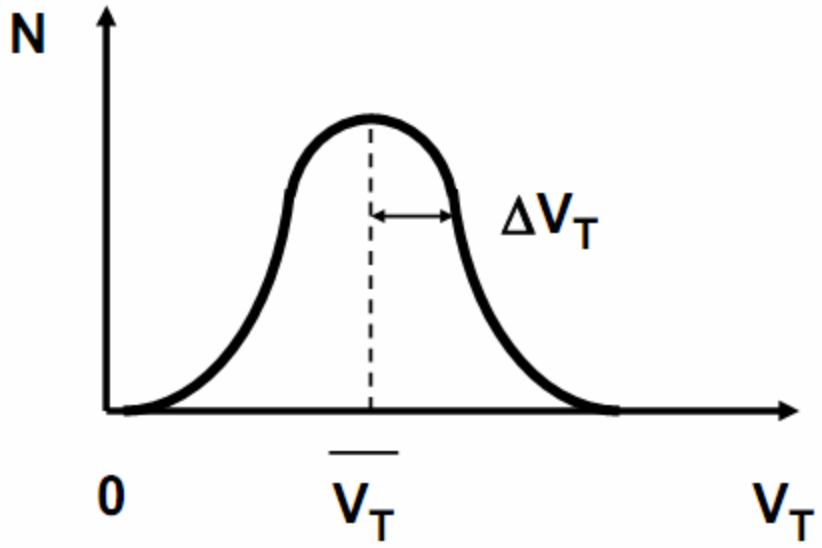
    oxide thickness variation

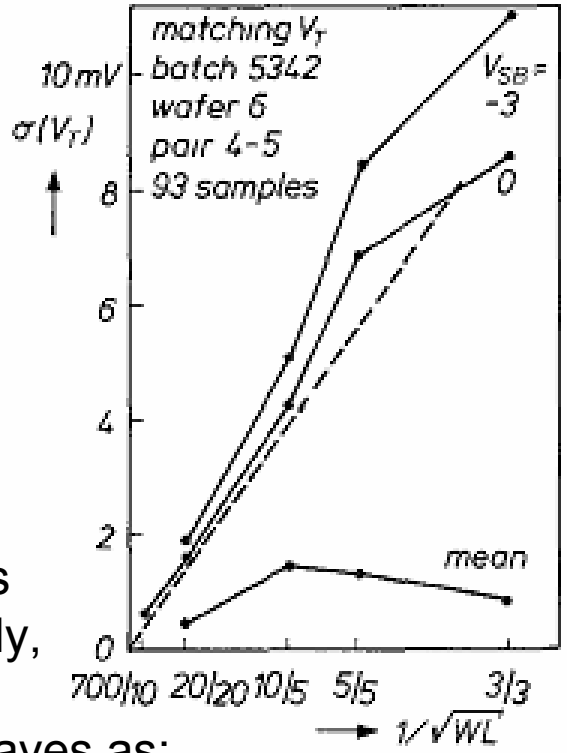
- This presentation covers $V_t$ & $\beta$ mismatch

# Profile of random mismatch

- Has a gaussian distribution
- Can be quantified by statistical variables of:
  - mean: $\bar{a}$
  - standard deviation: $\sigma_a$
  - variance: $\sigma^2_a$
  - Mismatch is defined as occurring between elements; a single element does not have mismatch, but a “self mismatch” can be defined.

# Threshold Voltage Mismatch



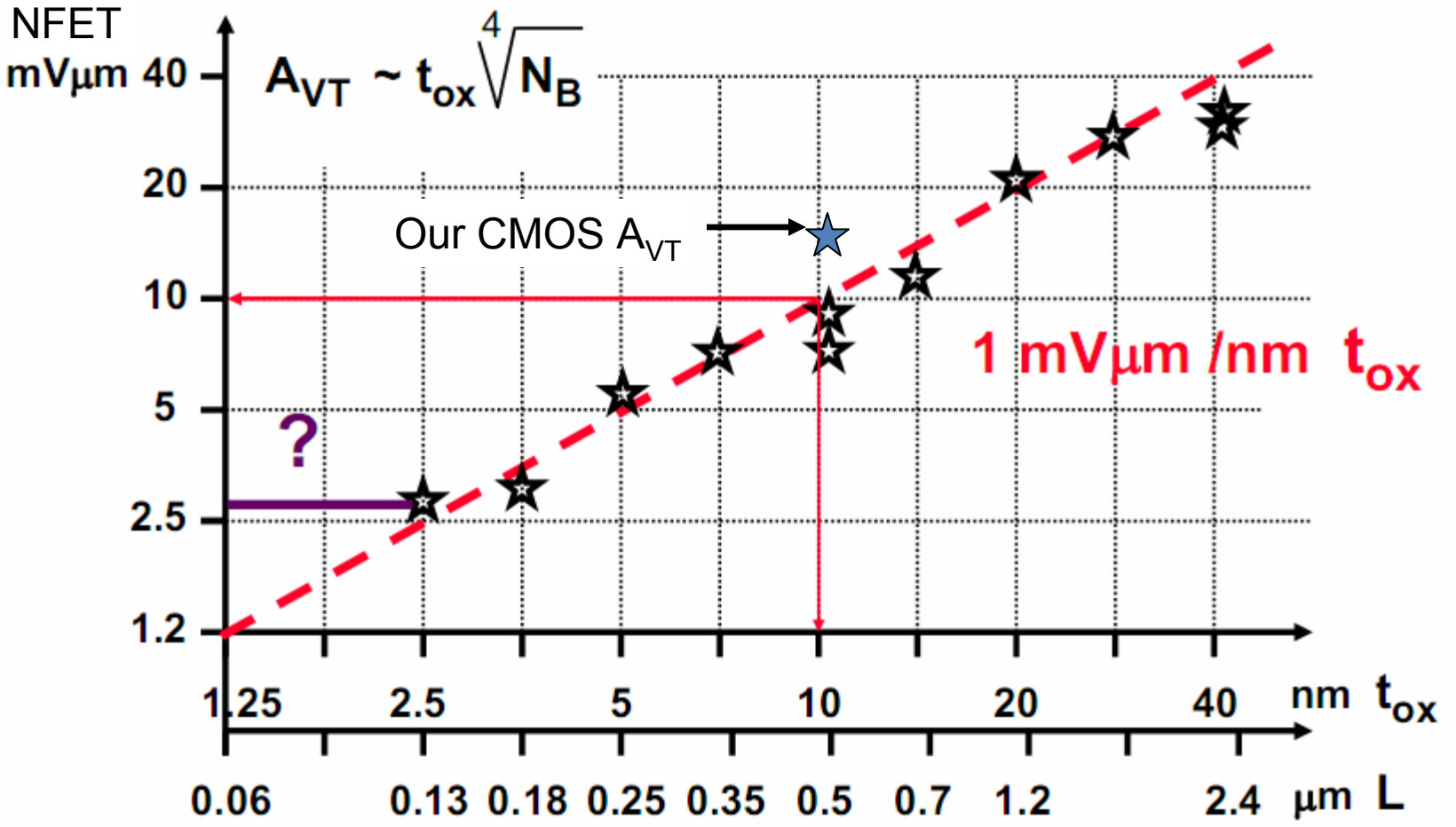

The threshold voltages among a group of transistors has a gaussian profile about a mean. Experimentally, it has been shown that the difference in threshold voltages between 2 identically sized transistors behaves as:

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}}$$

Note that to reduce the mismatch by ½ takes 4 times the area…

A fab will create test structures and measure $\Delta V_t$ multiple times per wafer for various sizes of transistors and collect ongoing statistics to monitor the process over time.

# Threshold Voltage Mismatch, cont'd




From W. Sansen showing how the mismatch constant, $A_{VT}$, varies roughly linearly with process size (doping concentration affects linearity of the relationship). Also, for p substrates, the **PMOS will have $A_{VT}$ ~ 1.5*$A_{VT}$ NMOS**.

# Current Factor Mismatch

Current Factor, $\beta$, behaves fractionally, as:

$$\frac{\sigma(\Delta\beta)}{\beta} = \frac{A_\beta}{\sqrt{WL}}$$

$A_\beta$ ~ 2%$\mu$m, invariant of process

National Semiconductor does not have this value characterized, so we may use this approximate value to estimate whether we need to worry about this or not.

# Offset Derivation

- Given the behavior of sufficiently uncorrelated parameters, want to know the effect of those parameters on 2 common circuits:
  - Current mirror
  - Differential pair

- Start with I-V equation for MOSFET and apply “total differential”:

$$\Delta f = \left(\frac{\partial f}{\partial x}\right)\Delta x + \left(\frac{\partial f}{\partial y}\right)\Delta y + \left(\frac{\partial f}{\partial z}\right)\Delta z + \ldots$$

# Offset Derivation – Current Mirror

What is the fractional error in the currents being mirrored in a 1:1 current mirror?

$$I_D = \frac{\beta}{2}\left(V_{gs} - V_T\right)^2 \qquad g_m = \sqrt{2\beta I_D} \text{ or } \frac{2I_D}{V_{gs} - V_T} \qquad \beta, V_{gs}, V_T \text{ variables}$$

$$\Delta I_D = \Delta\beta \frac{1}{2}\left(V_{gs} - V_T\right)^2 - \Delta V_T \frac{\beta}{2} 2\left(V_{gs} - V_T\right) + \Delta V_{gs} \frac{\beta}{2} 2\left(V_{gs} - V_T\right)$$

$\Delta V_{gs} = 0$ in a current mirror.
Divide by $I_D$ to get fractional error:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta\beta \frac{1}{2}\left(V_{gs} - V_T\right)^2}{\frac{\beta}{2}\left(V_{gs} - V_T\right)^2} - \frac{\Delta V_T \frac{\beta}{2} 2\left(V_{gs} - V_T\right)}{\frac{\beta}{2}\left(V_{gs} - V_T\right)^2}$$

$$\frac{\Delta I_D}{I_D} = \frac{\Delta\beta}{\beta} - \frac{\Delta V_T 2}{\left(V_{gs} - V_T\right)}$$

$$\boxed{\frac{\Delta I_D}{I_D} = \frac{\Delta\beta}{\beta} - \frac{g_m}{I_D}\Delta V_T}$$

# Offset Derivation – Diff Pair

What is $\Delta V_{GS}$ for 2 transistors operating at the same current?

$$I_D = \frac{\beta}{2}\left(V_{gs} - V_T\right)^2 \qquad g_m = \sqrt{2\beta I_D} \text{ or } \frac{2I_D}{V_{gs} - V_T} \qquad \beta, V_{gs}, V_T$$

$$\Delta I_D = \Delta\beta \frac{1}{2}\left(V_{gs} - V_T\right)^2 - \Delta V_T \frac{\beta}{2} 2\left(V_{gs} - V_T\right) + \Delta V_{gs} \frac{\beta}{2} 2\left(V_{gs} - V_T\right)$$

Constant current so $\Delta I_D = 0$

Divide by $\frac{\beta}{2} 2\left(V_{gs} - V_T\right)$

$$0 = \frac{\Delta\beta \frac{1}{2}\left(V_{gs} - V_T\right)^2}{\frac{\beta}{2} 2\left(V_{gs} - V_T\right)} - \Delta V_T + \Delta V_{gs}$$

$$\Delta V_{gs} = -\frac{\Delta\beta}{\beta} \frac{\left(V_{gs} - V_T\right)}{2} + \Delta V_T$$

$$\boxed{\Delta V_{gs} = -\frac{\Delta\beta}{\beta} \frac{I_D}{g_m} + \Delta V_T}$$

# Offset Derivation – Summary/Insights

- Differential Pairs and Current Mirrors operate with very different $g_m/I_d$ (i.e. bias point) ratios to minimize mismatch errors:
- Differential Pair: $\Delta V_{gs} = -\frac{\Delta\beta}{\beta}\frac{I_D}{g_m} + \Delta V_T$

  High $g_m/I_d$ → **low overdrive**
- Current Mirror: $\frac{\Delta I_D}{I_D} = \frac{\Delta\beta}{\beta} - \frac{g_m}{I_D}\Delta V_T$

  Low $g_m/I_d$ → **high overdrive**
- You can achieve this by designing <u>differential pairs with large W/L</u> and <u>current mirrors with small W/L</u> ratios

# Offset Derivation w/Standard Deviations

- Given the expected functional relationships of the 2 different offset behaviors, for various statistical reasons, you express these relationships in terms of standard deviations as:

Current Mirror

$$\frac{\Delta I_D}{I_D} = \frac{\Delta\beta}{\beta} - \frac{g_m}{I_D}\Delta V_T$$

$$\frac{\sigma(\Delta I_D)}{I_D} = \sqrt{\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \left(\frac{g_m}{I_D}\sigma(\Delta V_T)\right)^2}$$

Differential Pair

$$\Delta V_{gs} = -\frac{\Delta\beta}{\beta}\frac{I_D}{g_m} + \Delta V_T$$

$$\sigma(\Delta V_{gs}) = \sqrt{\left(\frac{\sigma(\Delta\beta)}{\beta}\frac{I_D}{g_m}\right)^2 + (\sigma(\Delta V_T))^2}$$

# Statistics Math

- You need to know how to propagate uncertainties to get the most out of this material.
- General form to propagate uncertainties for uncorrelated variables:

$$\sigma_z^2 = \sum_{i=1}^{n} \left( \frac{\partial f}{\partial v_i} \right)^2 \sigma_{v_i}^2$$

z = f(x,y,z…)

( n = # of variables )

$$\sigma_z^2 = \left( \frac{\partial f}{\partial x} \sigma_x \right)^2 + \left( \frac{\partial f}{\partial y} \sigma_y \right)^2 + \ldots$$

# Statistics Math, cont'd

- More commonly seen as this:
- Sum: $\sigma_z = \sqrt{\sigma_x^2 + \sigma_y^2}$ r.s.s, (square) root sum of squares

- Product/Quotient: f(x,y) = x*y or x/y

$$\frac{\sigma_f}{f} = \sqrt{\left(\frac{\sigma_x}{x}\right)^2 + \left(\frac{\sigma_y}{y}\right)^2}$$

Fractional error of f is the r.s.s of the fractional errors of the individual variables.

# Statistics Math, cont'd

To utilize these error propagation formulas, you need to know the individual contributions (e.g. $\sigma_x$, $\sigma_y$) which means you need the "self-mismatch" of the variables in question. This is found by noting that, if:

$\Delta V_t = V_{t1} - V_{t2}$ and we apply the sum formula, we get:

$$\sigma_{\Delta V_t} = \sqrt{\sigma_{V_{t1}}^2 + \sigma_{V_{t2}}^2} = \sqrt{2\sigma_{V_t}^2} = \frac{A_{V_t}}{\sqrt{WL}} \quad \text{or} \quad \sigma_{V_{t1,2}} = \frac{A_{V_t}}{\sqrt{2}\sqrt{WL}}$$

With a "self-mismatch" defined, we can now calculate the standard deviation of all sorts of mathematical operations of statistical parameters. We can calculate the accuracy of a 50x current mirror, for example, by utilizing the quotient version to propagate the uncertainty of the mirror gain.

# Statistics Math - Summary

- To propagate a …

sum: z = x + y

$$\sigma_z^2 = \sigma_x^2 + \sigma_y^2$$

product: z = x*y

$$\sigma_z^2 = \left(y\sigma_x\right)^2 + \left(x\sigma_y\right)^2$$

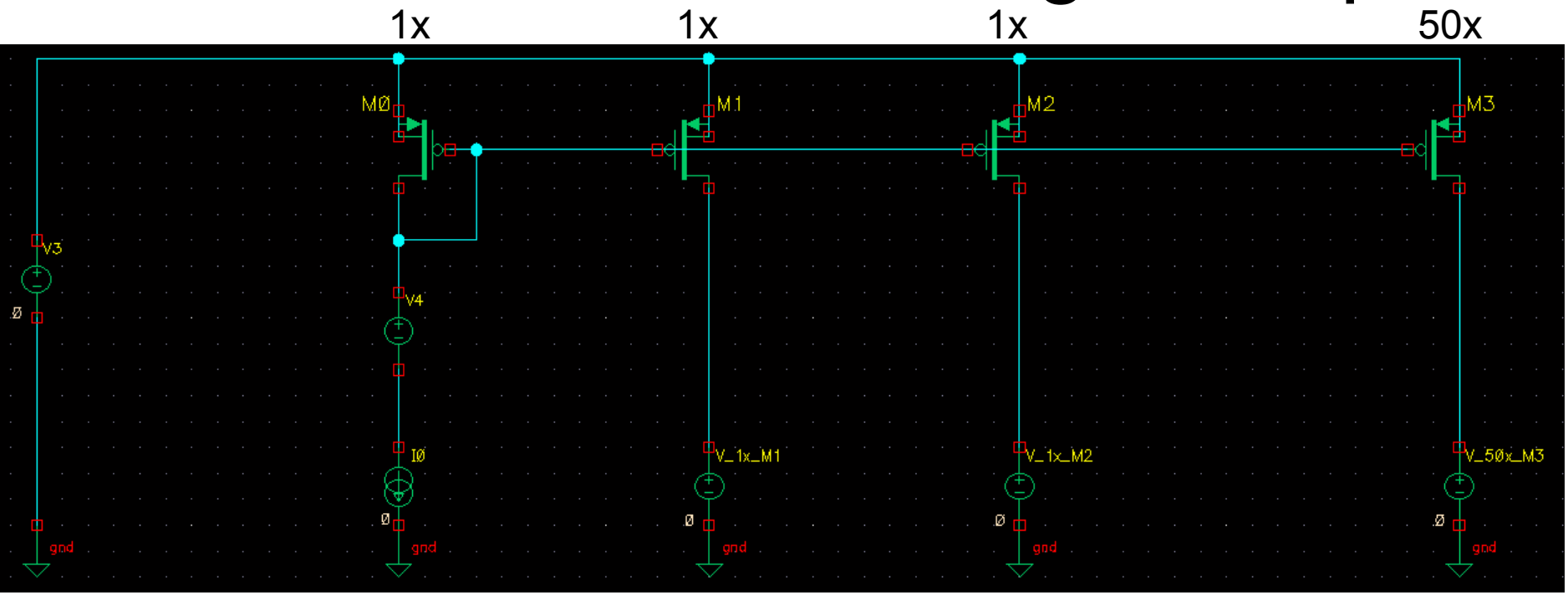
$$\sigma_z^2 = (xy)^2\left\{\left(\frac{\sigma_x}{x}\right)^2 + \left(\frac{\sigma_y}{y}\right)^2\right\}$$

quotient: z = x/y

$$\sigma_z^2 = \left(\frac{\sigma_x}{y}\right)^2 + \left(-\frac{x\sigma_y}{y^2}\right)^2$$

$$\sigma_z^2 = \left(\frac{x}{y}\right)^2\left\{\left(\frac{\sigma_x}{x}\right)^2 + \left(\frac{\sigma_y}{y}\right)^2\right\}$$

# Current Mirror Matching Example




- Ratios: 1:1:1:50
- Problem: Design 1:1 to required accuracy (1%), for $I_d$=1$\mu$A
- Procedure: Calculate self-mismatch and utilize statistics.

# Current Mirror Matching, cont'd

- PMOS: $\mu_p C_{ox}$=23μA/μm, $I_d$ = 1μA

$$\frac{\sigma(\Delta I_D)}{I_D} = \sqrt{\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \left(\frac{g_m}{I_D}\sigma(\Delta V_T)\right)^2}$$

- If β mismatch not modeled, $\frac{\sigma(\Delta I_D)}{I_D} = \frac{g_m}{I_D}\sigma(\Delta V_T)$
- Design 1:1 mirrors for 1%: $\frac{\sigma(\Delta I_d)_{self}}{I_d} = \frac{1\%}{\sqrt{2}} = \frac{.01}{\sqrt{2}}$
- $\frac{g_m}{I_d} = \sqrt{\frac{2\beta}{I_d}} = \sqrt{\frac{2\mu_p C_{ox}}{I_d}\frac{W}{L}}$ & $\sigma_{V_{t1,2}} = \frac{A_{V_t}}{\sqrt{2}\sqrt{WL}}$

$$\frac{\sigma(\Delta I_d)_{self}}{I_d} = \sqrt{\frac{2\mu_p C_{ox}}{I_d}\frac{W}{L}}\frac{A_{V_t}}{\sqrt{2}\sqrt{WL}} = \frac{A_{V_t}}{L}\sqrt{\frac{\mu_p C_{ox}}{I_d}} = \frac{23mV}{L}\sqrt{\frac{23\mu A}{1\mu A}}$$

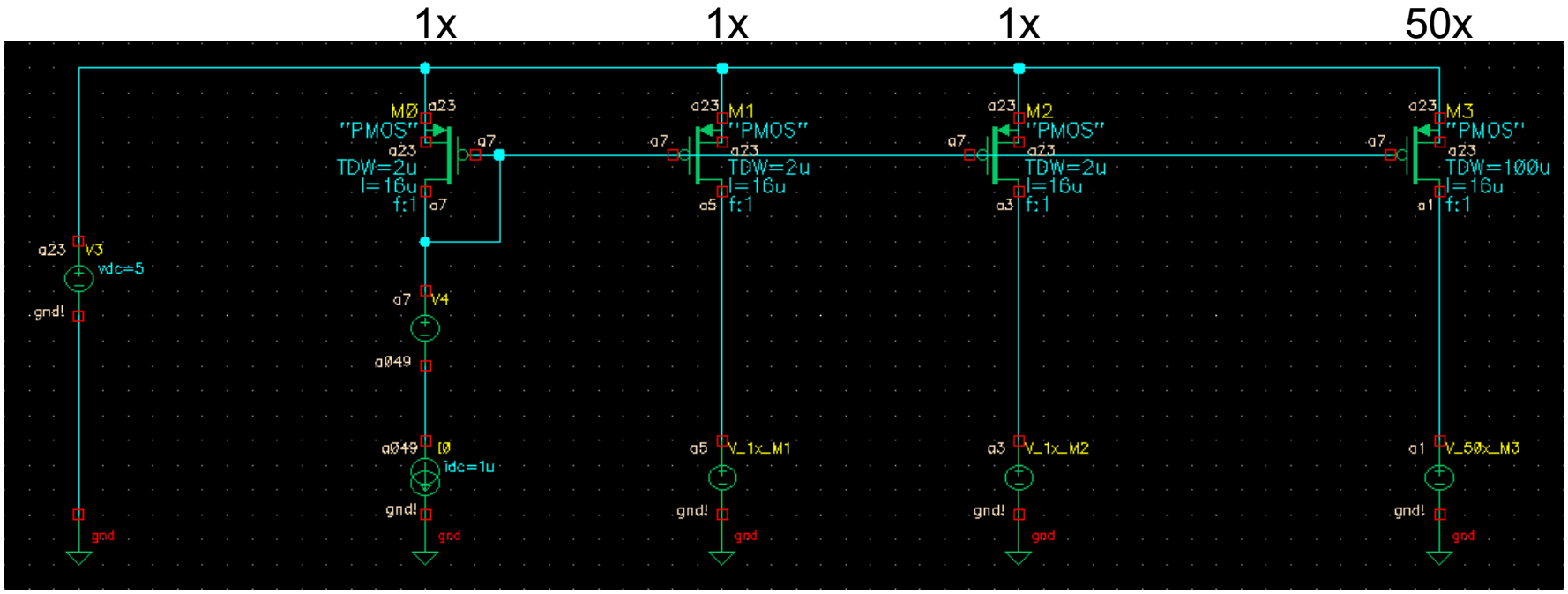
$$\frac{\sigma(\Delta I_d)_{self}}{I_d} = \frac{.110}{L}$$

← Note: **<u>no dependence on W, only L!!</u>**

$$\frac{.01}{\sqrt{2}} = \frac{.110}{L} \rightarrow L = 15.6$$

Use W/L=2u/16u

# Current Mirror Circuit



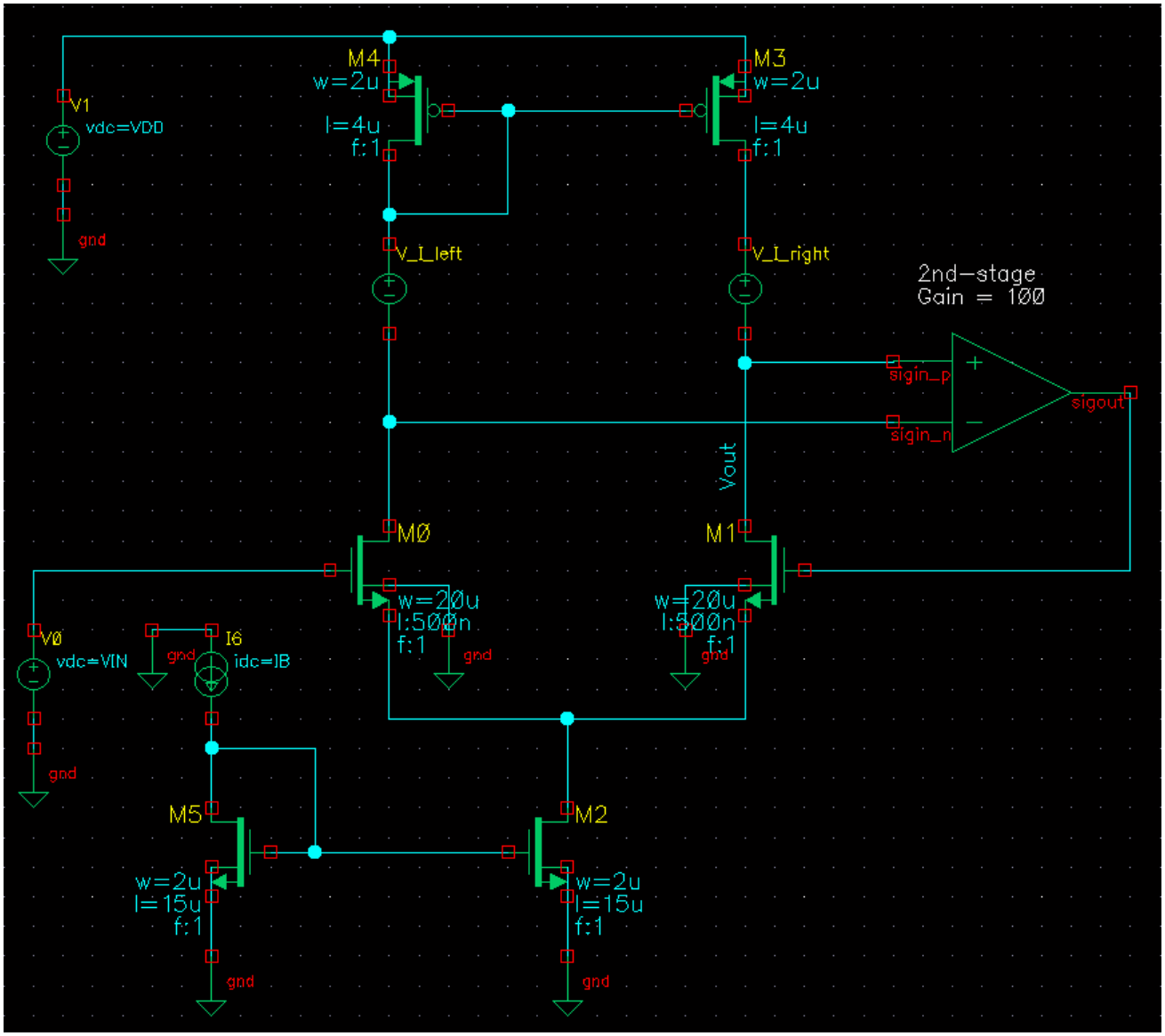

- 1:1:1 all have TDW = 2u
- 50x  has TDW = 2u*50 = 100u

# Current Mirror Followup

- Did neglecting $\beta$ mismatch matter?
- What is the matching for the 50x mirror?

See Appendix B

# Diff Pair Example




Use analysis to estimate input offset voltage to diff pair.

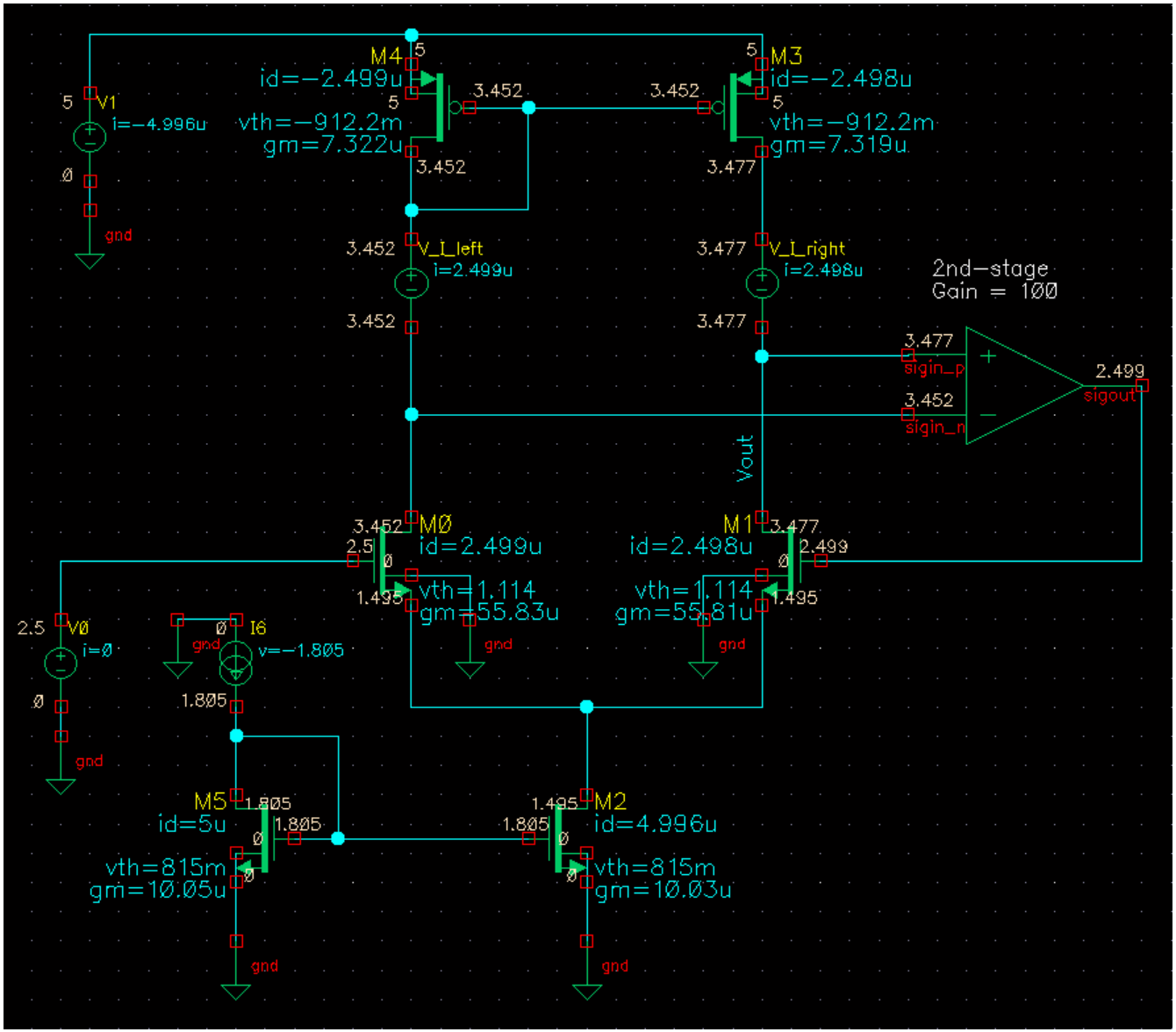
3 steps:

1.Calculate $\Delta V_{gs}$ of input pair

2.Calculate $\Delta I_d/I_d$ of current mirror and reflect to input using $g_m$ of input pair

3.Combine 2 independent sources using sum propagation

# Diff Pair Circuit, Quiescent Conditions




Need to know things like $g_m$, $I_d$ for total offset calculations

# Diff Pair Circuit, Step 1

1. Calculate $\Delta V_{gs}$ of input pair

$$\sigma\left(\Delta V_{gs}\right)=\sqrt{\left(\frac{\sigma(\Delta\beta)}{\beta}\frac{I_D}{g_m}\right)^2+\left(\sigma\left(\Delta V_T\right)\right)^2}$$

- W/L = 20u/.5u, $A_{Vt}$ = 16mVμm

$$\sigma_{\Delta V_t}=\frac{A_{V_t}}{\sqrt{WL}}=\frac{16mV\mu m}{\sqrt{20\mu m*0.5\mu m}}=5.06mV$$

- $g_{m\_M0/M1}$ = 55.8μA/V, $I_d$ = 2.5μA, $A_\beta$ ~ 2%μm

$$\frac{\sigma(\Delta\beta)}{\beta}\frac{I_D}{g_m}=\frac{.02\mu m}{\sqrt{20\mu m*0.5\mu m}}*\frac{2.5\mu A}{55.8\,\mu A/V}=.28mV$$

- Total = $\sigma\left(\Delta V_{gs}\right)=\sqrt{(.28mV)^2+(5.06mV)^2}=5.07mV$

# Diff Pair Circuit, Step 2

1. Calculate $\Delta I_d/I_d$ of mirror pair

$$\frac{\sigma(\Delta I_D)}{I_D} = \sqrt{\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \left(\frac{g_m}{I_D}\sigma(\Delta V_T)\right)^2} = \sqrt{\left(\frac{.02\mu m}{\sqrt{2\mu m * 4\mu m}}\right)^2 + \left(\frac{7.32\,\mu A/V}{2.5\mu A}\frac{23mV\mu m}{\sqrt{2\mu m * 4\mu m}}\right)^2} = .025$$

- Reflect current error to input offset through $g_{mN}$

$$\sigma_{\Delta Vgs} = \left(\frac{\sigma(\Delta I_D)}{I_D}\right) * I_D / g_{mN} = .025 * 2.5\mu A / 55.8\,\mu A/V = 1.12mV$$

# Diff Pair, Step 3 (r.s.s)

- Last step is to combine these 2 independent sources of error into the total:

$$\sigma_{\Delta Vgs\_total} = \sqrt{\underbrace{(5.07mV)^2}_{\text{input pair}} + \underbrace{(1.12mV)^2}_{\text{current mirror}}} = 5.19mV$$

- Given a choice to add area to current mirrors or input pair, in this example, more to be gained by using the area for the input pair.

# Summary Points

- Current mirror accuracy is improved with low W/L ratios
  - If $\beta$ mismatch is not a factor, current mirror accuracy is determined by selection of L only.
- Differential pair accuracy is improved with high W/L ratios
- Based on surveys of published fabrication data, you can estimate mismatch coefficients for your own process rather easily
- Uncorrelated statistics provide the basis to propagate individual mismatch information to arbitrary destinations
- Random mismatch can be improved with more area but it's costly: $mismatch \propto \frac{1}{\sqrt{WL}}$
- CAD tool analyses such as DCmatch and Monte Carlo are a useful tools for getting insight into sources of mismatch (expected and unexpected)

# References

- Layout:
  - The Art of Analog Layout, Alan Hastings
- General Information:
  - Analog Design Essentials, W. C. Sansen
- Early classic paper and commentary:
  - Matching properties of MOS transistors, Marcel J. M. Pelgrom, JSSC, Oct. 1989
  - http://www.ieee.org/organizations/pubs/newsletters/sscs/jan05/jssc1.html
- Recent papers with references:
  - “Device mismatch and tradeoffs in the design of analog circuits”, Peter Kinget, JSSC, June 2005 (in depth, with many references)
  - “Device Mismatch: An Analog Design Perspective”, Peter Kinget, ISCAS 2007, (condensed information)
- Cadence application note on DCmatch:
  - Affirma™ Spectre® DC Device Matching Analysis Tutorial

# Appendix A – CAD tools

- Cadence and other vendors have analyses to assist in propagating mismatch sensitivities to designated voltage nodes or current branches
- 2 analyses which we use are:
  - DCMatch
  - Monte Carlo

# Tools for Checking Matching

- “Local” mismatch: DCMatch (Spectre analysis)
  - Uses small signal analysis to reflect the combination of modeled mismatches to an arbitrary output node
  - By “local”, we mean the signal deviations introduced must not alter the dc operating point for the results to be accurate (i.e. small signal assumption)
  - Fast to run

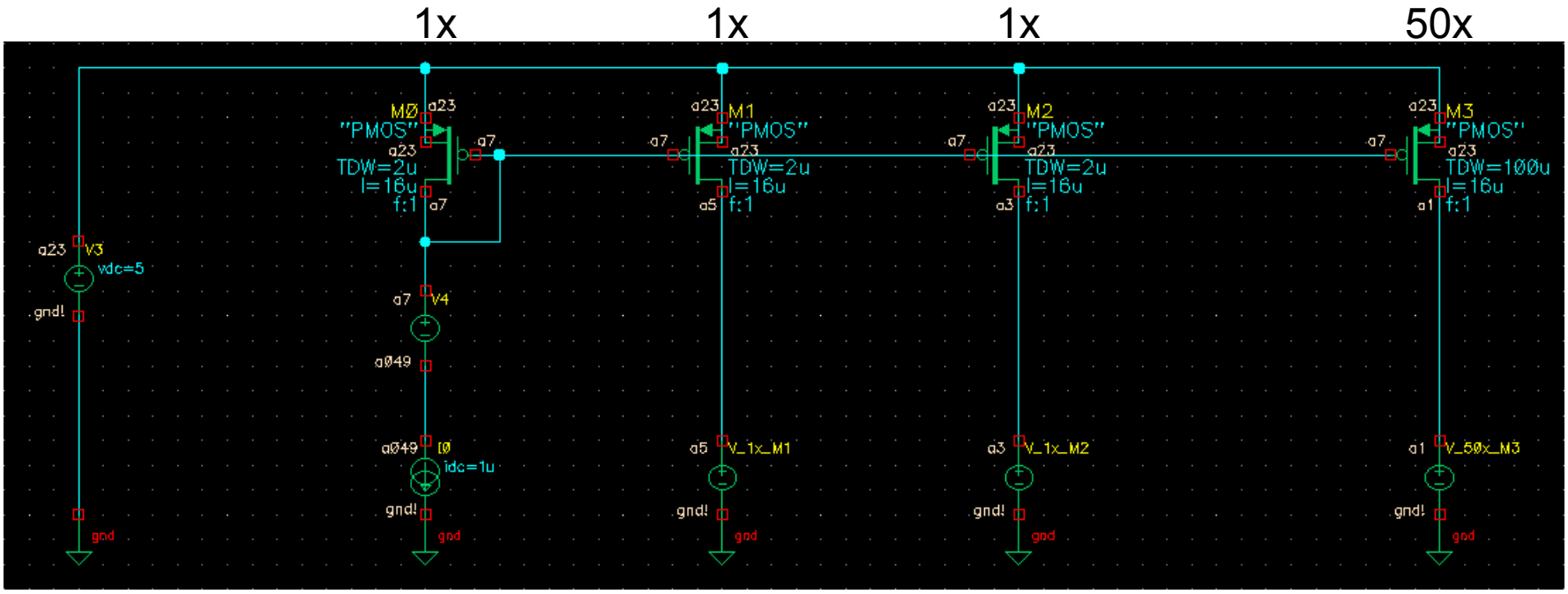
# Tools for Checking Matching

- "Global" mismatch: Monte Carlo
  - Alters parameters of individual elements, drawing variation from a statistical distribution.
  - Pro: Unlike DCMatch, doesn't rely on linear approximation, so does a (slightly) better estimate of matching, because real components are nonlinear.
  - Con: You need to run 100's of simulations to develop good statistics which means this takes 100's of times longer than DCMatch (which is 1 DC simulation); reported mean should be close to DC simulation if enough points are chosen.

# Procedure for Checking Matching

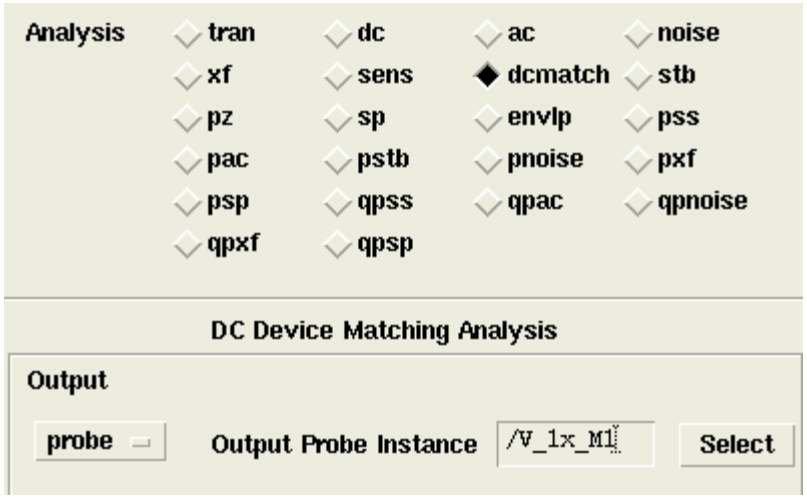
1. Use hand calculations to estimate required transistor sizes to meet matching
2. Utilize DCMatch to verify hand calculations. In more complicated circuits, a sensitivity from an unexpected transistor can show up
3. Later, utilize Monte Carlo to double check

# Current Mirror Circuit




- 1:1:1 all have TDW = 2u
- 50x  has TDW = 2u*50 = 100u

# Current Matching: DCMatch



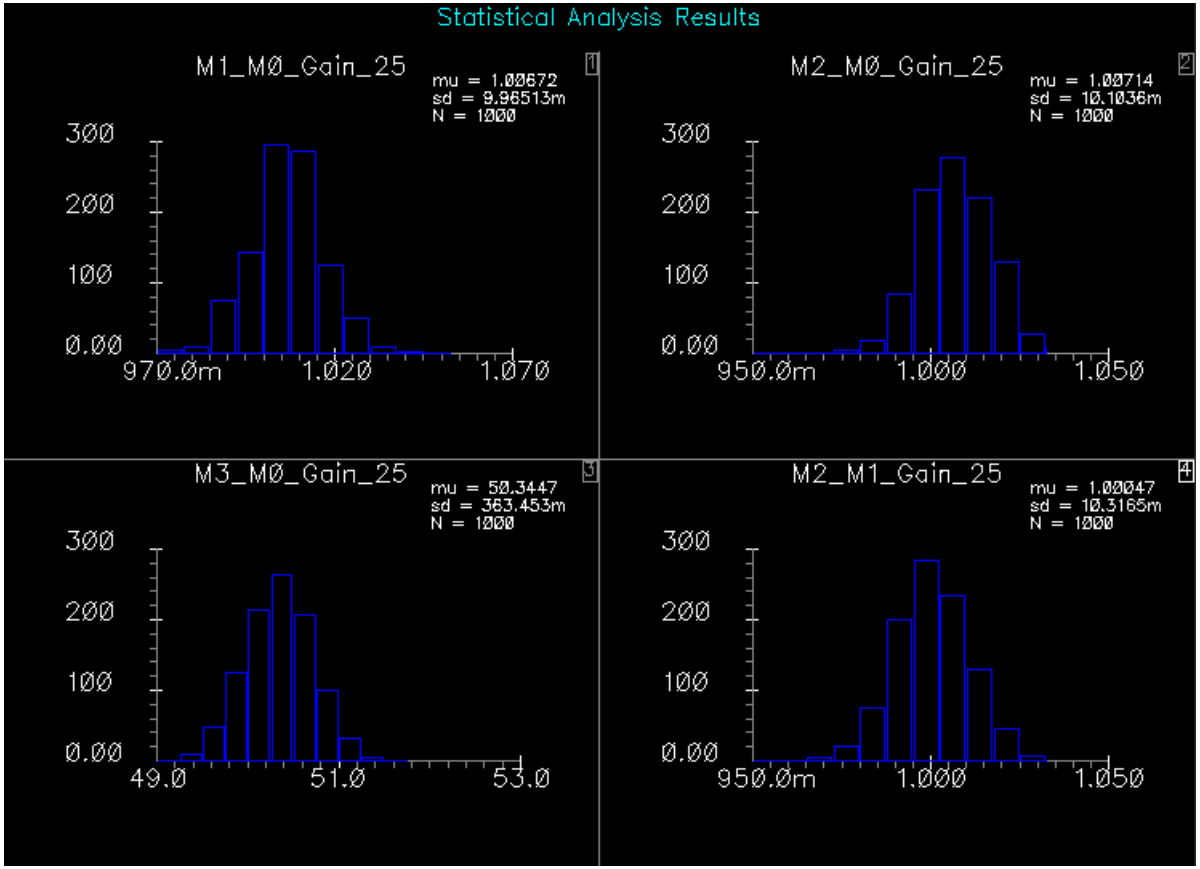

Select dcmatch analysis.

The Output is a probe (i.e. current), the voltage source, V_1x_M1.

```
bsim3v3
sigmaOut    sigmaVth    sigmaBeta   sigmaVg     sigmaIds
-20.3 nA    8.81 mV     0 %         8.81 mV     2.01 %      M1
20.2 nA     8.81 mV     0 %         8.81 mV     2.01 %      M0

2 bsim3v3 with absolute contributions below 0.1 % of maximum not shown.


V_1x_M1 = 1.007 uA  +/- 28.63 nA  (3-sigma variation)

Accumulated DC solution time = 0 s.
Intrinsic dcmatch analysis time = 0 s.
Total time required for dcmatch analysis `dcmatch' was 0 s.
```

Only sensitivities found are from M1 and M0. Note that sigmaBeta = 0, since it's not modeled. The sigmaIds value of 2% gets added in r.s.s fashion to achieve an overall fractional error of 28.63n/1.007u = 2.84% = 2%*sqrt(2). This is a 3-$\sigma$ value, so 1-$\sigma$ ~ .95% < 1%

# Current Matching: Monte Carlo




## Salient Features:

Matching Gain for M1:M0 and M2:M0 have 1% $\sigma$, but about .7% mean error.

M2:M1 mean error is about .05%.

Why(1)?

M3:M0 (50x) gain error can be calculated using the quotient formula of the Statistics Math:

$$\frac{\sigma_f}{f} = \sqrt{\left(\frac{\sigma_x}{x}\right)^2 + \left(\frac{\sigma_y}{y}\right)^2} = \sqrt{(.001)^2 + (.00707)^2} = .00714 = .7\%$$

← More detail in Appendix B

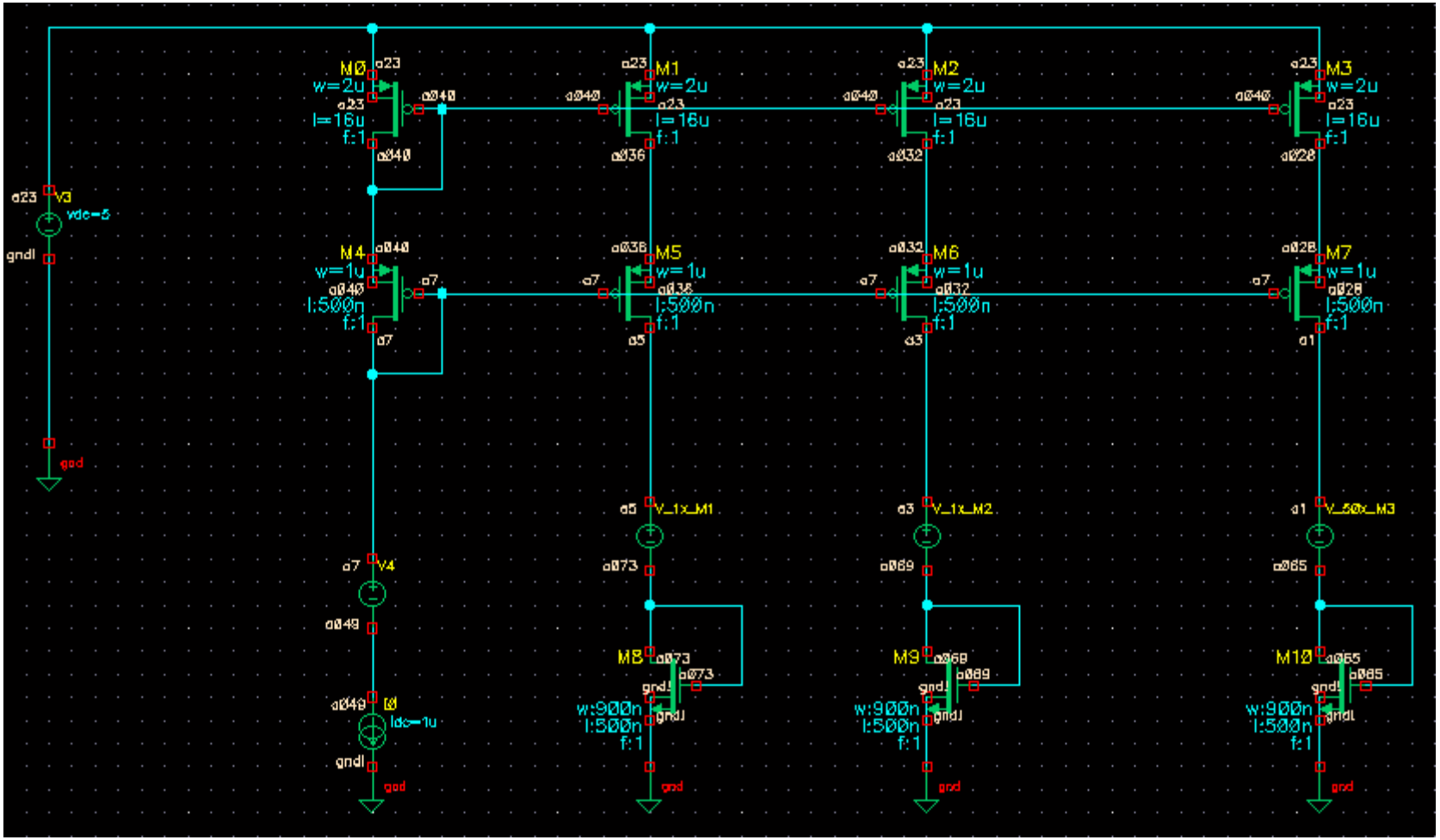
.7% $\sigma$, why not 1%(2)?

# Current Matching: Monte Carlo, cont'd

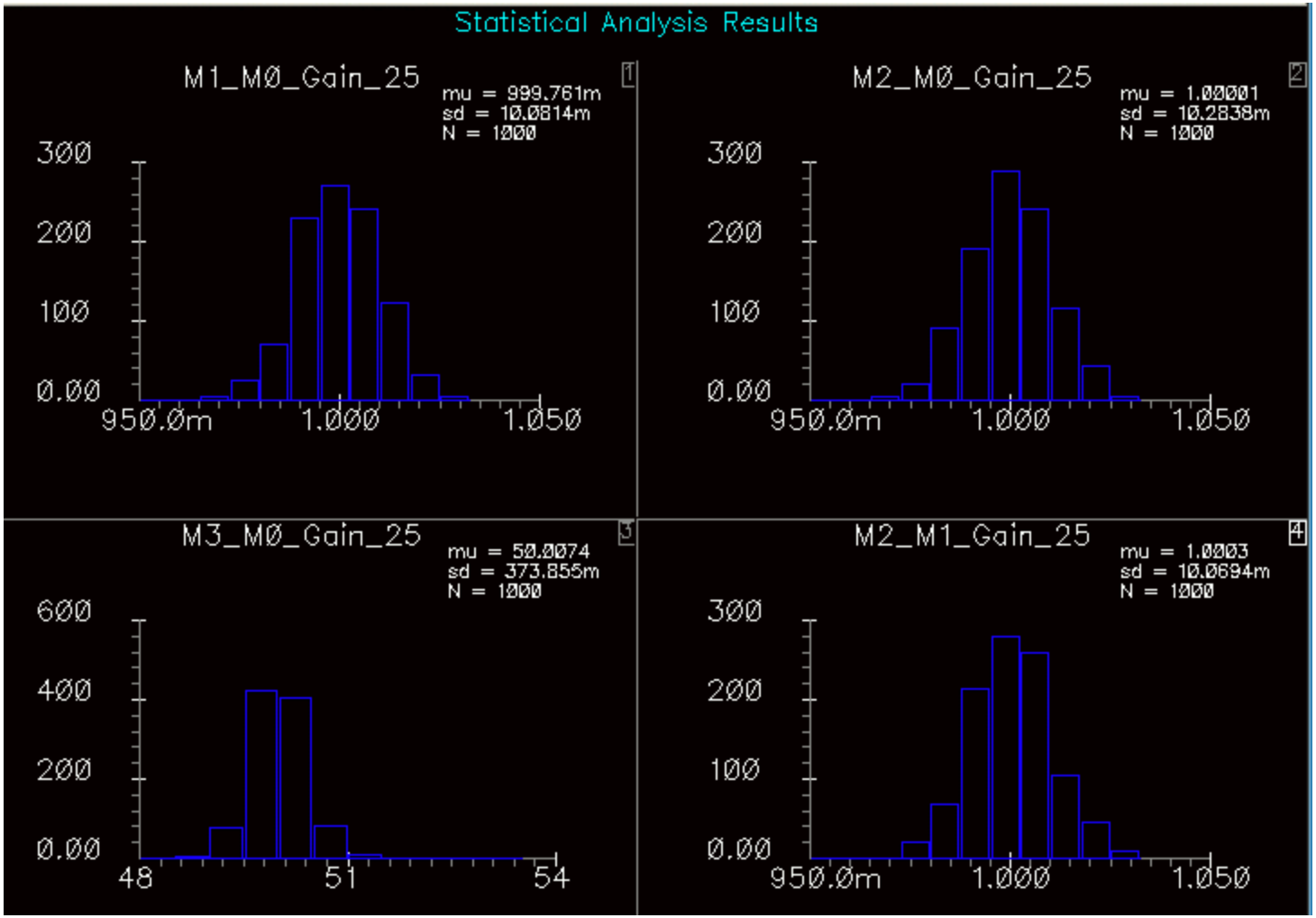
- Answers:
- (1): Any error in the mean is not statistical; the source of the difference in the means is coming from the design and it turns out to be channel length modulation since the input to the mirror's drain is near Vdd and the output to the mirrors' drains are near Ground.
- (2): Even though the 50x mirror transistors all share the same length, they don't share the same self-mismatch fractional error. If you look at the r.s.s portion ( $\sqrt{(.01)^2+(.007)^2}$ ), you can see how **the largest error dominates the sum**. The fractional error of the 50x is actually quite low, so the combination approaches the self-mismatch fractional error of the input transistor or 1%/sqrt(2) = .71%. Remember that for any fractional error combinations…

- How to remove the error in the means? (see next slide)

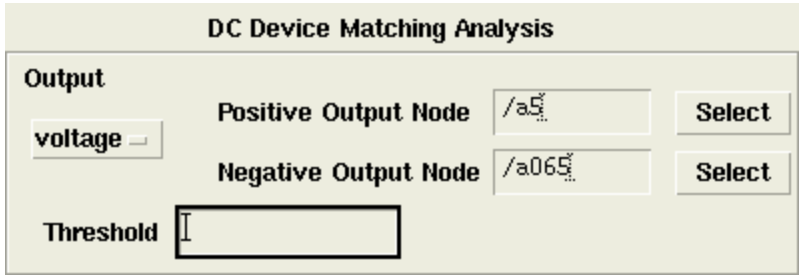
# Don’t forget your friend the cascode!



# Don’t forget your friend the cascode!



# Diff Pair: DCmatch




Similar to Current Mirror except Output is now a voltage and the nodes are the 2 inputs to the diff pair so it reports offset.

```
bsim3v3
sigmaOut    sigmaVth    sigmaBeta   sigmaVg     sigmaIds
12.3 mV     12.3 mV     0 %         12.3 mV     27.5 %      M1
-12.3 mV    12.3 mV     0 %         12.3 mV     27.5 %      M0
2.31 mV     17.6 mV     0 %         17.6 mV     5.16 %      M3
-2.31 mV    17.6 mV     0 %         17.6 mV     5.16 %      M4

2 bsim3v3 with absolute contributions below 0.1 % of maximum not showr


V(a5,a065) = 628.3 uV  +/- 17.73 mV  (3-sigma variation)
```

Offset error of 628.3uV (mean or systematic) and 17.73/3 = 5.9mV 1-$\sigma$ random offset. The DCmatch individual parameters are harder to match up to hand calculations.

sigmaVth for M1 (a differential input transistor) might be expected to be (from DCmatch documentation):

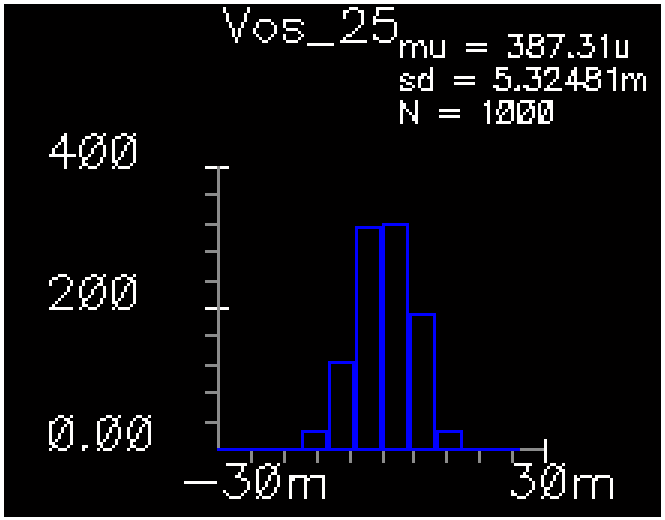
$$\sigma^2(\Delta V_{th}) = \frac{mvtwl^2}{WL} + \frac{mvtwl2^2}{WL^2} + mvt0^2 = \frac{(14.46e-9)^2}{20\mu m * 0.5\mu m} + \frac{(-.191e-15)^2}{20\mu m * (0.5\mu m)^2} + (-26.14e-9)^2 = 20.9e-6$$

$$\sigma(\Delta V_{th})_{self} = 4.6e-3 / \sqrt{2} = 3.3e-3 \qquad 3-\sigma(\Delta V_{th})_{self} = 9.9e-3 \quad !!$$

Which doesn't match up well to the 12.3mV reported in the listing. But, we haven't considered $\Delta$W and $\Delta$L to modify the width/length of the transistor. This transistor is a minimum length transistor, so it turns out that has quite an effect. After using Leff = L – 2$\Delta$Lint, and recomputing we find: $3-\sigma(\Delta V_{th})_{self} = 12.3e-3$ ✓

You can also see the gain reflection to the input for M3/M4.

# Diff Pair: Monte Carlo




- Should have similarly modeled effects as DCMatch.
- Also allows for nonlinear I-V behavior to be accounted for.

Matches better to hand calculations than DCmatch, but not necessary. Ideally, this is more accurate.

# Appendix B – β mismatch check

- Quick check on the assumption that β mismatch is not an issue.
- Fractional β mismatch ~ 2%/sqrt(2*16) = .35%
- Might estimate overall error to be really:

$$\sqrt{(.35\%)^2 + (.95\%)^2} \approx 1.01\%$$

- Didn't really have to oversize the length much (15.6u → 16u) to still get very close to meeting the goal of 1% mismatch in the presence of estimated β mismatch. Conclusion is that typically, β mismatch is not really an issue.

# 50x current mirror gain calculation

- Calculating accuracy of 50x current mirror gain:

$$\frac{\sigma_f}{f} = \sqrt{\left(\frac{\sigma_x}{x}\right)^2 + \left(\frac{\sigma_y}{y}\right)^2} = \sqrt{\left(\frac{\sigma\left(\Delta I_{d\_self\_50x}\right)}{I_{d\_50x}}\right)^2 + \left(\frac{\sigma\left(\Delta I_{d\_self\_1x}\right)}{I_{d\_1x}}\right)^2}$$

- Since 50x current transistor utilizes 50x W, use relationships for $g_m$, $\sigma V_t$, $I_d$ to W:

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_d} \Rightarrow g_{m\_50x} = 50 g_{m\_1x} \;\Big|\; \sigma_{V_t} = \frac{A_{V_t}}{\sqrt{2}\sqrt{WL}} \Rightarrow \sigma_{V_t\_50x} = \frac{\sigma_{V_t\_1x}}{\sqrt{50}} \;\Big|\; I_{d\_50x} = 50 I_{d\_1x}$$

$$\frac{\sigma\left(\Delta I_{D\_self\_50x}\right)}{I_{D\_50x}} = \frac{g_{m\_50x}}{I_{D\_50x}}\sigma\left(\Delta V_{t\_self\_50x}\right) = \frac{50 g_{m\_1x}}{50 I_{d\_1x}}\frac{\sigma_{V_t\_self\_1x}}{\sqrt{50}} = \frac{\sigma\left(\Delta I_{D\_self\_1x}\right)}{\sqrt{50} I_{D\_1x}}$$

$$\frac{\sigma_f}{f} = \sqrt{\left(\frac{1}{\sqrt{50}}\frac{1\%}{\sqrt{2}}\right)^2 + \left(\frac{1\%}{\sqrt{2}}\right)^2} = \sqrt{(.001)^2 + (.00714)^2}$$