Preface

The Verilog Hardware Description Language (Verilog-HDL) has long been the most popular language for describing complex digital hardware. It started life as a proprietary language but was donated by Cadence Design Systems to the design community to serve as the basis of an open standard. That standard was formalized in 1995 by the IEEE in standard 1364-1995. About that same time a group named Analog Verilog International formed with the intent of proposing extensions to Verilog to support analog and mixed-signal simulation. The first fruits of the labor of that group became available in 1996 when the language definition of Verilog-A was released. Verilog-A was not intended to work directly with Verilog-HDL. Rather it was a language with similar syntax and related semantics that was intended to model analog systems and be compatible with SPICE-class circuit simulation engines. The first implementation of Verilog-A soon followed: a version from Cadence that ran on their Spectre circuit simulator.

As more implementations of Verilog-A became available, the group defining the analog and mixed-signal extensions to Verilog continued their work, releasing the definition of Verilog-AMS in 2000. Verilog-AMS combines both Verilog-HDL and Verilog-A, and adds additional mixed-signal constructs, providing a hardware description language suitable for analog, digital, and mixed-signal systems. Again, Cadence was first to release an implementation of this new language, in a product named AMS Designer that combines their Verilog and Spectre simulation engines. At the time this preface was written, all but the oldest commercial circuit simulators support Verilog-A, and each of the major ICCAD vendors offer mixed-signal simulators that support Verilog-AMS. Verilog-A is extensively used in both device modeling for circuit simulation and for behavioral modeling of analog systems and adoption of Verilog-AMS is growing rapidly.

Verilog-AMS is continuing to evolve. Version 2.1 of the Verilog-AMS standard is based on the IEEE Verilog 1364-1995 standard. It was released in January 2003. The committee charged with the development of Verilog-AMS (*www.eda.org/verilog-ams*) is currently working to improve and update the standard. Progress is currently being made to update the basis of the standard to the latest version of Verilog-HDL, IEEE 1364-2001. They are also working to integrate Verilog-AMS into SystemVer-

ilog. Finally, extensions are being added to support compact semiconductor models and table models.

The intent of Verilog-AMS is to let designers of analog and mixed-signal systems and circuits create and use models that describe their designs. Once a design is described in Verilog-AMS, simulators are used to help designers better understand and verify their designs. Verilog-AMS allows designs to be described at the same level as does SPICE, but at the same time allows designs to also be described at higher more abstract levels. This range is needed for the larger more complex mixed-signal designs that are becoming commonplace today.

This book starts in Chapter 1 with a brief introduction to hardware description languages in general and Verilog-AMS in particular. Chapter 2 presents a formal top-down design methodology. While not used extensively today, top-down design is widely believed to be the only methodology available that can efficiently handle large complex mixed-signal designs. This chapter presents a refined and proven top-down methodology that overcomes many of the problems with existing top-down methodologies. Chapter 3 and Chapter 4 introduce the Verilog-A and Verilog-AMS languages. The important concepts of the languages are presented using practical and easy to understand examples. These chapters are intended to be read from beginning to end and are designed to take engineers with a working knowledge of programming concepts to the point where they are comfortable writing a wide range of Verilog-A and Verilog-AMS models. However, they do not cover all the details of the languages. Chapter 5 is a reference guide to the languages. It presents all of the details, but not in a completely linear fashion. Though it can be read from beginning to end, it was written with the expectation that most would use it as a reference, looking up just the details they need when they need them. As such, it, as with the rest of the book, is extensively cross referenced and indexed.

A word about the conventions used in this book. As new ideas and definitions are presented, a few keywords will be set in ***bold italics*** to make them easier to find and to call your attention to them as important points. Code is set in a sans serif font with keywords in **bold** and comments in *italics*. When in text, identifier names are set in *italics*. Acronyms that are spoken as words rather than letters are set in small caps; for example, SPICE. Besides the normal cross references found in the text, you will also find references that appear like this: (5§2.3p157). These abbreviated references include the chapter number, the section number, and finally the page number. Finally, all models presented in this book have been verified with the simulators from Cadence, either Spectre or AMS Designer as appropriate.

This book has two companion websites on which you can find updated information about both this book and its subject matter. *www.designers-guide.com* contains infor-

mation about the book, including an errata sheet, the latest versions of the models given in this book, articles that contain additional information about both modeling and Verilog-AMS, and links to other sites that would be of interest. In addition, it also provides a discussion forum where you can ask questions and have conversations with other practicing design engineers. *www.verilog-ams.com* provides a burgeoning library of high quality user contributed Verilog-A and Verilog-AMS models.

It is our intention to continually update and improve this book. As such, we would like to ask for your help in the process. Please send your comments, suggestions, experiences, feedback and reports of errors to either *ken@designers-guide.com* or describe them at *www.designers-guide.com/Forum*.

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